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Design and performance analysis of universal logic gate

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Abstract

Universal logic gates are the fundamental building blocks of modern digital integrated circuits because every Boolean function can be realized exclusively using either NAND or NOR gates. Due to their functional completeness, these gates form the basis of processors, memory architectures, arithmetic logic units (ALUs), programmable logic devices, finite state machines, and embedded digital systems.

With continuous CMOS technology scaling into the deep-submicron regime, the performance of universal gates is no longer determined solely by logical correctness. Instead, several physical design parameters—including propagation delay, dynamic power consumption, leakage power, transistor sizing, fan-out capability, noise margin, and process variability—significantly affect circuit reliability and efficiency.

This paper presents a comprehensive transistor-level design and performance analysis of two-input CMOS NAND and NOR gates implemented using 45 nm technology. The work investigates the influence of CMOS transistor arrangement on switching characteristics and compares universal gates using important performance metrics such as:

- Average Power Consumption
- Static Leakage Power
- Propagation Delay
- Rise/Fall Time
- Fan-out Capability
- Power Delay Product (PDP)
- Energy Delay Product (EDP)
- Area Efficiency

The paper also compares static CMOS implementation with alternative logic styles including pseudo-NMOS, transmission gate logic, dynamic CMOS, domino logic, and Gate Diffusion

Input (GDI) logic. Finally, the paper discusses future challenges associated with technology scaling below 10 nm.

Keywords: Universal Gate, CMOS, NAND Gate, NOR Gate, Static CMOS, Dynamic CMOS, Power Dissipation, Propagation Delay, Fan-out, PDP, EDP, 45 nm Technology.

1. Introduction

Digital electronics is fundamentally based on logic gates. Every arithmetic operation, decision-making process, communication protocol, and memory operation eventually reduces to combinations of simple Boolean operations.

Among all logic gates, NAND and NOR occupy a unique position because they are **functionally complete**, meaning that every digital circuit can be implemented using only NAND gates or only NOR gates.

Examples include

- Adders
- Multipliers
- Encoders
- Decoders
- Multiplexers
- Flip-Flops
- Registers
- Counters
- CPUs
- DSP processors

Historically, TTL logic families primarily relied on NAND implementations due to transistor economics, whereas CMOS technology supports both NAND and NOR efficiently.

However, as CMOS technology entered nanoscale dimensions (90 nm → 65 nm → 45 nm → 22 nm → 14 nm → 7 nm → 5 nm), several non-ideal effects emerged:

- Short-channel effect
- Drain-induced barrier lowering (DIBL)
- Hot carrier degradation
- Gate leakage

- Subthreshold leakage
- Process variation
- Reduced noise margin

Therefore, evaluating universal gates requires detailed transistor-level analysis rather than simple truth-table verification.

2. Universal Logic Gates

Definition

A universal gate is one that can implement every Boolean function without requiring any other gate type.

Only two logic gates satisfy this condition:

- NAND
- NOR

Mathematically,

NAND(A,B)=AB¯\text{NAND}(A,B)=\overline{AB}NAND(A,B)=AB

NOR(A,B)=A+B¯\text{NOR}(A,B)=\overline{A+B}NOR(A,B)=A+B

NAND Truth Table

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

NOR Truth Table

A	B	Output
0	**0**	**1**
0	**1**	**0**
1	**0**	**0**
1	**1**	**0**

3. CMOS Implementation

3.1 CMOS NAND Gate

The CMOS NAND gate consists of

Pull-Up Network (PUN)

- Two PMOS connected in parallel

Pull-Down Network (PDN)

- Two NMOS connected in series

Working

If any input is LOW

At least one PMOS conducts.

Output becomes HIGH.

If both inputs are HIGH

Both NMOS conduct.

Output becomes LOW.

Advantages

- Faster pull-up
- Strong logic HIGH
- Low leakage
- Good noise margin

3.2 CMOS NOR Gate

The NOR gate reverses the transistor arrangement.

Pull-Up Network

- PMOS in series

Pull-Down Network

- NMOS in parallel

Working

If both inputs are LOW

Both PMOS conduct.

Output HIGH.

If any input becomes HIGH

One NMOS immediately pulls output LOW.

4. Mathematical Analysis

Dynamic Power

Pdynamic=αCLVDD2fP_{dynamic}=\alpha C_LV_{DD}^{2}fPdynamic=αCLVDD2f

where

α = switching activity

CL = load capacitance

VDD = supply voltage

f = operating frequency

Static Power

Pstatic=ILeakage×VDDP_{static}=I_{Leakage}\times V_{DD}Pstatic=ILeakage×VDD

Total Power

PTotal=PDynamic+PStaticP_{Total}=P_{Dynamic}+P_{Static}PTotal=PDynamic+PStatic

Propagation Delay

tp=tPLH+tPHL2t_p=\frac{t_{PLH}+t_{PHL}}{2}tp=2tPLH+tPHL

Rise Time

tr=2.2RCt_r=2.2RCtr=2.2RC

Fall Time

tf=2.2RCt_f=2.2RCtf=2.2RC

Power Delay Product

PDP=P×tpPDP=P\times t_pPDP=P×tp

Energy Delay Product

EDP=PDP×tpEDP=PDP\times t_pEDP=PDP×tp

5. CMOS Transistor Count

Gate	PMOS	NMOS	Total
NOT	1	1	2
NAND	2	2	4
NOR	2	2	4
XOR	6	6	12
XNOR	6	6	12

6. Simulation Methodology

The proposed circuits are simulated using:

- Technology Node: 45 nm CMOS
- Supply Voltage: 1.0 V
- Temperature: 27°C
- Frequency: 100 MHz
- Load Capacitance: 10 fF
- Input Slew Rate: 100 ps
- Simulation Tool:
  - Cadence Virtuoso
  - LTspice
  - Microwind
  - Tanner EDA
  - HSPICE

Transient simulations are performed for all four input combinations.

Measured outputs include

- Delay
- Current
- Output waveform
- Leakage current
- Rise time
- Fall time

7. Performance Metrics

Average Power

Measures total energy consumed during switching.

Leakage Power

Dominates nanoscale CMOS.

Includes

- Gate leakage
- Junction leakage
- Subthreshold leakage

Propagation Delay

Measured between

50% input voltage

↓

50% output voltage

Fan-Out

Maximum number of CMOS inputs driven without violating timing.

Typical CMOS fan-out

10–20

Noise Margin

NMH=VOH−VIHNM_H=V_{OH}-V_{IH}NMH=VOH−VIH

NML=VIL−VOLNM_L=V_{IL}-V_{OL}NML=VIL−VOL

Static CMOS provides superior noise immunity compared with ratioed logic.

8. Comparative Analysis

Parameter	NAND	NOR
Propagation Delay	Lower	Higher
Leakage	Low	Moderate

Power	Low	Higher
Pull-up Speed	Fast	Slow
Pull-down Speed	Moderate	Fast
Fan-out	Higher	Moderate
Noise Margin	Excellent	Excellent
Area	Same	Same

Reason: Series PMOS in NOR possess higher resistance than parallel PMOS in NAND, resulting in increased delay.

9. Comparison with Other Logic Styles

Logic Style	Power	Delay	Area	Noise Margin
Static CMOS	Low	Low	Moderate	Excellent
Pseudo NMOS	High	Fast	Small	Poor
Transmission Gate	Very Low	Low	Small	Good
Dynamic CMOS	Very Low	Very Fast	Small	Moderate
Domino Logic	Low	Fast	Moderate	Moderate
GDI	Very Low	Very Low	Very Small	Reduced

10. Applications

Universal gates are used in

- CPU datapaths
- Arithmetic Logic Units
- Register Files
- SRAM
- Cache Memory
- FPGA LUTs
- DSP Chips
- AI Accelerators
- Neural Network Hardware
- Automotive Electronics
- IoT Devices
- Space Electronics

11. Future Scope

Emerging technologies are transforming universal gate design.

Future research directions include

- FinFET-based NAND/NOR gates
- Gate-All-Around (GAA) FET implementations
- Carbon Nanotube Field Effect Transistors (CNTFET)
- Tunnel FET (TFET)
- Quantum-dot Cellular Automata (QCA)
- Reversible Logic
- Adiabatic Logic
- Spintronics
- Approximate Computing
- Near-threshold Computing
- AI-assisted transistor sizing
- Machine Learning-based power optimization

12. Conclusion

The study demonstrates that universal logic gates remain indispensable components of digital integrated circuits. Although NAND and NOR gates are logically equivalent, their electrical characteristics differ significantly because of transistor arrangement within the pull-up and pull-down networks. CMOS NAND generally achieves lower propagation delay and reduced power consumption due to its parallel PMOS configuration, whereas CMOS NOR experiences higher pull-up resistance resulting from series PMOS transistors, leading to increased delay.

Static CMOS continues to provide the best balance of full voltage swing, low static power, and high noise immunity, making it the preferred implementation for reliable VLSI systems. Alternative logic styles such as dynamic CMOS, transmission-gate logic, and GDI can offer advantages in specific applications but often involve trade-offs in robustness, leakage, or design complexity.

Future work should extend this analysis through post-layout extraction, process-voltage-temperature (PVT) variation studies, Monte Carlo simulations, and implementation using advanced device technologies such as FinFETs and Gate-All-Around transistors to better reflect modern semiconductor fabrication processes.

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