COMPARATIVE ASSESSMENT OF InGaAs/InP AND SILICON BASED DG MOS-HEMT

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ABSTRACT

In this paper we have performed a comprehensive comparative assessment of InGaAs/InP and Silicon based DG MOS-HEMT is done using 2D Sentaurus TCAD simulation. III–V heterostructure device has narrowband $In_{0.53}Ga_{0.47}As$ and wideband InP layers for body, and high-K gate dielectric. Drift diffusion model is used for simulation and variable gate length is considered. Benchmarking of simulation results show that III–V device provides higher ON current, lesser delay, lower energy delay product and lower DIBL than silicon device. However III–V device has higher SS and lower I_{on}/I_{off} ratio and V_t than silicon device. The results indicate that there is a need to optimize the I_{on}/I_{off}, SS and DIBL values for specific circuits.

Keywords: MOS-HEMT, DIBL, SS, Delay, EDP, Vt, Ion/Ioff ratio TCAD, InGaAs/InP MOS-HEMT, Silicon.

I. INTRODUCTION

For the last four decades, the microelectronic industry has been benefited enormously due to MOSFET miniaturization. The shrinking of transistors dimensions below 100 nm enabled hundreds of millions transistors to be fabricated on a single chip. As MOSFETs are scaled (decrease in horizontal and vertical dimensions), the switching speed increases, power dissipation decreases and packing density increases exponentially [1, 2]. But the reduced gate length leads to detrimental short channel effects (SCEs) such as increased DIBL, increased Sub threshold slope (SS), reduced I_{on}/I_{off} ratio, reduced delay, etc. These SCEs adversely affects the device and circuit performance. To overcome these SCEs advanced MOS structures such as Double Gate (DG), FinFETs, surround gate, etc are extensively investigated. The DG MOSFET is particularly very popular due to excellent electrostatic gate control which offers immunity to SCE and better scalability [3].

To further enhance the switching capability III-V compound semiconductor came up. In the commonly used III-V compound, InGaAs based devices showed improved switching capability. The InGaAs have much higher mobility and offers much higher speed than silicon based devices. In the DG MOSFET structures some groups have used InGaAs as the channel material to improve switching capability. However, to further enhance the capabilities Heterostructures may be useful option. Heterostructure consists of a wide band gap semiconductor grown on a lattice matched narrow band gap semiconductor. This combination leads to the formation of a quantum well with a 2DEG confinement having very high mobility.

The intent of this work is to combine the advantages of heterostructures (used in HEMT like structures) and the DG MOSFETs. The combination of the HEMT and DG MOSFET would result in the novel DG MOS-HEMT device. The novel InGaAs/InP device would give high performance like high ON current due to HEMT like structure and reduced SCEs due to DG-MOSFET like structure. The use of InGaAs/InP would offer very high switching speed due to high mobility in these compounds.

Some groups have reported AlGaN/GaN and AlInN/GaN single gate MOS-HEMTs. The InGaAs/InP heterostructure based DG MOS-HEMT has not been reported yet. Thus, for the first time we report a comprehensive comparative investigation of this novel device with silicon counterpart. This study would certainly help us in establishing this novel device for low power high frequency switching application. Extensive device simulations of major device metrics such as drain induced barrier lowering (DIBL), sub threshold slope (SS), delay, V_t, ,I_{on}/I_{off} ratio, and energy delay product have been done for a wide range of gate lengths (L_g).

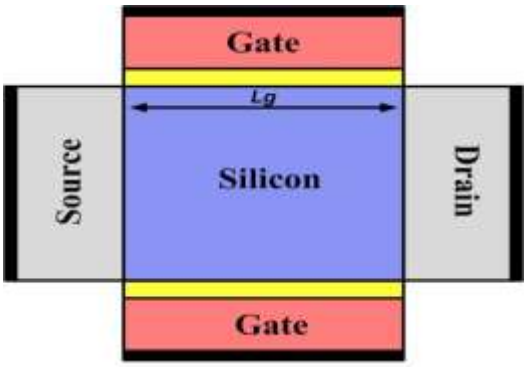

Fig 1A The device structure of silicon DG MOS-HEMT. Source/drain region doping is 10^{20} cm^3 with 5 nm length. The gate length *Lg* is varied from 12 nm to 18 nm, the oxide thickness *t*ox is 1.2 nm and body thickness is 16 nm.

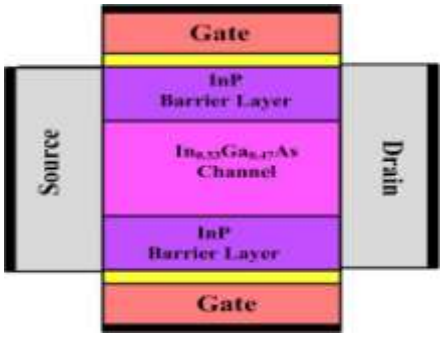

Fig. 1B III–V heterostructure based InGaAs/InP DG MOS-HEMT. The channel consists of undoped narrowband (*t*2) region and two wideband (*t*1) regions. Region *t*2 = 10 nm uses In0.53Ga0.47As region, *t*1 = 3 nm uses InP. Source/drain region doping is 10^{20} cm^3 with 5 nm length. The gate length *Lg* is varied from 12 nm to 18 nm, the oxide thickness *t*ox is 1.2 nm and body thickness is 16 nm.

II DEVICE STRUCTURE

The Silicon based DG MOS-HEMT is shown in Fig. 1A (Device 1) and Fig. 1B shows the InGaAs/InP DG MOS-HEMT (Device 2) structure used for the performance assessment. In Fig. 1B the III–V heterostructure consisting of narrowband $In_{0.53}Ga_{0.47}As$ layer of 10 nm region and two wideband InP (t_1) layers of 3 nm. The gate lengths of the both devices are varied from 12 nm to 21 nm in steps of 3 nm. The InGaAs/InP DG MOS-

HEMT channel is intentionally kept undopped. The device 1 has channel consists of silicon with body thickness of 16 nm. The simulated device structures have source/drain regions doped at 10^{20} cm^3 and uses abrupt doping at source/drain ends. The source/drain lengths are 5 nm, the top and bottom gate has equivalent oxide thickness of t_{ox} = 1.2 nm. Device 1 uses SiO_2 (silicon dioxide) and device 2 uses high dielectric constant HfO_2 (hafnium dioxide) to minimize leakages.

Physical properties of narrow band gap $In_{0.53}Ga_{0.47}As$ materials and wideband gap InP materials are listed in the table. The $In_{0.53}Ga_{0.47}As$ having excellent electron mobility is used for narrowband gap layer and lattice matched InP is used for wide band gap layer. Narrow band gap material is sandwiched between the two wideband gap barrier layers and the channel is confined at the heterostructure interface. The barrier layer used has the conduction band edge offset with the channel and is nearly lattice matched with the narrowband layer to minimize the traps at its interface with the channel [4].

Table 1. Physical Properties of In0.53Ga0.47as and InP

Material	E_g (eV)	CBO (eV)	VBO (eV)	ε_0	Lattice constant, Å	μ_e, $cm^2/(Vs)$	μ_h, $cm^2/(Vs)$
InP	1.344	_	_	2.5	5.867	5400	200
$In_{0.53}Ga_{0.47}As$	0.74	0.22	0.38	13.9	5.868	12000	300

III. SIMULATION FRAMEWORK AND EXPERIMENTAL COMPARISON

For validating the simulation model, the comparison of simulated and experimental transfer characteristics of the single gate InGaAs/InP MOS-HEMT [5] is done. The model parameters are chosen to get perfect matching between experimental and simulation results. After matching is done, the model is then applied for simulating the proposed DG MOS-HEMT, which is also having similar body material combination (InGaAs/InP). Two-dimensional drift-diffusion (DD) numerical simulations are done with the Sentaurus TCAD device simulator G2012.06. [6].The numerical simulator uses DD model to solve self- consistently the Poisson's equation with carrier continuity equation. We have used Canali mobility model [7] with suitable modifications to precisely capture the non-equilibrium carrier transport.

$$\mu(E) = \frac{(\alpha+1)\mu_0}{\alpha+\left[1+\left(\frac{(\alpha+1)\mu_0 E}{v_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \qquad (1)$$

The model parameters are determined by matching the simulation with the experimental results. The parameters applied to do the calibration include low field mobility $\mu 0 = 10000$ cm^2/Vs, α=0 and β=0.6

(constant reflecting the steepness of the carrier velocity profile in the channel). The default values for electrons are saturation velocity v_{sat}=0.93×10^7cm/s and β=2. However, as per the approach adopted by Bude [8], we use high saturation velocity (v_{sat} = 9.5 x 10^7 cm/s) and lower than unity value for beta (β=0.6) within the drift-diffusion simulation to account for the velocity overshoot effect at high fields and to maintain the correct

velocity at low fields. Literature values are adopted for a band gap, electron affinity [9] and interface traps density [5]. The TaN work function Φ_{ms}=4.65 eV [10] is used in the simulation. Traps values are defined to be acceptor like from the conduction-band edge E_C to the charge-neutrality level E_{CN} and donor like from E_{CN} to the valence-band edge E_V [11]. We have also implemented band gap narrowing across all regions in the

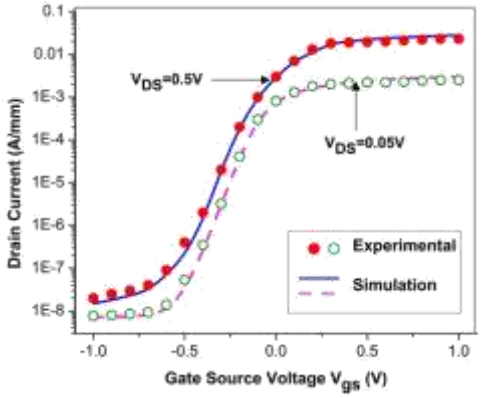

Fig. 2. Experimental (Symbols) And Simulated (Solid Lines) Transfer Characteristics For Ingaas/ Inp Buried Channel DG MOS-HEMT [5] After Tuning The Simulation Mode To Match The Experimental Curve.

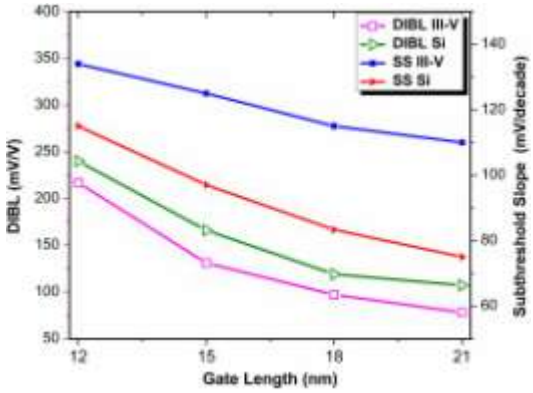

Fig. 3. DIBL and SS as A Function of Gate Length. *Lg* is Varied From 12 Nm to 21nm. the SS is Extracted at *Vds*=0.05V.

simulation because if band gap narrowing ignored there will distortions in energy band diagrams and electron transport across regions of potential barriers may be blocked. For recombination, the Shockley–Read–Hall (SRH) model is used with SRH, radiative and Auger recombination values chosen are: t_{SRH}=60 ns, C_{rad}= 1.4x10^{9} cm^{3}/s, and C_{Auger}=4x10^{29} cm^{6}/s [11]. The transfer characteristics (Fig. 2) show very good agreement between the experimental and simulated results for both high and low drain bias voltages, thus validating our approximation of the carrier transport model and other model parameters. As the model is validated, extensive simulations for DG MOSHEMT are done by introducing the gate length variation in the device structure.

IV. RESULT AND DISCUSSION

Fig. 3 shows the drain induced barrier lowering (DIBL) and Sub threshold slope (SS) as a function gate length variation from 12 nm to 21 nm. As gate length changes from 12 nm to 21 nm, the DIBL decreases from 350 mV/V to 270 mV/V and SS from 130 mV/decade to 110 mV/decade, whereas for Silicon device for the same variations in the gate, the change in DIBL is from 280 mV/V to 70 mV/V and the change in SS is from 280 to

75 mV/decade. Thus, DIBL increase drastically with small gate length. When the gate length changes from low to high the channel area near the drain end is tightly controlled by both front and back gate, and thus DIBL will decrease to low value.

Fig.4 shows the impact of the gate length on threshold voltage (V_t) and ratio of I_{on}/I_{off} for both devices. The gate length variation results in modulation of effective channel length. Larger values of gate length results

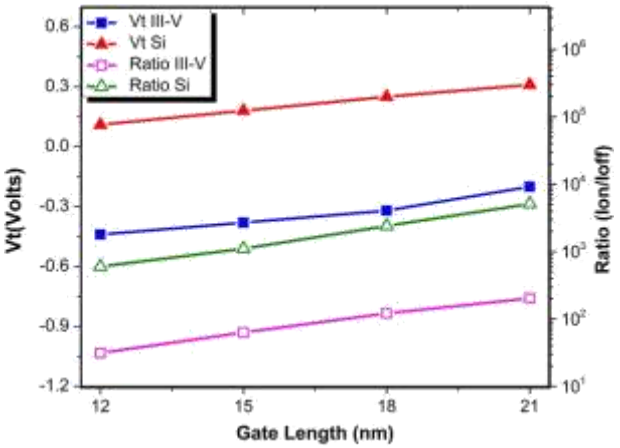

Fig.4. Threshold voltage and ratio of I_{on}/I_{off} as a function of gate length. L_g is varied from 12 nm to 21nm.

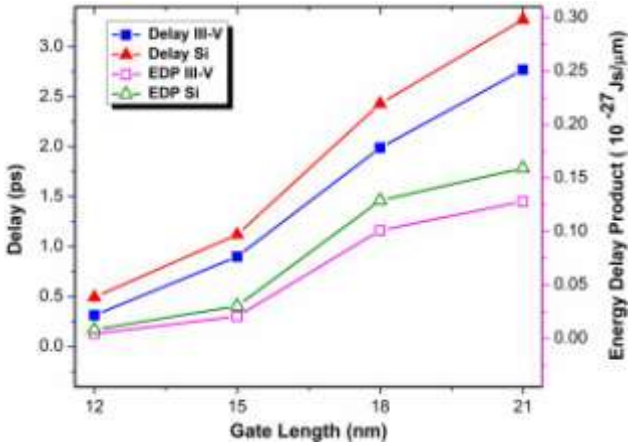

Fig. 5 Device Delay and Energy Delay Product as a Function of Gate Length. *Lg* is Varied from 12 Nm to 21nm.

in increased V_t and the ratio of I_{on}/I_{off}. The V_t increases from ~0.45 V to ~0.2V as gate length increases from 12 nm to 21 nm. The variation in current ratio is almost linear with respect to gate length. Ratio increases from 5000 to 10000 as gate length increases from 12 nm to 21 nm.

Fig.5 shows the intrinsic device delay (in ps) and energy delay as a function of the gate length. The intrinsic delay of the device depends on gate capacitance C_g, I_{on} and V_{DD}. The gate capacitance decreases as gate length increases [12], which results in increase current ratio of device. The energy delay product is also increases. The delay of the device changes from 0.5 to 4 ps and the EDP of the device changes from.00 to 0.12. The change in EDP is less compare to device delay in our MOSHEMT..Thus reduction in gate length reduces device delay and EDP.

V. CONCLUSION

The comparative assessment of InGaAs/InP DG MOS-HEMT and Silicon based DG MOSFET is

comprehensively done for a wide variation in gate length using sentarus TCAD simulation. Heterostructure devices using narrowband ternary III–V materials, such as $In_{0.53}Ga_{0.47}As$ and wideband InP, with high dielectric provides higher ON current, lesser fall in SS with respect to change in gate length, lesser delay, lower energy delay product and lower DIBL than the silicon based devices. Results also indicate that Heterostructure device has good electrostatic control. However, higher SS and lower I_{on}/I_{off} are some of the concerns which need to be addressed.

VI. ACKNOWLEDGMENTS

Authors would acknowledge the Faculty of Engineering Department of Electronics and Telecommunication Engineering, Jodhpur National University, Jodhpur, Goverenment Polytechnic Mumbai and K J somaiya polytechnic Mumbai for support this research work.

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