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Design and Implementation of a low power high speed full adder cell for low power applications

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Abstract

This review paper explores in detail the development and application of a highspeed, low-power complete adder cell unit that is suited for energy-efficient applications. Important topics covered in the study are architecture, design process, best practices for performance, and relevant performance measurements. It also discusses recent developments, obstacles, and opportunities in the field of low-power high-speed full adder cell units.

Keywords- Full Adder, Transmission gate, Low Power

I. INTRODUCTION

Full adders play a crucial role in the rapidly changing field of VLSI circuit design, where quick computation times combined with low power consumption are essential. These basic building blocks have gained increased importance in the complex architectures of Arithmetic Logic Units (ALUs) found in microprocessors and digital signal processing chips. As technology has advanced, many versions of adder cells have appeared, each with unique benefits and disadvantages.

In the initial phases of VLSI design, Complementary Pass Logic (CPL) was implemented using only n-channel CMOS (nMOS). But as the field developed, the ability to reduce excessive power loss and transistor count led to the replacement of CPL with static complementary CMOS (CCMOS) technology, which combined p-channel CMOS (pMOS) and nMOS transistors. Later, alternatives that required fewer transistors were introduced with the development of Transmission Function Adder (TFA) and Transmission Gate Adder (TGA), opening up promising paths for more efficient designs.

Three main techniques have been identified in the field of traditional full adder design, which is defined by a single logic style: CPL, C-CMOS, and TGA. But recent work has clearly moved in the direction of hybrid adders, which combine the advantages of several logic approaches. In recent studies, hybrid logic designs with 24 transistors (24-T), 14 transistors (14-T), and 10 transistors (10-T) have been investigated. Each design offers a distinct combination of benefits.

In addition, scientists have experimented with novel hybrid architectures, including Double Pass Transistor Logic (DPL), Hybrid Pass Static CMOS (HPSC), and Swing Restored Complementary Pass Logic (SR-CPL). Notably, K. Navi et al. have introduced a novel paradigm to address the enduring trade-offs in speed, power consumption, and overall performance by straying from traditional CMOS implementations and using capacitors in their full adder design.

This paper explores the details of these various full adder designs to give a thorough overview and comparative analysis. In the context of 180 nm technology, simulation studies carried out with Cadence CAD tools provide a modern perspective for examining and assessing the performance characteristics of these adder cells. The goal of this investigation is to clarify the advantages and disadvantages of each design in order to advance our understanding of the dynamic environment surrounding full adder implementations in VLSI circuits.

II. LITERATURE REVIEW

In [1] This paper presents a new hybrid Full Adder (FA) design that makes use of Conventional Complementary Metal Oxide Semiconductor (CCMOS) logic, Pass Transistors (PTs), and Transmission Gates (TGs). The purpose of the proposed FA is to improve performance, especially in the areas of power consumption and delay, which are critical for high-speedCPUs. Four primary modules comprise the FA design: two dedicated to carry generation and two for sum generation. While sum generation cascades two XOR modules using TGs and PTs, carry generation uses a unique

AND-OR module based on TG and CPL logic. Every module is made to fulfil certain requirements in order to guarantee proper operation. Utilising Cadence tools, simulation results in a 45 nm technology node show that the suggested FA outperforms previous designs in terms of delay and Power Delay Product (PDP). Despite not being the most powerefficient, the suggested FA is still useful in contemporary processors.

Additional examination expands the FAs to diverse bit lengths up to 64 bits, emphasising the scalability of the suggested architecture. Remarkably, operability at 64 bits is demonstrated by only five of the twenty FAs that currently exist in addition to the suggested design. The final section of the paper discusses the drawbacks of some FAs, like high latency that prevents scalability, and offers optimisation techniques for upcoming technologies, highlighting the significance of interconnect optimisation for better performance. All things considered, the suggested hybrid FA design offers a viable way to improve the arithmetic unit performance in microprocessors, especially with regard to scalability, delay, and power consumption.

In [2] The goal of this paper's new low-power hybrid 1-bit full adder design is to maximise power, delay, and transistor count for efficient VLSI applications. Strong transmission gates and weak CMOS inverters are combined in the proposed adder to maximise switching speeds and minimise power consumption. Thorough simulations conducted in 90nm and 180-nm technologies demonstrate that the proposed design outperforms existing techniques, with a significant reduction in propagation delay (224 ps) and average power consumption (4.1563 μW) at a 1.8-V supply in 180-nm technology. Moreover, the design is expanded to a 32-bit carry

propagation adder while maintaining the improved performance, demonstrating the practicality and scalability of the proposed approach.

The new features of the proposed hybrid full adder—strong transmission gates and weak inverters—along with a careful analysis of area, delay, and power consumption represent a significant advancement in VLSI design. The suggested hybrid full adder is now in a competitive and effective position for other VLSI applications that require improved power-delay characteristics, as well as the evolving field of battery-operated portable devices, thanks to the promising results, which are confirmed by thorough simulations and comparisons with current designs.

In [3] The work presents a novel approach to enhancing the performance of 1-bit adder cells, which are crucial components of numerous microprocessors and VLSI systems. The hybrid logic-based 1-bit adders that are proposed perform better than their existing counterparts because they combine CMOS inverters and strong transmission gates. To achieve lower power consumption, faster switching, and increased energy efficiency, the number of transistors in the structure can be reduced, strong transmission gates can be used, and transistor sizes can be optimised. Using the design principles, two versions of the 1bit adder are implemented that show improvements in terms of overall performance and power-delay product (PDP). Simulations and post-layout analyses validate the effectiveness of the proposed method and show that these hybrid logic-based adders are promising candidates for application in modern VLSI technologies. The study also extends the application of the recommended 1-bit adders to an 8-bit ripple carry adder (RCA), demonstrating the scalability and compatibility of these adders with larger circuits. Compared to earlier designs, the hybrid logic-based 8-bit RCA exhibits notable improvements in delay performance, suggesting that the proposed approach is feasible for larger-scale implementations. The smaller silicon area, achieved through careful layout design, further supports the practical applicability of the suggested adders. All things considered, this research tackles the critical problems of speed, energy efficiency, and power consumption in contemporary VLSI systems, making a substantial contribution to the design and optimisation of adder cells.

In [4] In this work, a new design for a Hybrid Full Adder (HFA) that integrates CMOS, Pass Transistor Logic (PTL), and Transmission Gate Adder (TGA) technologies is presented. The study tackles the urgent need for Very Largescale Integration (VLSI) circuits that are energy-efficient and necessary for electronic devices that run on batteries. The proposed HFA, realised in 90-nm technology, shows a notable improvement in performance metrics, such as a better Power-Delay Product (PDP) and lower power consumption when compared to traditional CMOS designs. The technology offers a feasible solution for low-power applications in portable electronics, including bioelectronics, smartphones, and personal computers, since its innovative design only requires 13 transistors. Simulation results validate the functionality of the HFA, and comparisons with existing designs demonstrate its superiority. This makes it a
desirable choice for modern computing systems where optimising speed and power efficiency is essential.

Additionally, the research emphasises the broader implications of hybrid technology on the development of microelectronic circuits, focusing on the fundamental logic module of a one-bit Full Adder. By carefully

addressing their limitations, the study offers important insights into the benefits and trade-offs of various logic styles, such as Transmission gate FA, dynamic CMOS logic, and static CMOS logic. Furthermore, by concentrating on the core logic module of a one-bit Full Adder, the study highlights the wider consequences of hybrid technology on the advancement of microelectronic circuit development. The study provides significant insights into the advantages and trade-offs of different logic styles, including Transmission gate FA, dynamic CMOS logic, and static CMOS logic, by carefully addressing their limitations.

In [5] The paper presents a novel hybrid Full Adder (FA) design that outperforms its predecessors in terms of speed and Power Delay Product (PDP). The four primary components of the suggested FA's design are meticulously planned and employ state-of-the-art techniques such as Complementary Pass Transistor Logic (CPL), Transistor Gates (TG), and Gate Diffusion Input (GDI). The simulation results using Cadence tools in a 45 nm technology node demonstrate that the suggested FA performs better in terms of delay and PDP, even though it might not be the most power-efficient. The study also extends its analysis to the scalability of FAs, discovering that the proposed design and a very limited number of other designs can operate flawlessly without intermediate buffers in a 64-bit word length configuration. This scalability analysis showcases the potential of the proposed hybrid FA for integration into modern computer systems, which need efficient and fast adders for complex operations.

The driving capability test validates the recommended FA's performance across a range of output loads and draws attention to its beneficial aspects. The study highlights the importance of considering performance and scalability under different load scenarios, which provides valuable insights into FA design strategies. It appears that the suggested FA is a good fit for next-generation computing architectures, where efficiency and speed are important considerations, since it demonstrates notable benefits, particularly in longer wordlength configurations.

In [6] The study presents a novel and efficient 1-bit full adder (FA) design based on a hybrid approach using 20 transistors, with a focus on addressing issues related to decreasing MOS transistor sizes. The suggested design, which utilizes carbon nanotube field effect transistors (CNTFETs) instead of existing counterparts at 90 nm technology, shows a notable improvement in performance metrics like delay and powerdelay product. The design shows improvements between 13.01% and 59.20% based on a comprehensive comparison using the Cadence Virtuoso tool, indicating its efficacy in resolving threshold voltage issues and improving driving capacity. The suggested FA design's robustness and versatility for integration into high-performance Very Large Scale Integration (VLSI) applications are further demonstrated by its resilience under varying supply voltage and process corner conditions.

The study also sheds light on the larger background of the difficulties facing semiconductor technology, emphasises the necessity of researching substitute materials and technologies to get around issues like elevated leakage power and short channel effects. The suggested FA design is a practical illustration of the benefits these alternative technologies offer, and the use of CNTFETs seems to be a feasible option. As the semiconductor industry changes, the study encourages further research into cutting-edge strategies that take advantage of the

unique properties of materials like carbon nanotubes to advance the development of low-power, highspeed circuits necessary for applications like digital image processing, digital signal processing, and graphics processing units.

III. RESULT AND ANALYSIS

[1]This study compares and contrasts multiple full adders in great detail and provides a thorough analysis of their benefits and drawbacks. Given that different adders employ different strategies and logic styles that have evolved over time, a detailed examination of their performance characteristics is necessary to determine the benefits and drawbacks of each adder. In this study, Cadence Virtuoso tools are used to simulate and practically implement adder cells. In every instance, the same 90 nm technology is used. The findings of the study are a helpful resource for VLSI designers as they enable the careful selection of the optimal complete adder cell based on the requirements of a particular system. This work advances the field of VLSI circuit design by providing designers with a helpful manual to follow when making decisions to achieve optimal performance in terms of speed, power consumption, and other important parameters.

[2]This study presented a low-power hybrid 1-bit full adder design that was expanded to a 32-bit setup. The suggested adder was extensively compared to well-known design methodologies such as CMOS, CPL, TFA, TGA, and other hybrid designs using 180/90-nm technology and standard Cadence Virtuoso tools. The simulation's output demonstrated how much better the Power-Delay Product (PDP) was than earlier designs. Sturdy transmission gates powered by feeble CMOS inverters were cleverly combined to allow for rapid switching (224 ps at 1.8 V supply) in a 102.94 μm^2 layout area (in 180 nm technology, buffer-free). Specifically, the proposed full adder demonstrated an amazing 20.56% improvement in PDP over the best-reported design at 1.8 V in 180-nm technology. The application of the proposed full adder was extended to a 32-bit carry propagation adder. Three stages of optimal performance were produced by carefully positioned buffers. Remarkably, the achieved PDP improvement reached 27.36% when the same design was implemented in 90-nm technology at a 1.2-V power supply. These results demonstrate the efficiency and scalability of the proposed hybrid full adder design in raising the bar for low-power VLSI applications.

[3]In order to show how scalable and compatible these adders are with larger circuits, the study also applies the suggested 1-bit adders to an 8-bit ripple carry adder (RCA). The hybrid logic-based 8-bit RCA shows significant improvements in delay performance over previous designs, indicating that the suggested method is feasible for largerscale implementations. The recommended adders' practical applicability is further supported by the smaller silicon area, which was attained through meticulous layout design. All things considered, this research significantly advances the design and optimisation of adder cells by addressing the pressing issues of speed, energy efficiency, and power consumption in modern VLSI systems.

[4]One notable achievement in VLSI circuit design at 90 nm technology is the 1-bit Hybrid Full Adder (HFA), which was designed using the Cadence Virtuoso platform. With only 13 transistors, the HFA design is more

energy-efficient than other Full Adder (FA) designs. This reduces power consumption and delay. The HFA performs significantly better, as demonstrated by the experimental results, which show that it only consumes 16.889 µW of power, delays 20 ns, and has an outstanding Power-Delay Product (PDP) of 137.78 fJ. The circuit's low transistor count makes it compact, which emphasises its potential for uses where space is a critical consideration. It is recommended that further research be done in the future to look at the area characteristics of the circuit, such as layout studies. Moreover, an interesting way to boost overall performance in cutting-edge computer systems is to extend the HFA design to higher bit-width configurations in various nanometer technologies, such as 32-bit and 64-bit Ripple Carry Adders.

[5]In this study, VLSI circuit design is examined, with a
focus on selecting the right logic style for implementing a full adder (FA) circuit. By using a hybrid design approach, VLSI designers can choose different modules that best fit their specific needs. The study presents a new 1-bit FA design that uses 20 transistors in this hybrid framework. Notably, the proposed method effectively resolves the threshold voltage problem and enhances driving capability. A detailed comparison using the Cadence Virtuoso tool at 90 nm technology shows notable improvements when benchmarked against leading counterpart circuits, with delays ranging from 13.01% to 54.93% and power-delay product (PDP) from 13.01% to 59.20%. Performance analyses conducted under a range of supply voltages and process corner conditions validate the suitability of the suggested design for highperformance VLSI applications and substantiate its robustness.

[6]This work presents a novel implementation of a 1-bit full adder (1b-FA) and a carry look adder (CLA) using carbon nanotube field effect transistors (CNTFETs with a minimal transistor count. Previous full adder designs are surpassed by the suggested design in terms of power consumption, delay, and power-delay product. The successful implementation of the suggested design approach is supported by the simulation results, which corroborate the theory that a greater number of transistors corresponds to a lower average power. Using 32 nm CNTFET technologies, the 1b-FA10 circuit is used to design a 4-bit carry look adder (4b-CLA) with a measured delay of 5.876 ps and a power consumption of 0.062 W. The findings demonstrate the low-power applications suitability of CNTFET technologies and establish them as a competitive alternative to traditional metal oxide semiconductor fieldeffect transistors (MOSFETs). The practicality of the proposed 1b-FA10 design is demonstrated by its effective application in logical unit cores, arithmetic, and computational design, particularly in comparison to MOSFET alternatives.

IV. COMPARISON TABLE: -

Parameters Value	[1]	[2]	[3]	[4]	[5]	[6]
Average Power (µW)	2.42	1.5799	6.28	25.507	25.8	0.184

Total Delay (ps)	510.6	1269	304.25	6482	36.1	33.881
Power Delay Product (PDP) (aj)	1240	200.489	1910.69	165330	931.38	6.258
Leakage Power (nW)	---	---	0.9	---	---	---

CONCLUSION

From early implementations such as complementary pass logic (CPL) to more sophisticated static complementary CMOS (C-CMOS), transmission gate adder (TGA), and transmission function adder (TFA) techniques, the evolution of full adder designs for Very Large-scale Integration (VLSI) circuits has been observed. A growing number of researchers are investigating hybrid adders, which combine several logic styles to take advantage of their individual benefits and improve overall performance. A variety of creative designs are showcased in the literature review, including hybrid logic-based adders, low-power hybrid 1-bit full adders, and new applications that use carbon nanotube field effect transistors (CNTFETs). Simulations carried out with tools such as Cadence Virtuoso demonstrate notable reductions in delay, power consumption, and Power-Delay Product (PDP). These results highlight the continued search for effective, low-power VLSI circuits that take into account important factors like power consumption, speed, and energy efficiency. The presented research serves as a thorough guide to help VLSI designers navigate the complexities of adder selection. It also paves the way for future developments in digital computation technologies by providing insightful information.

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