International Journal of Advance Research in Science and Engineering
Volume No. 12, Issue No. 06, June 2023
www.ijarse.com
IJARSE
ISSN 2319 - 8354

Performance Evaluation and Synthesis of IIR Filters Using Various Multipliers Algorithms

Vaishali Sharma and R. P. Agarwal

Abstract:
As sensors and network-enabled devices improve, there is an increasing desire for great efficiency and low power use. The main delaying element of these devices is the multiplier included within used in signal processing applications are digital filters. In order to create infinite impulse response (IIR) filters of orders four, eight, sixteen, thirty-two, and sixty-four, this paper suggests the The design of several conventional and traditional multiplier algorithms is examined, along with the latency, memory utilization, and amount of logic used in the suggested algorithms' performance.

Keywords*: IIR digital filter , Delay , FPGA ,Verilog HDL, Filter design and analysis (FDA) , Matlab, LUTs.*

1 Introduction

Natural phenomena are examples of the many different signal types that are employed in several signal processing and telecommunication applications, including human speech, audio signals, seismic waves, etc. Many fields incorporating data communication, radar, seismology, and sonar, biomedical engineering, and a lot more, have used signal processing for many years. Digital signal processing (DSP) is a vital modern instrument that digitally transforms analog input inputs, analyzes those signals, and then converts the conclusions back to analog signals. DSP is used in a variety of scientific and technical domains.

DSP systems were introduced as a result of recent developments in integrated circuit technology and the creation of complex signal processing algorithms. IIR (infinite impulse response) filtering is a critical step in many DSP applications. Implementation of standard and traditional multiplier methods, which are used to create IIR filters, allows for the optimisation of this process in relation to latency, area, LUTs, and logic level. The implementation of IIR filters with orders 4, 8, 16, 32, and 64 is subsequently done using their findings. It is vital to optimise the multiplier's design, a problem on which many earlier studies have focused, as the multiplier's complexity influences the filter's reaction time. These research built digital multipliers for a range of bit lengths.

2. Implementation

The VERILOG codes of all the aforementioned multiplier algorithms are built on an FPGA using Xilinx software with bit widths of 4, 8, 16, 32, 64 to provide information on latency, hardware complexity, LUTs, and IO parameters.

Table 1 presents the analytical report generated subsequent to simulating a algorithm for a certain bit length in VERILOG.

The MATLAB R2021a software is utilised to generate comparative graphs pertaining to latency and memory utilisation characteristics. Figure 1 illustrates the response delay of the algorithms mentioned earlier, while Figure 2 illustrates the memory consumption of these algorithms during the construction of the final product terms.

Figure 2 illustrates a comparison of the memory (KB) demands of various multiplier algorithms on the Virtex 5.

Bit length	Type	Delay in ns	Logic Levels	Number Of slice LUTs	Memory Usage(inKB)
4	Vedic	5.853	6	20	4546656
	Array	5.540	5	26	4546716
	Booth	5.374	5	23	4546628
	Sequential	6.803	8	20	4546704
8	Vedic	10.683	12	117	4546712
	Array	12.046	13	91	4546632
	Booth	15.362	30	192	4546648
	Sequential	13.763	29	94	4546712
16	Vedic	18.290	22	494	4596280
	Array	19.832	25	375	4581196
	Booth	25.533	63	737	4562876
	Sequential	25.657	61	382	4562844
32	Vedic	30.397	38	2121	4831320
	Array	38.120	61	528	4579112
	Booth	45.970	128	3009	4679272
	Sequential	49.431	125	1534	4646968
64	Vedic	52.670	69	8850	5646976
	Array	69.022	125	2079	4693552
	Booth	88.869	256	12161	4887660
	Sequential	96.980	253	6142	5407860

Table 1 Multiplier algorithms that are compressed for various bit lengths

International Journal of Advance Research in Science and Engineering
Volume No. 12, Issue No. 06, June 2023
www.ijarse.com
IJARSE
ISSN 2319 - 8354

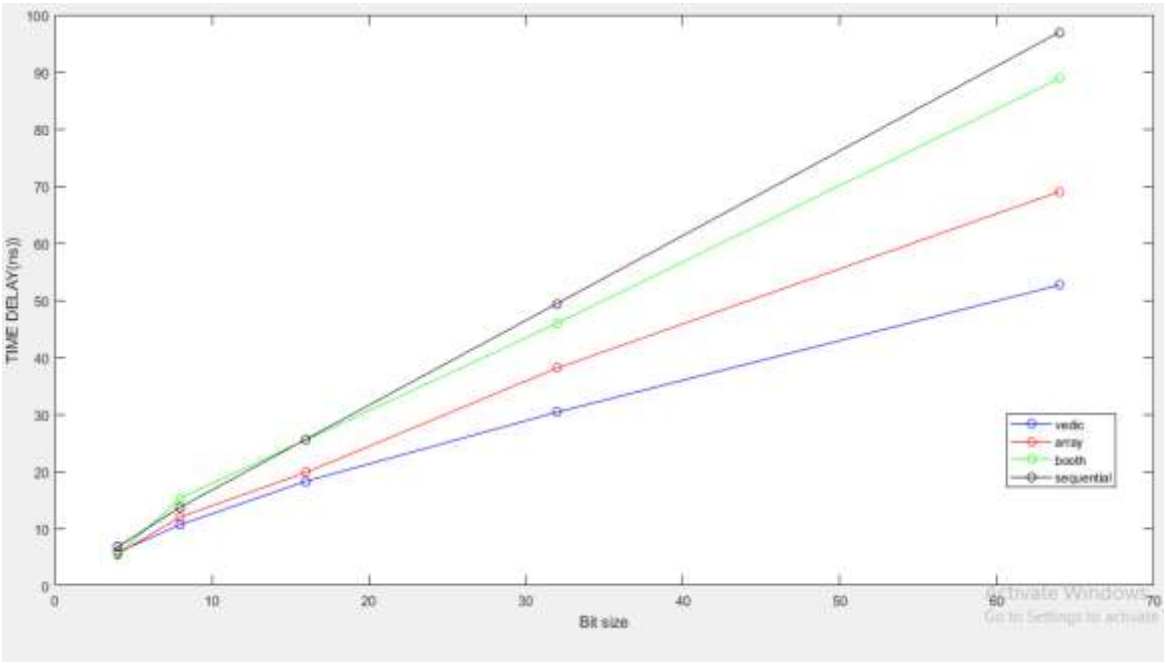

Fig. 1 Graphs of comparative delays for certain multiplier algorithms

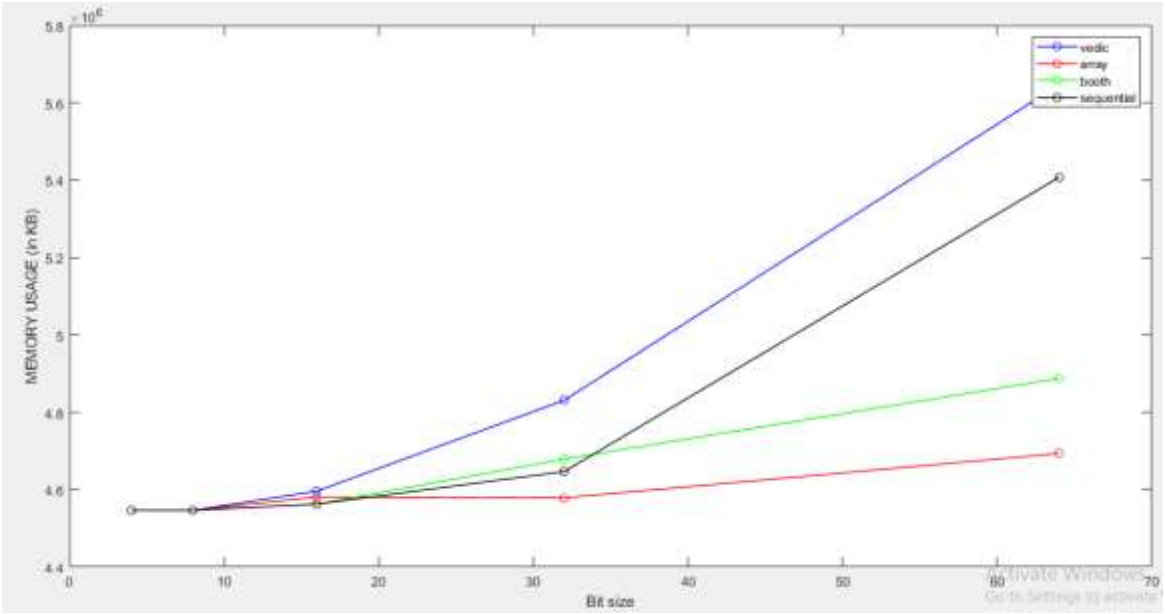

Fig. 2 Comparison graphs of memory use for different multiplier algorithms

In this study, we developed low-pass Infinite Impulse Response (IIR) filters of varying orders, specifically four, eight, sixteen, thirty-two, and sixty-four, using the VERILOG programming language. These filters were subsequently subjected to simulation and implemented on a Field Programmable Gate Array (FPGA) with the aid of XIlinx software. Table 2 presents an analytical report of an Infinite Impulse Response (IIR) filter with regards to temporal delay, hardware intricacy, Look-Up Tables (LUTs), and Input/Output (IO) parameters.

Filter Order	Type	Delay in ns	Logic Levels	Number Of slice LUTs	Memory Usage(inKB)
4	Vedic	24.684	73	1321	4798312
	Array	25.552	45	1465	4680960
	Booth	48.541	132	4327	4643772
	Sequential	31.606	129	952	4579112
8	Vedic	55.107	169	4737	5141960
	Array	57.238	189	3976	4886008
	Booth	100.570	353	8867	4662604
	Sequential	66.153	294	2317	4596288
16	Vedic	103.672	348	8224	5740636
	Array	107.917	350	7825	5235524
	Booth	196.171	677	16724	4781464
	Sequential	116.873	544	4315	4676236
32	Vedic	194.692	688	15203	6963680
	Array	218.001	734	15788	5951104
	Booth	387.845	1420	35146	5066832
	Sequential	234.402	1097	8740	4749764
64	Vedic	482.294	1603	22212	9313464
	Array	462.728	1501	23332	7241756
	Booth	771.717	2856	70942	5574236
	Sequential	464.123	2164	17562	4939484

Table 2 Using the Virtex-5 device, XC5VLX50T-3FF665, a comparison of IIR filters of orders 4, 8, 16, 32, and 64 using Vedic, Array, Booth, sequential, and algorithms.

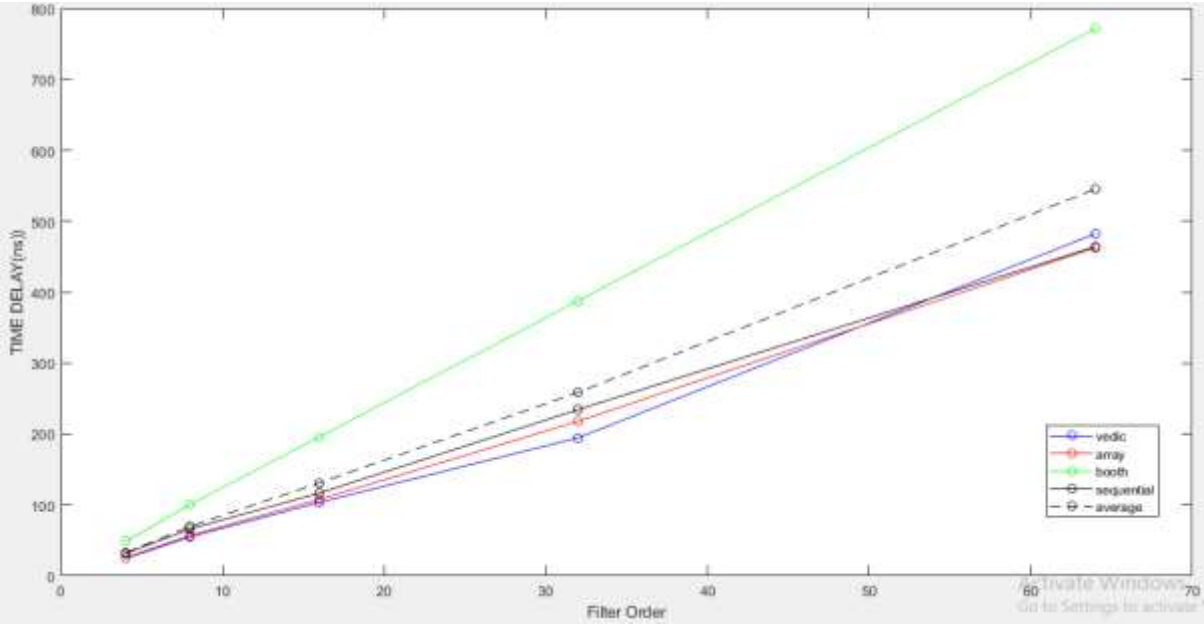

Fig. 3 Graphs of comparative delays for certain multiplier algorithms

The Butterworth methodology is employed for the purpose of designing a direct form low-pass IIR filter, and the coefficients are obtained through the utilisation of filter design and analysis (FDA) tools. The software tool MATLAB R2021a is utilised to generate comparative graphs pertaining to delay and memory utilisation characteristics. Figure 4 illustrates the quantity of memory utilised in the aforementioned filter order to attain the requisite output, while Figure 3 demonstrates the response delay for IIR filters of different orders.

3. Conclusion

Based on the results obtained from the simulation, implementation, and analysis report (Table 1), as well as the comparative multiplier algorithm graphs (Fig. 1 and 2), it can be concluded that the Vedic algorithm exhibits the highest speed for high-bit-sized systems, with a delay of 52.670 ns. The array algorithm follows with a delay of 69.022 ns, while the booth algorithm exhibits a delay of 88.869 ns. Finally, the sequential algorithm displays a

delay that is approximately twice as long as the Vedic algorithm.

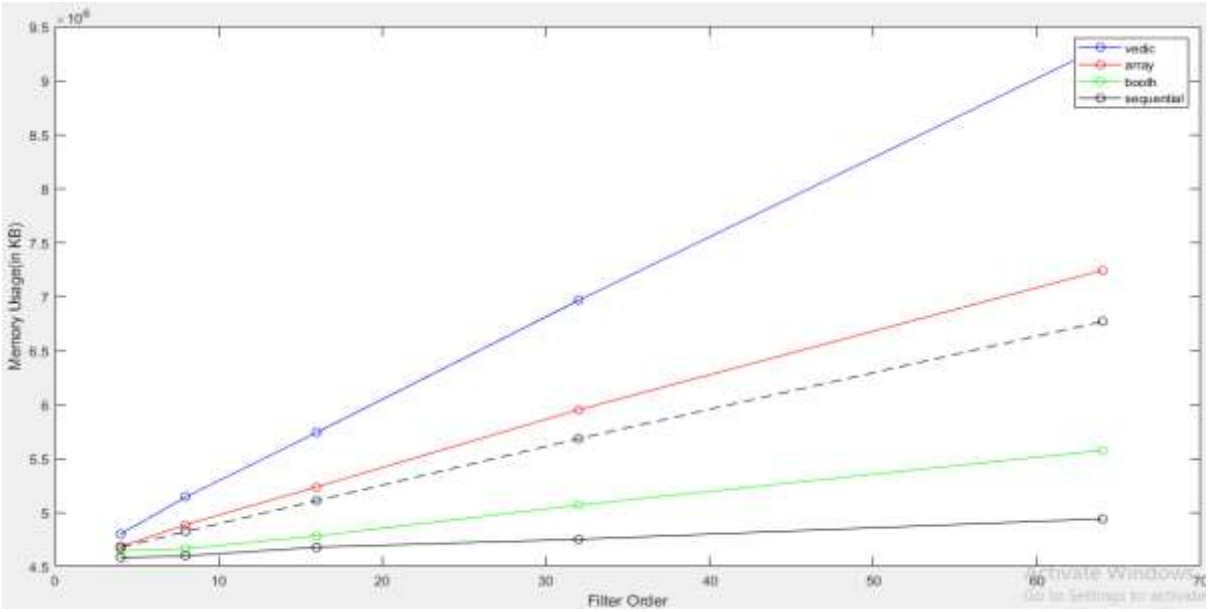

Fig. 5 Comparison graphs of memory use for different multiplier algorithms

The Vedic algorithm has been found to be highly effective as a standalone multiplier. However, when considering the design of IIR digital filters, the use of established multiplier techniques has been shown to yield superior results. Specifically, it has been determined that the Vedic algorithm is optimal for low-pass filter design in relation to delay, as evidenced by the data presented in Tables 1 and 2, as well as Figures 3 and 4. The aforementioned deduction was derived through the examination of solely multiplier algorithms, followed by their implementation in a practical context such as the design of an IIR filter. The Vedic Logic algorithm exhibits superior performance compared to other established multiplier algorithms, as evidenced by its lower mean deviation of time delay. When considering memory consumption and device complexity as primary concerns, sequential multipliers are typically favoured over booth, array, and vedic multipliers.

References

1. S. R. Sutradhar, N. Sayadat, A. Rahman, S. Munira, A. K. M. F. Haque, and S. N. Sakib, “IIR based digital filter design and performance analysis,” 2nd International Conference on Telecommunication and Networks, 2017.
2. B. Garu and thomas.koorakula, "Design and implementation of iir filter by using modified wallace tree multiplier," Proceedings of ASAR International Conference, pp. 54–59, 2017.
3. A. Savadi, R. Yanamshetti, and S. Biradar, “Design and Implementation of 64 Bit IIR Filters Using Vedic Multipliers,” Procedia Computer Science, pp. 790–797, 2016.
4. S. Sarkar, Shubham. Sarkar, and J. Mehedi, “Comprehensive Study for Selection of Proper IIR Filter: Specifications Dependant Approach,” 2018 3rd International Conference on Convergence in Technology,

pp. 1–7, 2018.

5. S. K. Yadav and R. Mehra, "Analysis of Different IIR Filter based on Implementation Cost performance," International journal of engineering and advanced technology, pp. 2249–8958, 2014.
6. A.kumar,Mamta"ComparisionofdifferenttypesofIIRFilters"IJARECE,Vol.5,pp.393-402,2016.
7. R. Arya, "Design IIR Filter using MATLAB,"International Journal of Science Technology and Engineering,Vol.4, pp. 1–9,2015.
8. Marek Cieplucha "High Performance FPGA-based Implementation of a Parallel Multiplier-Accumulator" 20th International Conference on "Mixed Design of Integrated Circuits and Systems", pp. 485-489 June2013.
9. Mariza Wijayanti1, Abdul Hakim2& Sunny Arief Sudiro3 "Designing and Simulation of Band-Pass Infinite Impulse Response Digital Filter using FPGA Devices" International Technology Research Letters, pp.25-31,2012.
10. Arjuna Madanayake· Thushara K.Gunaratne· Leonard T.Bruton "Reducing the Multiplier-Complexity of Massively Parallel Pollyphase 2D IIR Broadband Beam Filters"pp:1231-1243,November2011©Springer.
11. Y.D Singh, S. tripathi and Manoj Pandey, "Analysis of Digital IIR filter ", IJCA, Vol. 10, No. 06, pp.23-30,2010.
12. Ke, Zhang, etal."The application of the IIR filters based on FPGA in the DTV field." On Computer Science-Technology and Applications ,. International Forumon.Vol.3. IEEE ,pp:406-409 2009.
13. Vagner S.Rosa, Fábio F.Daitx, Eduardo Costa, Sergio Bampi,"Design Flow for the Generation of Optimized FIR Filters",ICECS2009.
14. Soo-Chang Pei and Hong-JieHsu, Fractional Bilinear Transform for Analog-to-Digital Conversion, IEEE Transactions on signal processing, Vol.56, No.5, May2008.
15. Fábio Fabian Daitx, Vagner S.Rosa, Eduardo Costa, Paulo Flores, Sérgio Bampi,"VHDL Generation of Optimized FIR Filters",2008 International Conference on Signals, Circuits and Systems.
16. Les Thede,"PracticalAnalogandDigitalFilterDesign",2004,p.141.
17. Vinay K.Ingle,JohnG.Proakis,"DigitalSignalProcessingUsingMATLAB",3e.
18. Sergiyenko A, Serhienko A "Digital flter design using VHDL". In: Fifth international conference high performance computing HPC-UA, pp.123-126,2018.
19. AladinKapić, RijadSarić , Slobodan Lubura, et.al., 2, "FPGA-based Implementation of IIR Filter for Real-Time Noise Reduction in Signal".
20. Debarshi Datta, Himadri Sekhar Dutta," High performance IIR flter implementation on FPGA". Journal of Electrical Systems and Information Technology,pp. 1-9,2021.
21. K. Keshav Sai Chowdary, K. Mourya, S. Ravi Teja, et al., "Design of Efficient 16-bit Vedic Multiplier".International Conference on Signal Processing and Communication, pp. 214-218, 2021.
22. R. Pal, "Comparison of the design of FIR and IIR filters for a given specification and removal of phase distortion from IIR filters".International Conference on Advances in Computing, Communication and Control, 2017.

23. Kaustubh Gaikwad, Mahesh Chavan," Design and Implementation of Digital Butterworth IIR filter using Xilinx System Generator for noise reduction in ECG Signal". Wseas Transactions on Electronics, Vol.8, pp 8-12, 2017.
24. Sushmitha.C, Swathy.R, Veena Devi.S, et.al., Design and Simulation of FIR Filter, International Journal of Innovative Research in Science, Engineering and Technology,Vol.5, pp 241-245, 2016.
25. S. R. Sutradhar, N. Sayadat, A. Rahman, S. Munira, A. K. M. F. Haque, and S. N. Sakib, "IIR based digital filter design and performance analysis," 2nd International Conference on Telecommunication and Networks., 2017.
26. P.Ram Sirisha, A.M.Prasad, "Design and Performance Analysis of 32 bit Array Multiplier using optimized Carry Select Adder".IEEE JOURNAL, 2015.
27. S.Vijaya kumar , J.Sundararajan, P.Kumar and S.Rajkumar, "Low power multiplier using vedic carry look ahead adder". International Conference on Engineering and Technology,pp.1-4,2015.
28. Suganthi Venkatachalam and Seok-Burn Ko, "Design of Power and Area Effcient Approximate Multiplier" .IEEE Transactions on Very Large Scale Integration Systems, pp.1-5,2016.
29. Samiksha Dhole, Sayali Shembalkar,TirupatiYadav and PrasheelThakre,"Design and FPGA Implementation of 4x4Vedic Multiplier using Different Architectures". International Journal of Engineering Research &Technology ,Vol.6,pp.812-816,2017.
30. C. Durgadevi ,M. Renugadevi , C. Sathyasree, et al.," Design of High Speed Vedic Multiplier Using Carry Select Adder".International Journal of Engineering Research & Technology,Vol.5,pp.1-5,2017.
31. K. Nehruand T.T.Linju," Design of 16 Bit Vedic Multiplier Using Semi-Custom and Full Custom Approach". Journal of Engineering Science and Technology Review, pp.221-232,2017.
32. Divya ,K Surya, K Uma Narayani, etal.,"Design of 32 Bit Vedic Multiplier using Carry Look Ahead Adder". Global Research and Development Journal for Engineering, pp.95-99,2018.
33. L Z Shinga, RHussin, A Kamarudin, S N Mohyar, S Taking, M H A Aziz and N Ahmad, "16X16 Fast Signed Multiplier Using Booth and Vedic Architecture".Electronic and Green Materials International Conference, pp.020085(1)-020085(8), 2018.
34. V.Naresh and G.Kalpana,"Design of 64 bit vedic multiplier using carry look ahead adder".Journal of Emerging Technologies and Innovative Research,Vol.7,pp.91-95,2020.
35. K.Keshav Sai Chowdary, K.Mourya,S.Ravi Teja,etal.,"Design of Efficient 16-bit Vedic Multiplier".International Conference on Signal Processing and Communication,pp.214-218,2021.
36. V. Sharma,R.P Sharma,"Design, Implementation & Performance of Vedic Multiplier Based on Look Ahead Carry Adder for Different Bit Lengths".International Journal for Research in Applied Science & Engineering Technology,pp.24-30,2022.