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DESIGN AND PERFORMANCE ANALYSIS OF 32-BIT ADDERS FOR AREA EFFICIENTVLSI APPLICATIONS

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ABSTRACT:

This paper represents the basic process like firstly addition subtraction can be done using various types of binary adders with dissimilar addition times, area consumption in any digital processing application. Parallel prefix adders are considered to be one of the fastest adders that had been designed and developed. Parallel prefix adders were established as the most efficient circuits for binary addition. This paper investigates the performance of three different parallel prefix adders namely Kogge Stone Adder(KSA), Brent Kung Adder(BKA) and Ladner Fischer Adder(LFA). In this paper the key contribution is the information about the structure of the parallel prefix adders. All the simulations and synthesis results can be noted using Xilinx ISE 14.2i tool.

Keywords: Parallel Prefix Adders, Kogge Stone Adder(KSA), Ladner Fischer Adder(LFA), Brent Kung Adder(BKA), Carry look ahead adder, carry generation stage.

I.INTRODUCTION

Generally, the basic process such as addition, subtraction, division that can be done by using different types of binary adders in any digital based processors and control systems. The adder performance is used in the device is only measured the high speed and accuracy of the system. Previously the processors are used 32- bit carry adders like Ripple carry Adder(RCA), Carry Propagate Adder(CPA), and Carry Look ahead Adder(CLA) with different delay and area consumption.

How fast the carry reaches for every single bit position, from which the delay of any binary adder is calculated. But the above existing 32-bit basic carry adders having a delay value in higher order bits because each level of adder has to wait for the previous carry result. Due to the above problem of 32-bit basics existing carry adders, in today's world of technology, PPA is well suitable designed adder for high speed addition process with less delay in VLSI technology.

PPA is one of the most popular designs and provides good negotiation amongst area and delay. The low order PPA is designed at earlier like 8-bit and 16-bit. This paper consisting of three additions first addition: describes briefly about PPA, in second addition: explain the design of 32-bit proposed parallel prefix(Kogge Stone Adder, Brent Kung Adder, Ladner Fischer Adder), and in third addition it express the simulation results(waveform and reports) of 32-bit PPA which we have designed in the previous section with the performance aspects(delay and area). The last section is concluded that Kogge Stone Adder performance is the best among the other adders with low area and less delay from the analyzed results of 32-bit PPA

1. Parallel Prefix Adder

Now a days, to avoid the higher delay problem of existing carry adders the PPA isused which is simply the modified design form of CLA. The Prefix adders can be designed in many different ways based on the different requirements and the production of carries[6]. Recently, use the tree structure form of adder storaise the speed of addition function in any kind of processors. PPA are fastest adders with tree structure based and used for high performance arithmetic processes in successive industries and DSP laboratories [7].

The PPA's are also called as logarithmic delay adders because the delay value is established using logarithmic functions [8]. Addition in PPA can be processed using three main actions such as Pre-computation (P and G signal generation), Prefix- computation (carry signals group generation), Post-computation (Sum signal generation) [9].

1.1. Pre–Computation

In the pre-processing stage, propagate functions and generate functions are calculated depends up on the given input signals[10].The propagate functions are carried out by the equation (1).

$$P[j]=X[j] \oplus Y[j] \quad (1)$$

ItisstatedthatXandYaretheinputsignalsthatcomposedby XOR logic gate. The generate functions are carried out by the equation(2).

$$G[j]=X[j] \bullet B[j] \quad (2)$$

ItisstatedthatXandYaretheinputsignalsthatcomposedby ANDlogicgate.Sincetheaboveequations(1)and(2)aredonein parallel, it does not increasing a significant calculation of areaconsumption and delay fully depends upon the bit size which isdesired at the input [11].

1.2. Prefix– Computation

This prefix computation stage, calculates the carry signalgroupsdirectly,whichusestheinputandvalueswhichmeasured from the first stage. Carry signals generation uses the more than twoinputs for which the delay is automatically increased in this process[12].Thecarrypropagationfunctionandcarrygeneration function [13] is measured by the equations (3) and (4).

$$\text{Carry } P = P[j] \bullet P[j+1] \quad (3)$$

$$\text{Carry} G=(G[j] \bullet P[j+1])+G[j+1] \quad (4)$$

1.3. Post–Computation

In this stage, the sum result is generated by an Ex-OR operation thatusesthevaluesofcarrygenerationstage(prefix-computation). The last sum operation is calculated by the equation (5)

$$S[j+1]=P[j+1]\oplus C[j] \quad (5)$$

Where Cisthe last carry signal and Pisthe propagate function [14].

2. Designandanalysisofproposed32bitvariousPPA

To over come high delay problem of existing carry adders this work proposed the design of 32-bit various PPA for less delay and low power VLSI applications. This proposed system consists of two modules: The first module is to design of 32 bit PPA like KSA, BKA, and LFA. These condmodule is to analyses the performance comparison of PPA on the basis of area, delay and power.

In this section, analyse the different technologies of adders to design in the form of parallel prefix, apart from the RCA topology, such as Kogge-Stone, Brent-Kung, and Ladner-Fisher PPA. The important aim is to examine the trade-off between area consumption delay and power consumption in the particular PPA depends up on the design performance. All the designs are using a power gating technique to reduce the power consumption [15].

2.1. KoggeStoneAdder(KSA)

Normally, the KSA attains the key role with fast addition operation and it reflects like prefix form of Carry Look ahead Adder (CLA). Also this type of PPA entirely decreases the delay time in design to generate the carry signals [16]. Henceforth this KSA is popularly used in DSP (Digital Signal Processing) laboratory and Control system industries for fast arithmetic function.

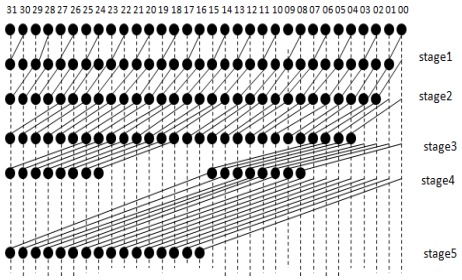


Figure1:32bitKoggeStoneAdderdesign

The structure of 32-bit KSA design is exposed in Figure 1.This design can be divided into 5 stages [17]. The calculation ofPropagateandGeneratesignalsusingfulladderswithcarryinput thatprocessincludedinfirstandsecondstage.Thegenerationof carry signals which used the values of Propagate and Generatethatprocessincludedinthirdandfourthstage.Thecalculationof sumbits based on the P and carry generation values that isincludedinthefifthstage[18].This32bitdesignofKSAiscoded byVHDLand viewed the test bench waveformand analyzed theperformance and noted the results.

2.2. BrentKungAdder (BKA)

The BKA calculates the prefixes based on the bit groups.

Initiallycalculatetheprefixesvaluesfor2bitgroups.These2bit prefixvaluesareusedtofindtheprefixvaluesforthe4bitgroups, thatareusedtocalculatetheprefixvaluesfor8bitgroupsandso on[19].Then these prefixes values are used to measure the carry outof the particular bit stage. These carries will be used along withthe Group Propagate of the next stage to calculate the Sumbit ofthat stage[20].Brent Kung Tree will be using(2log2N- 1) stagesfor any bit design.

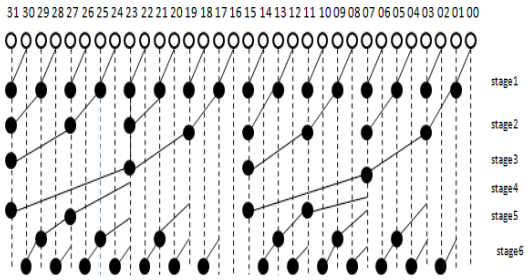


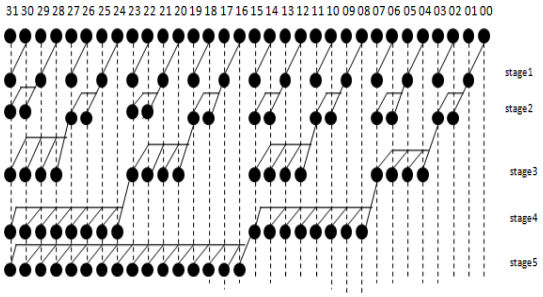
Figure2:32bitBrentKungAdderdesign

Thestructureof32-bitBKAdesignisgiveninFigure2.

Hence the designing of 32- bit adder takes the number of stageswillbe9.Thefan-outforeverybitstageislimitedto2.Theabove diagram shows the fan out being reduced and the loading on theadvance stages being reduced [21]. This 32 bit design of BKA iscoded by VHDL and viewed the test bench waveform andanalysed the performance and noted the results.

2.3. LadnerFischerAdder(LFA)

The LFA tree structures are a family of tree networks betweenBrentKungandSklanskytree.Itisveryclose like to Sklansky PPA, but it calculates the prefix values for odd numberbitsafterthatagainusesanotherstagewhichrippleinto



theevenlocations[22].Athigherorderbits,togetimprovedin speedsthe cells must still be properly sized or grouped.

Figure3:32bitLadnerFischerAdderdesign

Thestructureof32-bitLFAdesignisexposedinFigure3.The Ladner Fischer adder is used for high performance arithmetic operation with complicate designs. The LFA consists of black cellsand gray cells with 5 stages for 32 bit design. Each black cell enclosesonlyoneORlogicgateandtwo ANDlogicgates.EachgraycellcontainsonlyoneANDlogicgate[23].This32bitdesign ofLFA is coded by VHDL and viewed the test bench waveformand analysed the performance and noted the results.

3. Simulationresultsofproposed32bitPPA

Inthissimulationsection,tookallthreetypesof32bitparallel prefix adders (KS, BK, LF) that are discussed above. All the PPA'sare designed on VHDL (Very high speed Hardware DescriptionLanguage) / Verilog project navigator 14.2i is used for synthesis (Xilinx version) [24]. Simulationresultsare verified onthe basisofarea,poweranddelay.Inadditiontothatthewaveformsandthe comparison results for all three parallel prefix adders are given.

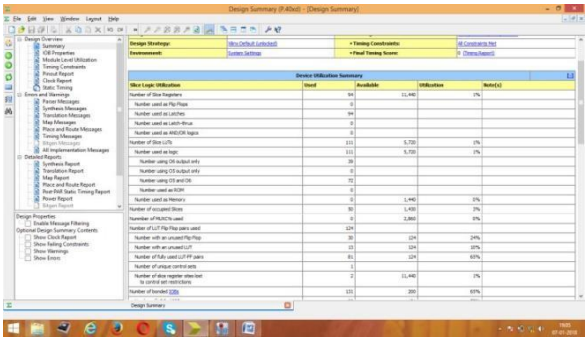


Figure4:AreaConsumptionreportfor KSA

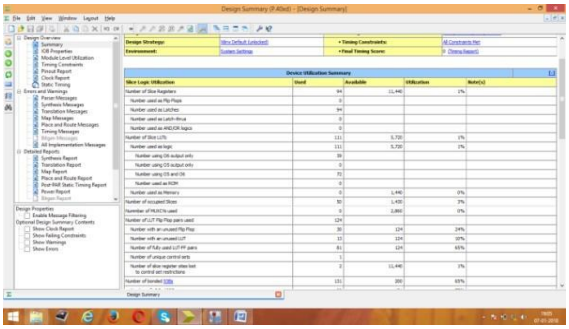


Figure5:PowerAnalyzerreportforKSA

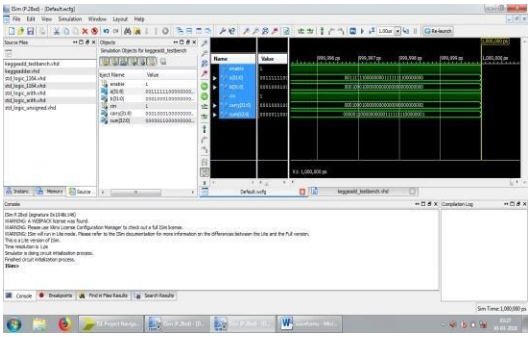


Figure6:TestbenchwaveformresultsofKSA

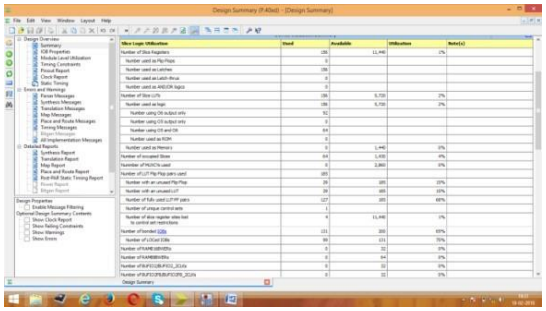


Figure7:AreaConsumptionreportforBKA

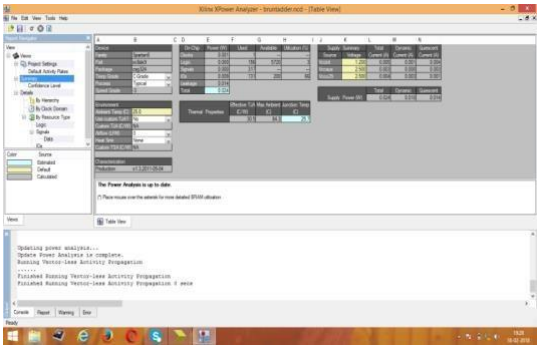


Figure8:PowerAnalyzerreportforKSA

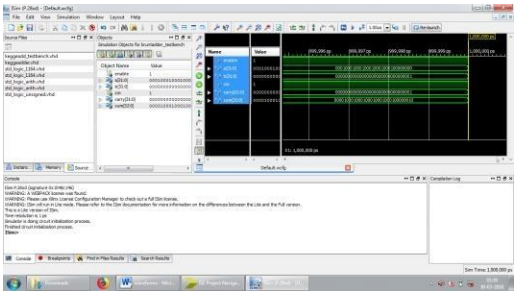


Figure9:TestbenchwaveformresultsofBKA

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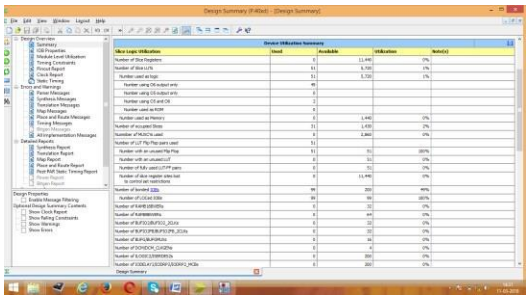

Figure10:AreaConsumptionreportforLFA

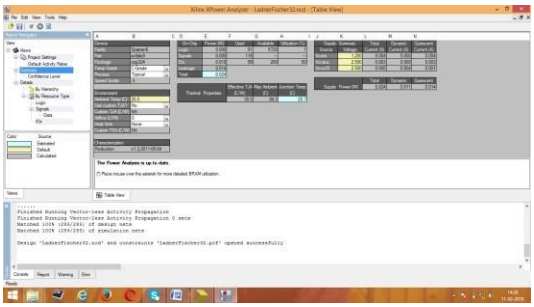

Figure11:PowerAnalyzerreportforKSA

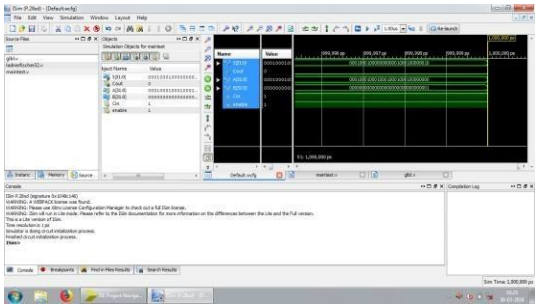

Figure12:Testbenchwaveformresultsof LFA

Area consumption, power analysis, and the test bench waveform of KSA are shown in figures 4, 5, and 6 respectively. Area consumption, power analysis, and the test bench waveform of BKA are shown in figures 7,8,and 9 respectively. Also the area consumption, power analysis, and thetest bench waveform of LFA are shown in figures 10, 11, and 12respectively.

From the above figures, the comparison results of all three PPA on the aspects of area, delay and power is given in table I. From the analysis, LFA is better due to the less area consumption butthe power utilization is more compared to other adders. Normally PPA's have less delay in any processors while doing addition.

Accordancewithlowpowerapplication,KSAismoresuitabledue toless power utilization in any digital based processors.

Table1:Comparisonresultsofarea,delayandpowerforvarioustypesofPPA

AdderTypes	LUT's Used	Delay(ns)	Power (mW)
KoggeStoneAdder	189	6.483	21
BrentkungAdder	156	6.489	24
LadnerFischerAdder	51	21.879	24

Conclusion

In this paper, an efficient 32 bit Parallel Prefix adders like KSA, BKA, LFA is designed. This proposed 32 bit adder addition operation offers a great advantage in reducing delay. For low power VLSI applications, also the designed adders are comparedon the basis of power, area consumption, and delay. The synthesis results reveal that among the proposed adders, KSA is achieved some saving of power-delay product due to less power utilization. But the area delay product is little increased, compared to other adders due to high area consumption. For decreasing the complexity at all performance aspects, further optimization techniques can be achieved on the performanceparameters that will be the future work of the paper.

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