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ENERGY EFFICIENT APPROXIMATE MULTIPLIER

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Abstract:
In Digital Signal Processors and Microprocessors, Multipliers play an important role in performing the arithmetic operations. Exact computing units are not always necessary in applications like data mining, multimedia signal and image processing. Approximate computing decrease power consumption of inherently error tolerant application which trades off accuracy to certain extent for efficiency. A new design approach for approximation in multipliers is proposed. Approximate computing unit reduces the design complexity. This paper presents the design of Approximate Dadda Multiplier (ADM) architecture and its implementation in a digital image processing application. ADM for n=16, ADM with Altered Partial Products (ADMAPP) for n=12 and ADM with only Approximate Adders (ADMA) for n=12 are proposed. The proposed and state of art designs are structured using Verilog HDL and synthesized using Cadence Encounter with 90 nm ASIC technology. Power saving of 6.22%,71%,72%, area reduction of 3.7%, 54.1%, 51.7%, and delay reduction of 4.1%, 35.9%, 38.9%, are obtained in ADM 16 bits, ADMAPP 12 bits and ADMAA 12 bits respectively, compared to 16 bits Exact Dadda Multiplier (EDM). Hence ADMAA 12 bits possess low power consumption and delay with high accuracy compared to other two architectures, so it can be considered as the energy efficient approximate multiplier for Mean Filter algorithm.

Key words: *Dadda Multiplier, approximate adder, compressor, Image processing.*

1. INTRODUCTION

In this Digital era Multiplication and squaring functions are very important arithmetic operations. They play an important role in the implementation of many Digital Signal Processing, Digital Image Processing and Multimedia algorithms. The architectures of

multiplication and squaring circuits decides the size and power consumption of DSP chip. This demands the need to have a multiplication and squaring function that is fast enough, occupying less area on the chip and consuming less power.

Many applications require less precision than offered by the existing hardware. Approximate computing decrease power consumption of inherently error tolerant application which trades off accuracy for efficiency. Approximation is introduced only in non-critical data. In multi-media applications, when interpreting an image or a sound or a video, human beings possess perceptual capabilities to accept approximated outputs. In serial-parallel multiplier [1] design the contents of the product register are shifted right by one position and the multiplicand is added to the contents occupying smaller area. In Parallel multipliers AND array structure is used to generate the partial product terms and the final result is obtained by adding the partial product terms over each column [2, 3]. In Full Width Multiplier the AND gates are used to generate the partial product terms and the HALF and FULL ADDERS applied to perform the column wise sum of the partial product terms results in large number of transistors, leading to large area and power consumption.

A fixed width multiplier occupies smaller silicon area due to truncation of Least Significant Bits. The first approach involves truncating the least significant N-bits out of 2N-bits.This design offers the best results of the fixed-width multiplier designs. Since this design retains the entire columns of the partial product array the area saving is minimal. The next design involves generating a result with N-1 bits wide by truncating the least significant N-columns of the partial product matrix of a full-width multiplier This design results in massive savings in area but the errors introduced due to truncation are high. Design of fixed-width multiplier is always a compromise between area saving and error.

2. LITERATURE REVIEW

Fixed-width multipliers are obtained by omitting half the adder cells of parallel multiplier. This approach results in area reduction but intolerable error not acceptable even for DSP applications. Inexact computing is the most useful technology for digital processing at nano metric scales. To reduce the truncation error Kidambi et al. [4] added a constant bias to the retained cells of the fixed-width multipliers. Based on the correction term the design is altered to replace the half adders with full adders wherever needed. This strategy is also used

to design reduced width multipliers. The main disadvantage of this design is the correction bias added to offset the error in the process of truncation. The correction term added is a constant term and does not depend on the multiplier inputs. To compensate this truncation error a binary compensation vector circuit is introduced in [5]. To overcome the hardware overhead the compensation structure is implemented in array and Booth multiplier. Compensation bias is derived using the generalized index of the two n bits inputs [6].This reduces the truncation error for an n bits product. This type of area efficient structure is used in digital FIR filter applications.

Low-error carry-free fixed-width multipliers with Low-Cost Compensation Circuits [7,8] design results with low truncation errors, small area with very simple compensation circuits of low cost. Pre-truncation technique is applied in [9] for the partial product array. The resulting array is further truncated to generate an output that is N bits wide for N bits input data size. This flexible design results in varying order of area savings by varying the input bits truncation. By slightly modifying the partial product matrix of Booth multiplication [10] the truncation error is further reduced. The mean and mean-square errors are reduced much due to the compensation circuit proposed with sorting network. In image processing applications it improve the average PSNR of output images.

To overcome long latency, large area and power faced by multipliers compressors are designed with reduced stages of products. In the design of inexact parallel multipliers compressors are used. A 4-2 compressor utilizes different features of compression. The proposed four different designs [11] results with significant reductions in power dissipation, delay and transistor count compared to an exact design.Inexact multiplication circuits are designed using partial product perforation [12] technique. The imposed errors are bounded and predictable, which depends on the input distribution. The partial product perforation delivers reductions in power, area and critical delay compared with the respective exact design.

An n-bits unsigned truncated sequential multiplier that compensate for the truncation error with improved accuracy is designed [13] using the $(n-1)^{th}$ or n^{th} columns of the partial product matrix dynamically. To compensate for the error due to the removal of the carry bits of the least significant parts of the partial product matrix a small circuit is incorporated with original sequential multiplier.

A high speed and energy efficient approximate multiplier is proposed in [14] by Reza et al. At the cost of a small error the computational intensive part of the multiplication is omitted improving speed and energy consumption. In the approximation of multipliers, the resultant partial products of the multiplier are produced using generate and propagate signal. For the reduction of partial products approximate half-adder, approximate full-adder, and 4-2 compressor are recommended. For zero valued inputs non-zero outputs are obtained in [15]. The modified compressor design in [16] rectifies this issue and resulting with good image quality and power, area optimized.

The rest of the paper is organized as follows, section 2 deals with literature survey regarding existing approximate multipliers. Section 3 deals with existing approximate 16 bits Dadda multiplier. Section 4 deals with proposed approximate 12 bits Dadda multipliers. Section 5 deals with the simulation outputs and results and section 6 deals with the conclusion.

3. EXISTING ADM (ADM 16 bits)

The 16 bits approximate multiplier is designed using the Dadda Architecture [17]. The Dadda architecture is the simplest and efficient architecture in partial product reduction. The approximate 16 bits DM can be constructed using four 8 bits approximate DM as shown in the Figure 1. The 8 bits multiplier shown here is the approximate 8 bits Dadda multiplier. The adders used here are 24 bits carry select adder and 16 bits ripple carry adder.

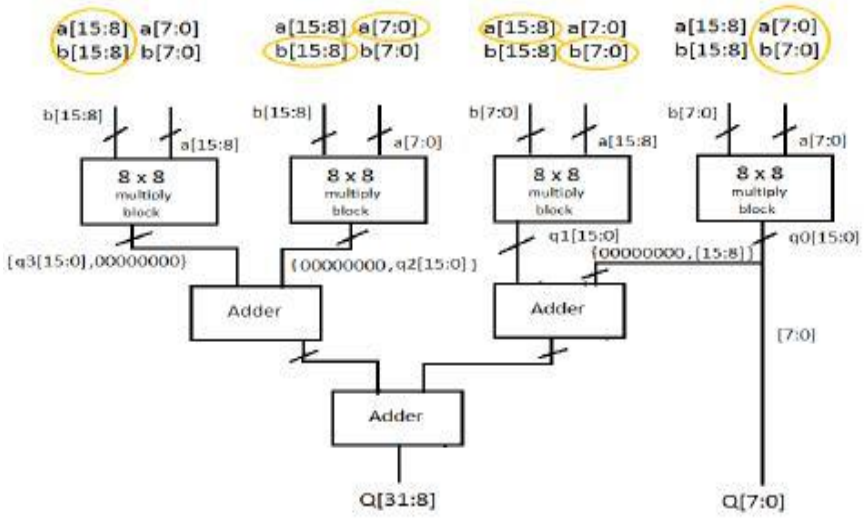

Figure1. Approximate 16-Bits Dadda Multiplier using Approximate 8-Bits Dadda Multiplier

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4. PROPOSED APPROXIMATE DADDA MULTIPLIERS

4.1 Proposed Approximate DM with Altered Partial Products (ADMAPP 12 bits)

In the proposed parallel multiplier, partial product generation is carried out in parallel dividing the inputs in to subgroups. For example, n bit inputs A and B are split in to A_{msb}, A_{lsb} and B_{msb}, B_{lsb}. The multiplication operation is carried out in parallel as shown in the Figure 2.

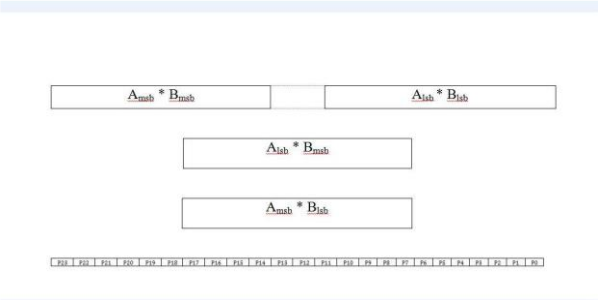

Figure 2. Parallel multiplication operation

Here for the proposed DM A and B is of 6 bits. Four 6 bits multiplier are used to construct 12 bits output. Based on the above concept an approximate 12-bits DM has been designed in the same flow as that of 16 bits ADM. The Original partial products can be generated by giving the two input bits to the AND gates. Then the partial products can be arranged in a symmetric manner such that the reduction of partial products becomes easy. Then the original partial products are altered using propagate and generate terms and then approximate adders are used as in approximate 16 bits DM to reduce the partial products [17]. The arrangement of partial products and the reduction of partial products for 6 bits Dadda architecture is given in Figure 3.

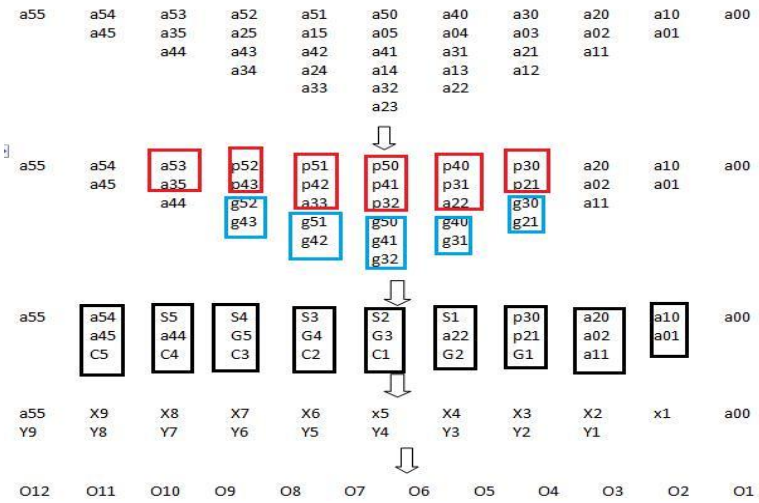

Figure 3.Approximate 6-BitsDaddaArchitecture Using Altered Partial Products

Mean= (a1+a2+a3+a4+a5+a6+a7+a8+a9)*(1/9)

The result of s= (a1+a2+a3+a4+a5+a6+a7+a8+a9) is 12 bits. So (1/9) is also represented in 12 bits.1/9=0.111111….in decimal and 1/9=0.000111000111…. in binary.

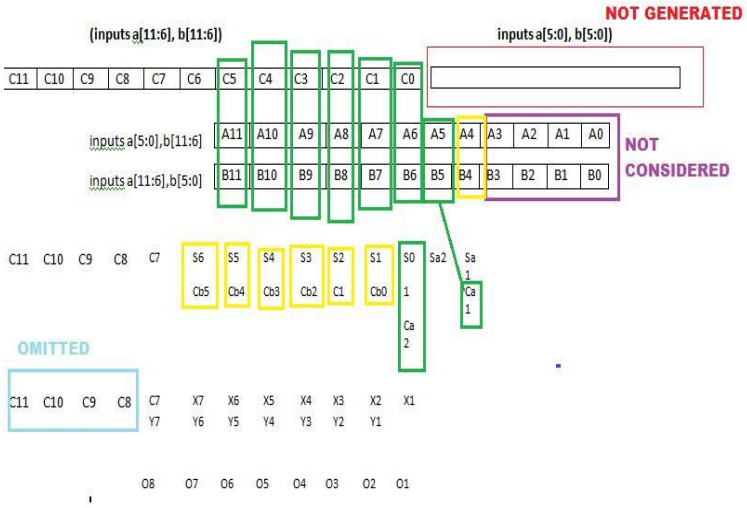

Figure 4. Approximate 12-Bits Dadda Architecture with Truncated Vedic Operation

But only the values after decimal point is considered 000111000111->455. Mean=s*455.When two 12 bits inputs are multiplied to get 24 bits output. Since the 12 bits only are to be considered after decimal point for (1/9), so only the 12 bits in MSB are considered. The DM (n=12) with truncation is shown in the Figure 4. Finally, only 8 bits from the 12 bits MSB of the output of 12 bits multiplier is considered since 8 bits is enough for representing the 8 bits per pixel image.

4.2 ADM with Approximate Adders (ADMAA 12 bits)

Energy efficient Approximate DM for n=12 is proposed similar to Approximate 12 bit DM except that the propagate and generate terms are eliminated and instead approximate adders are used with the original partial products. Though the area of the architecture increases, the delay, power and error percentage is lesser than the approximate 6 bits Dadda architecture. The arrangement of partial products and the reduction of partial products for 6 bits Dadda architecture with approximate adders is given in Figure 5.

An approximate Half Adder (HA) is designed using OR gate with logical expression as given by equation (1) which introduces one error in sum, and carry by equation (2).

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$$Sum = x1 + x2 \qquad (1)$$

$$Carry = x1 \cdot x2. \qquad (2)$$

An approximate Full Adder (FA) is designed using one OR gate and one XOR gate with logical expression as given by equation (3) which introduces two errors in sum, and carry with logical expression as given by equation (4) which introduces one error in carry.

$$Sum = (x1 + x2) \oplus x3 \qquad (3)$$

$$Carry = (x1 + x2) \cdot x3. \qquad (4)$$

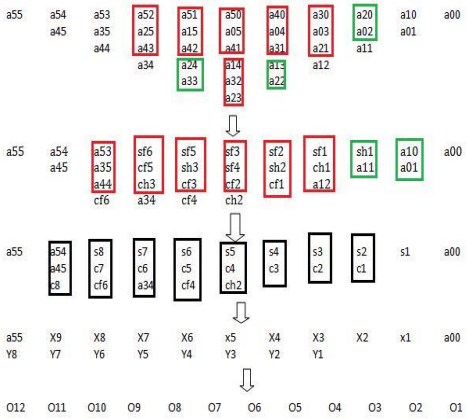

Figure 5. Approximate 6-Bits Dadda Architecture Using Approximate Adders

Efficient 12 bits approximate Dadda architecture is constructed with the approximate 6 bits Dadda architecture using only approximate adders. Figure 6 depicts its architecture. Here, the LSB bits are not generated, since the MSB bits are enough. This concept of truncation eliminates the need for larger area, power and delay.

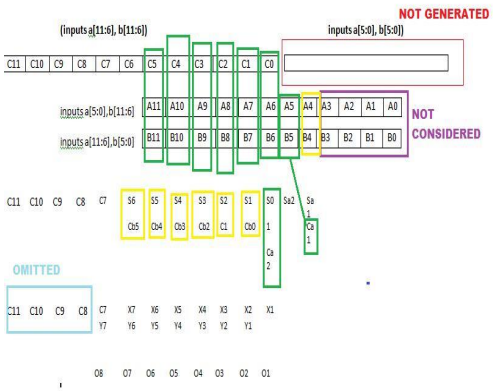

Figure 6. Approximate12-Bits Dadda Architecture with Truncated Vedic Operation

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5. SIMULATION RESULTS

The 16-bits approximate DM and the 12 bits approximate DMs are designed using Xilinx ISE Design Suite 14.7 simulator and implemented in image processing applications using System Generator in MATLAB.

The simulation outputs of mean filter implemented with Exact Dadda (n=16), approximate Dadda (n=16), approximate Dadda (n=12) are shown in the Figure 7 to 10.

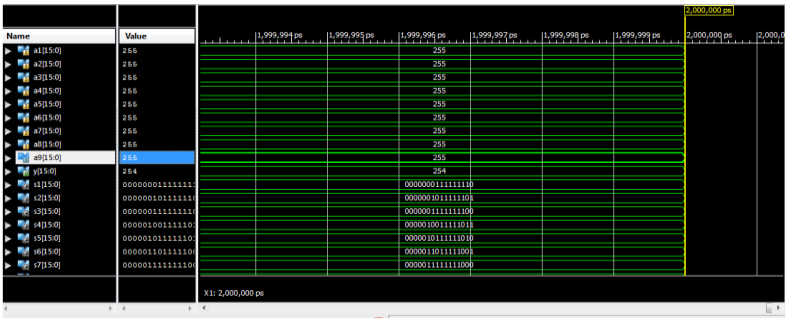

Figure 7. Simulation Results for Mean Filter with Exact DM(n=16)

When all nine inputs are 255 in Mean Filter with Exact Dadda multiplier(n=16), the output is 254. The error here is because of the division(1/9=0.1111, the value cannot be round off).

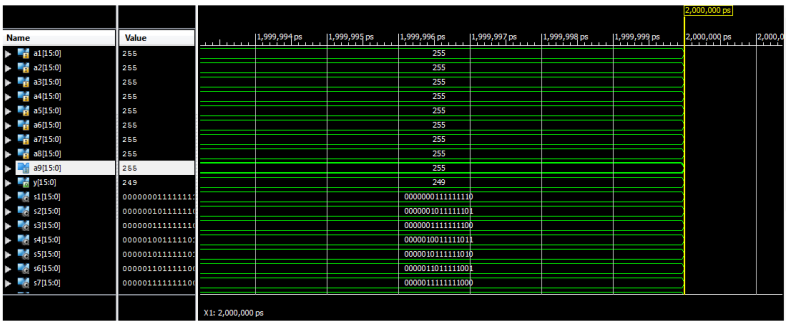

Figure 8. Simulation Results for Mean Filter with Approximate DM(n=16)

When all nine inputs are 255 in Mean Filter with approximate Dadda multiplier(n=16), the output is 249. The error difference is 6 and the error percentage here is 2.3.

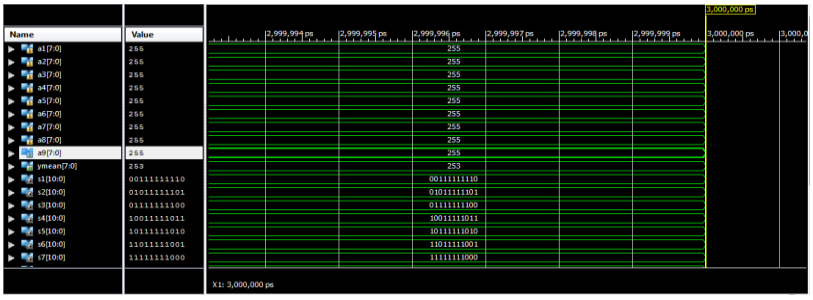

Figure 9. Simulation Results for Mean Filter with Approximate DMfor n=12 (With Altered Partial Products)

When all nine inputs are 255 in Mean Filter with approximate DMfor n=12 (with altered partial products), the output is 253. The accuracy is 99.2%. The error difference is 2 and the error percentage here is 0.8. The error is low when compared to the approximate Dadda multiplier (n=16) When all nine inputs are 255 in Mean Filter with approximate DM for n=12 (with only approximate adders), the output is 254. The accuracy is 99.6%.

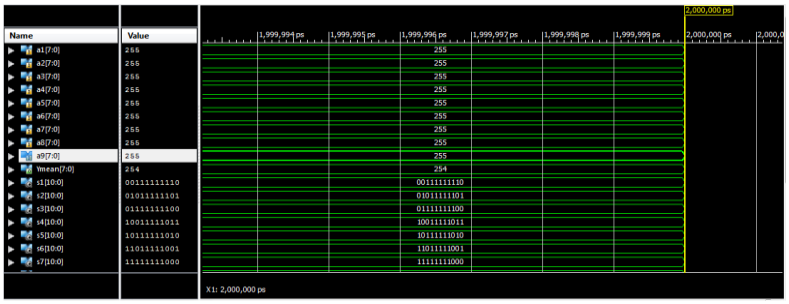

Figure 10. Simulation Results for Mean Filter with Approximate DMfor n=12 (With only Approximate Adders)

The error difference is 1 and the error percentage here is 0.34. The error is low when compared to the approximate Dadda multiplier (n=16) and approximate DM for n=12(with altered partial products).

6. PERFORMANCE ANALYSIS

The following multipliers are used in the Mean Filter with 8 bits per pixel image as input and their performances are compared interms of area, delay and power.

Exact 16 bits DM for n=16 (EDM 16 bits), ADM for n=16 (ADM 16 bits), ADM with Altered Partial Products for n=12 (ADMAPP 12 bits) and ADM with only Approximate Adders for n=12 (ADMAA 12 bits).

6.1 Images Processed by Mean Filter

To determine the novelty of the proposed multiplier designs in error tolerant applications and verify its driving capability, an implementation in processing applications viz., mean filtering is done in FPGA platform. The Verilog HDL model of the proposed and std designs used for comparison are synthesized using Xilinx ISE 14.2 tool and hardware for application system is prototyped on Spartan 6 FPGA (XC6XLX45-CSG324 device).Input images are fed from MATLAB environment to the hardware on FPGA using Xilinx-MATLAB co-simulation with System Generator tool. The mean square error (MSE) and Peak Signal to Noise Ratio (PSNR) are the two error metrics used to compare the image quality. These two metrics are

analyzed with different DM architecture and their performance is compared. PSNR measures the maximum possible power of an image with respect to the unwanted image message caused due to approximation, compression and truncation. PSNR depends on MSE. If K is the processed output image for an accurate image I, then MSE is given by the equation (1) and PSNR by equation (2).

$$MSE = 1/mn \sum_{i=0}^{m-1} \sum_{j=0}^{n-1} [I(i,j) - K(i,j)]^2 \quad (1)$$

$$PSNR = 20 \log \left(\frac{MAXi}{\sqrt{MSE}}\right) \quad (2)$$

Here $MAXi$ is the maximum probable pixel value in the image. It is observed from Figure 11 that MSE of ADMAA 12 bits is lesser than ADM 16 bits and ADMAPP 12 bits.

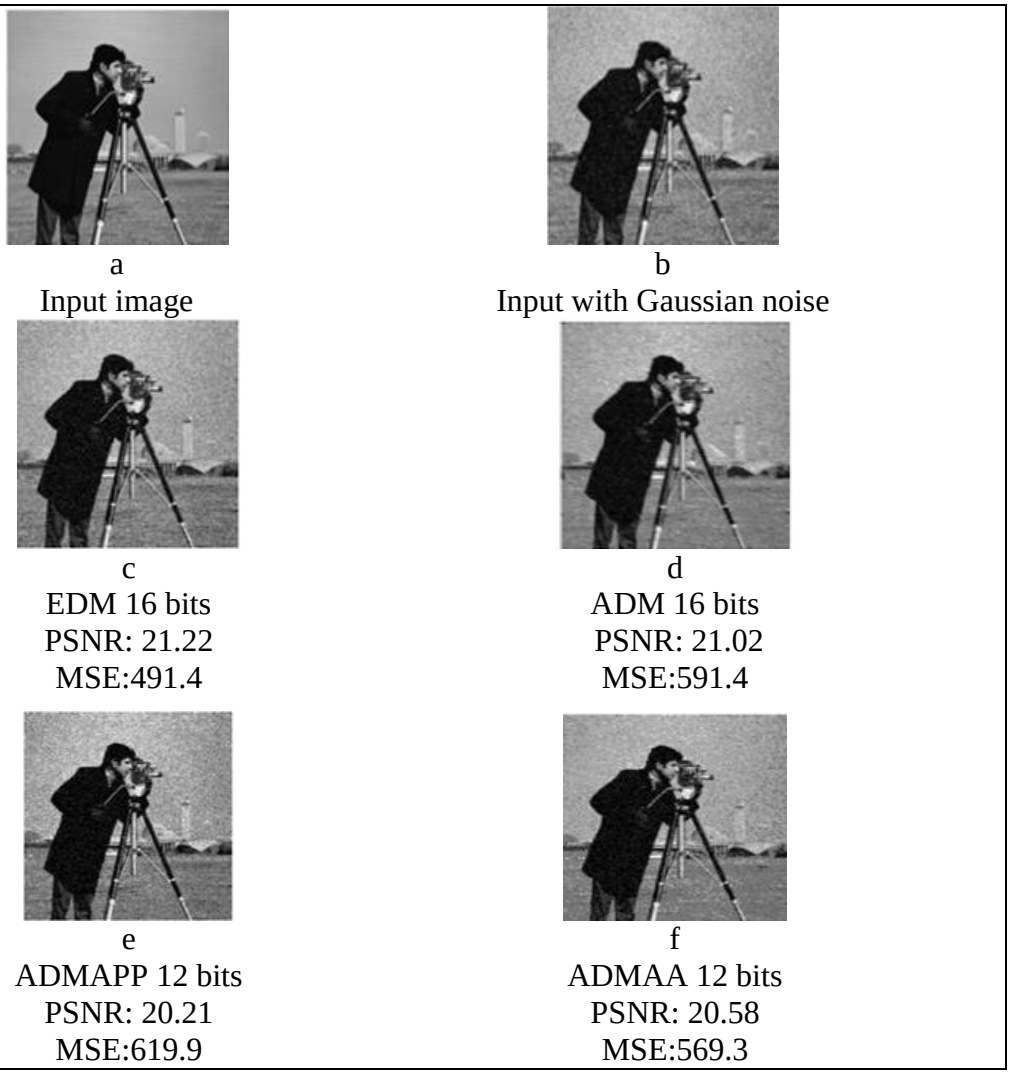

Figure 11.(a) input image (b) Input image with Gaussian noise (c-f) Reconstructed images (c) EDM 16bits (d)ADM 16 bits (e) ADMAPP 12 bits (f) ADMAA 12 bits.

6.2 Power, Area, Delay Estimation

The proposed multiplier designs and state-of the art similar Design[15]are designed using structural Verilog HDL code and synthesized using Cadence Encounter with 90 nm technology in ASIC platform. Performance measure in terms of area, delay, power dissipation in terms of power and power-delay product (PDP) of the proposed and std design are shown in Table 1.

Table 1 Power, Delay Estimation for Mean Filter with Different Dadda Architecture

Mean Filter with	DELAYps	POWER nW	AREAum^2	PDP 10^{-5}j
EDM 16 bits	20848	1485722.290	7154	3.0
ADM 16 bits	19980	1393187.873	6890	2.7
ADMAPP 12 bits	13344	424527.167	3287	0.62
ADMAA 12 bits	12740	414749.649	3455	0.515

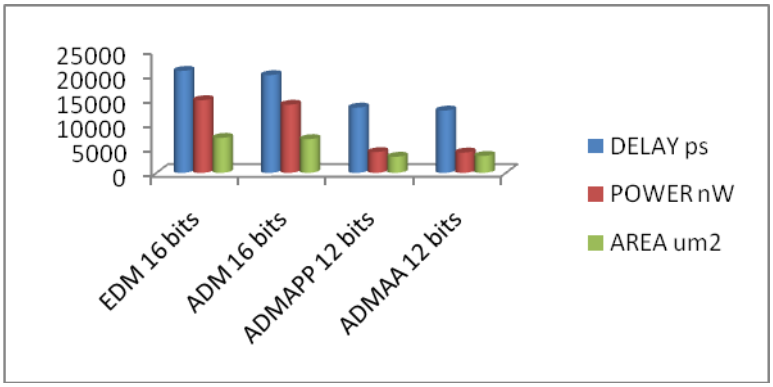

Figure 12. Performance comparisons of existing and proposed DM designs

It is observed from the Table1 and figure 12, that power saving of 6.22%,71%,72%, area reduction of 3.7%, 54.1%, 51.7% and delay reduction of 4.1%, 35.9%, 38.9%, ADM 16 bits, ADMAPP 12 bits, ADMAA 12 bits respectively, results compared to EDM 16 bits. Hence the approximate DM with approximate adders for n=12 is considered to be an energy efficient multiplier.

7. CONCLUSION

Applications that are compute-intensive and error tolerant are most suitable to adopt approximation strategies. This includes digital signal processing, image processing, data

mining, machine learning or search algorithms. One such application in image processing is Mean Filter algorithm. So with the three different Dadda architecture designed, the 12 bits approximate DM with only approximate adders has low power consumption and delay with high accuracy compared to other two architectures, so it can be considered as the energy efficient approximate multiplier for Mean Filter algorithm.

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