

DESIGN AND ANALYSIS OF DIGITAL AUTOMATIC GAIN CONTROL FOR BLUETOOTH LOW ENERGY RECEIVERS

Anushree B¹, Apoorva Mohanta², Chaithra K. S³,

S. Chaitra⁴, Bharath H. P⁵

^{1,2,3,4,5}School of ECE, REVA University, (India).

ABSTRACT

Design and analysis of a coarse tuned Feed Forward Digital Automatic Gain Control (FF-DAGC) with wider dynamic range and lesser attack time for Bluetooth Low Energy (BLE) Receiver is demonstrated in this work. DAGC controls the gain of Variable Gain Amplifier (VGA) through digital control signals. This ensures to prohibit the deviation of Analog signal through the Analog to Digital converter (ADC) from its efficient dynamic range. Hence, minimizing the saturation effects of the ADC at the receiver section. Feed forward architecture is designed to control the gain of 4 stages of VGA, each of 15dB gain factor. Therefore achieving marginal attack time and high stability at the output signal. This paper depicts the efficient work where an overall AGC gain of 60dB is achieved, comprising an attack time of 52.94ns. The novel AGC structure designed for Bluetooth receiver is simulated on MATLAB tool. The designed AGC algorithm controls the amplification factor for effective reception of data in high data rate BLE receivers.

Keywords—Analog to Digital Converter(ADC), Automatic gain control(AGC), Dynamic range, Feed-Forward Digital Automatic Gain Control(FF-DAGC), Variable Gain Amplifier(VGA).

I. INTRODUCTION

Communication is the process of imparting purposeful information from one entity to another. The actively present elements of electronic communication systems are basically a communication medium, a transmitter, and the receiver. Wireless communication, is a methodology which incorporates all the mechanisms for exchanging intended information between two devices without the presence of any physical infrastructure. The prominent applications include GPS, wireless Bluetooth, Wi-Fi, cordless telephone etc., where air/vacuum acts as the transferring medium. Most of the wireless systems are being enhanced and analyzed over the digital communication, where the modulation and transmission of digital bits takes place through free space.

Receivers are the fundamental component of communication system. In most of the wireless transceiver applications, the received signals rarely maintain the constancy as they deviate from the actual signal properties during the transmission process. Received signals, before being fed to ADC, are filtered, amplified and down-

converted for the recovery of data. The analog input has a wider dynamic range and can lead to saturation of ADC at the receivers due to the over amplification of the received analog signal. AGC is one such integral block of wireless communication, which tunes the receiver gain adjusting the output level to achieve desired dynamic range of ADC's. AGC is the principal function in wireless receivers, which maintains the output signal level of Variable Gain Amplifier (VGA) for varied input signal strengths [8]. VGA is used to amplify the incoming signals to maintain the gain linearity [15]. It is used to control the gain of analog front end operators such as Band Pass Filter (BPF), VGA and mixer to minimize ADC saturation effects.

DAGC governs the gains of VGA through digital control signals, hence regulating the amplitude range [14]. DAGC could be administered both in feed-forward and feedback configuration. It yields the amplifying factor which is required to obtain the output in required range. Feed-forward configuration, whose input is being fed by the digital peak detector, is employed in this work. It controls the gain of front end operators, which maintains the coarse tuning of 4 stages of VGA in order to sustain marginal attack time and attain more stability. FF architecture shortens the settling time and minimizes the acquisition time [8]. In this depicted work, essential output is 1V reference.

The aim of the work is to design and analyze DAGC with wider dynamic range and lesser settling time for Bluetooth receivers. Bluetooth, being the standard protocol in wireless communication operates at frequency 2.4GHz and supports a short range communication of 700-800m. Bluetooth employs GFSK (Gaussian frequency shift key) modulation and has burst mode data transmission. The DAGC which is present at the receiver is used in feed-forward (FF) loop configuration which controls the gain of analog front-end amplification in Bluetooth receiver. Hence, this paper represents the design and analysis of digital AGC for maintaining controlled constant output regardless of the contrast in the input levels, as to intensify the efficiency.

III. RELATED WORK

Okjune Jeon et al., in [5] has designed a circuit that detects signal strength from repeated Orthogonal-Frequency Division Multiplexing (OFDM) short training symbols & uses an inverse gain feed technique. This paper focuses on analog AGC. Implementation of AGC in analog circuitry gives lower system power. It is implemented in a 0.18 μ m CMOS process. It achieves 40dB attenuation at 20 MHz and 54 dB at 40 MHz. It settles to within 1 dB in 0.6 μ s and attack time being 5.6 μ s.

J.P.Alegre, et al., in [8] has implemented a 0.35 μ m standard CMOS technology in this system. The system consumes 1.6mW power with supply voltage of 1.8V at frequency response of 100MHz. The attack time of the system is 0.02 μ s and decay time is 0.25 μ s. Gain of the system ranges from 0 to 21dB. The cost of the chip is reduced. Large integration is attained by the development in CMOS technology. To avoid undesired feedback the requirement of resistor banks is more.

J.P.Alegre et al., in [13] has effectively proposed a double loop AGC circuit which depicts the applications concerned with the combination of feed forward loop and feedback loop. This design has been constructed with respect to standard 0.35µm CMOS technology with 1.8V as the supply voltage and current consumption is below 1.22mA. Settling time of the AGC is below 0.8µs and attack time is 0.7µs with dynamic gain adjustment of 12dB. This work proposes low cost model which provides constant bandwidth.

III. PROPOSED WORK 3.1. Block Diagram

The proposed AGC architecture with extensive dynamic range and minimal attack time is procured from the Fig1 shown below:

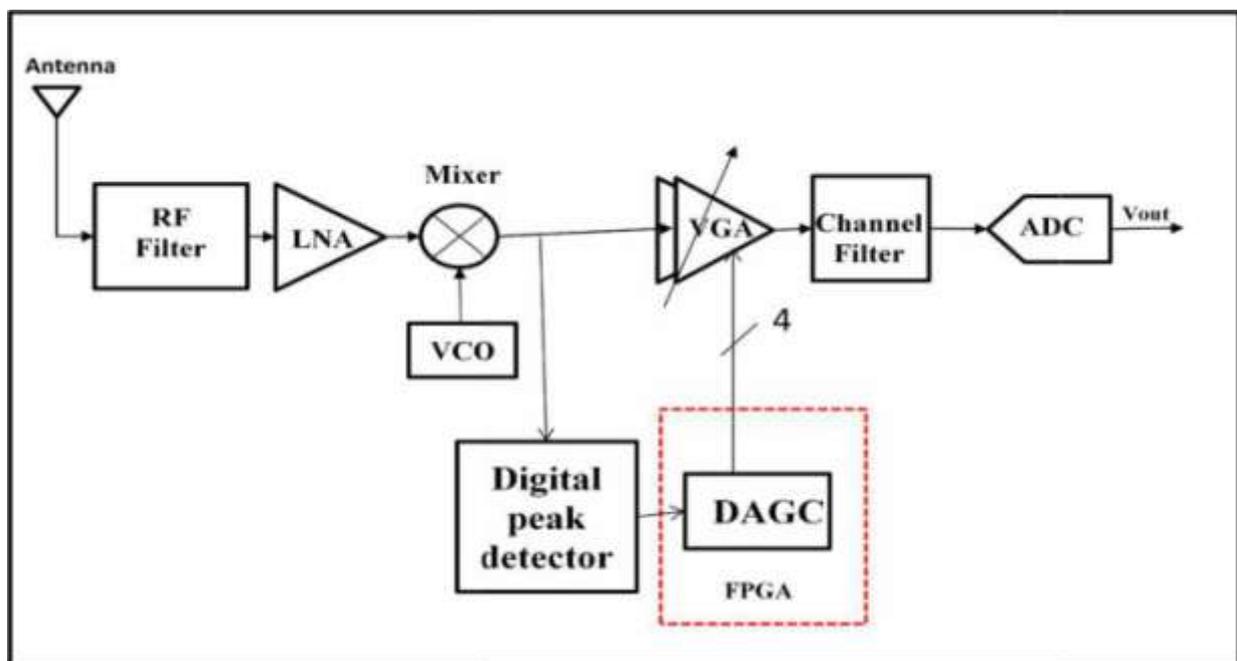


Fig.1.General block diagram for Bluetooth low energy receiver

The receiver consists of active channel filter, VGA, mixer, Voltage controlled Oscillator (VCO), digital peak detector and DAGC block as depicted in the Fig1. To reduce the saturation effects of ADC, AGC is employed at the receiver which controls the gain of analog front end operators. The VCO provides the optimum frequency range required by the Bluetooth receiver to operate i.e., 2.4GHz. Digital peak detector finds the peak of the received analog signal and provides it to the DAGC block. The 4 stages of VGA are controlled by DAGC.

AGC, also known as automatic volume control is used to accommodate input strength variations providing regulated signal amplitude at the output. VGA, also known as voltage controlled amplifier is designed having

gain of 15dB each and amplifying factor of about 31.62V. When all the 4 amplifiers are turned ON, we get maximum gain about 60dB. Each amplifier is controlled by digital control bits which are obtained from DAGC block.

The undertaken evaluation is based on the previous journals which illustrates the benefits and drawbacks of the existing AGC techniques. This detailed evaluation is to procure convenient parameters such as gain controlled signal amplitude at the output side, to maintain stringent settling time and dynamic range. In addition to this, to have regulated control on factors such as gain tuning range, data rate, power dissipation, circuit linearity, bandwidth efficiency etc., this mentioned work has been carried out and revised elaborately.

3.2. Result

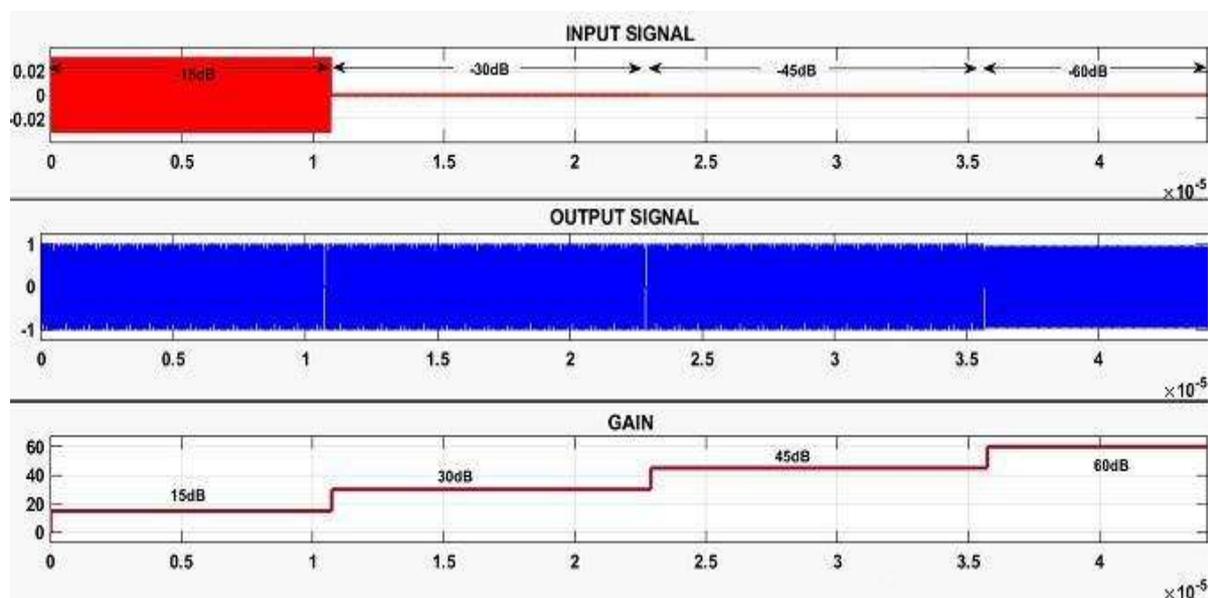


Fig.2.Simulation results

The above estimated and evaluated result portrays the optimized outcome determining the efficiency of the work undertaken. It shows that irrespective of the changes in the input strengths, the output is maintained to the optimum controlled level. The output is maintained with respect to the requisite level, which being 1V reference voltage in this respective work.

The DAGC simulation is carried out on MATLAB tool. The proposed algorithm will be validated on digital signal processor platform. The simulation and measurement results have varied advantages in aspects of constancy and astringency. The procured result illustrates an estimation of overall gain of 60dB; attack time range being 52.94 μ sec. This journal depicts the work done to design and analyze the enhanced AGC features, which forms an essential layout in numerous applications.

IV.CONCLUSION

The efficiency of the received signals does not maintain the persistency due to varied external and inherited reasons in Wireless systems. Employed traditional techniques which were administered to invalidate the limitations could not tackle the wider dynamic range. Numerous works have been endeavored to counteract the drawbacks of wireless communication but could not achieve the desired output. Hence, this paper represents the design and analysis of digital AGC for maintaining controlled constant output regardless of the contrast in the input levels, as to intensify the efficiency.

This work summarizes the salient features of evaluated digital AGC. The main ideology of the paper is to design and analyze DAGC for Bluetooth low energy receivers. AGC layout, in feed-forward gain control technique is accomplished for achieving fast settling time, of 52.94ns and evaluates wider dynamic range, attaining maximum up to 60dB. The simulation and estimated results have diverse benefits in aspects of constancy and astringency, predominantly in wireless receivers.

REFERENCES

- [1]Hyunchol Shin, Dong-Jin Keum, Jin-Sub Choi, Duck-Young Jung, Byeong-Ha Park, "Highly Linear Variable Gain Amplifiers with Programmable Temperature Compensation for CDMA Wireless Applications," IEEE International Symposium on Circuits and Systems, pp. 467-470, May 2000.
- [2]Chonghoon Kim, Sungbin Im, "Digital automatic gain control for software radio W-CDMA base stations," in Electronics Letter, Vol. 39, No. 3, pp. 318-320, February 2003.
- [3]Thomas Byunghak Cho, David Kang, Chun-Huat Heng, Bang Sup Song, "A 2.4-GHz Dual-Mode 0.18- μ m CMOS Transceiver for Bluetooth and 802.11b," IEEE Journal Of Solid-State Circuits, Vol. 39, No. 11, pp. 1916-1926, November 2004.
- [4]Corrado Carta, Rolf Vogt, Werner Bächtold, "Multiband Monolithic BiCMOS Low-Power Low-IF WLAN Receivers," IEEE Microwave And Wireless Components Letters, Vol. 15, No. 9, pp. 543-545, September 2005.
- [5]O.Jeon, R.M.Fox, B.A.Myers, "Analog AGC Circuitry for a CMOS WLAN Receiver," IEEE Journal of Solid State Circuits, Vol. 41, No. 10, pp. 2291-2300, October 2006.
- [6]FENG Dong, SHI Bingxue, "Linear-in-dB Variable-Gain Downconversion Mixer for Zero Intermediate Frequency Receivers," Tsinghua Science and Technology Issn, Pp. 8-11, Vol. 11, No. 1, February 2006.
- [7]I.-Hsin Wang, Shen-Iuan Liu, "A 0.18 μ m CMOS 1.25Gbps Automatic Gain Control Amplifier," IEEE Transactions on Circuit and Systems-II: Express Briefs, Vol. 55, No. 2, pp. 136-140, February 2008.
- [8]J.P.Alegre, S.Celma, B.Calvo, "A High Performance CMOS Feedforward AGC circuit for Wideband Wireless Receivers", IEEE International Symposium on Industrial Electronics, Vol. 30, No.5, pp. 1657-1661, November 2008.

- [9]Yong-Xin Guo, Viet Hung Pham, Ming-Li Yee, Ling Cheun Ong, “Improved Radio-Over-Fiber Transponder with Multistage Automatic Gain Control”, IEEE Transactions on Microwave Theory and Techniques, Vol. 57, No. 11, pp. 2816-2823, November 2009.
- [10]J.P.Alegre, S.Celma, B.Calvo, “SiGe Analog AGC Circuit for an 802.11a WLAN Direct Conversion Receiver”, IEEE Transactions on Circuit and Systems-II: Express Briefs, Vol. 56, No. 2, pp. 93-96, February 2009.
- [11]Anbang Liu, Jianping An, Aihua Wang, “Design of a Digital Automatic Gain Control with Backward Difference Transformation,” IEEE Wireless Communications Networking and Mobile Computing, pp. 1-4, September 2010.
- [12]J.P.Alegre, B.Calvo, S.Celma, “A High-Performance CMOS Feedforward AGC Circuit for a WLAN Receiver”, IEEE Transactions on Industrial Electronics, vol. 57, No. 8, pp. 2851-2857, August 2010.
- [13]J.P.Alegre, B.Calvo, S.Celma, F.Aznar, “CMOS Combined Feedforward/Feedback AGC Circuit for VHF Applications,” Midwest Symposium on Circuits and Systems, pp. 709-712, August 2010.
- [14]Anbang Liu, Jianping An, Aihua Wang, “Performance Analysis of a Digital Feedback AGC with Constant Settling Time,” IEEE International Conference on Communication Technology, pp. 1060-1063, November 2010.
- [15]Shang-Hsien Yang and Chua-Chin Wang, “A 48-dB Dynamic Gain Range/Stage Linear-in-dB Low Power Variable Gain Amplifier for Direct-Conversion Receivers,” IEEE International Conference in SoC Design, pp. 1821-1824, November 2011.
- [16]Xing Zheng, Zhi Gang Wang, Yue Cheng Huang, “Implementation of a Two-Stage Digital AGC for Spectrum Analyzer”, IEEE International Conference on Applied Superconductivity and Electromagnetic Devices, pp. 37-40, December 2011
- [17]Chongwen Huang, Xiao Yan, Ling He, “A High-Precision All-Digital Automatic Gain Control Algorithm for Broadband Real-Time Spectrum Analyzer”, IEEE International Conference on Communications, Circuits and Systems, pp. 240-244, November 2013.
- [18]C.Gimeno, C.Sanchez-Azqueta, E.Guerrero, C.Aldea, S.Celma, “A 1-V 1.25Gbps CMOS Analog Front-end for Short Reach Optical Links,” Proceedings of the ESSCIRC, pp. 339-342, September 2013.
- [19]Xiang Yi, et al., “A 65nm CMOS Carrier-Aggregation Transceiver for IEEE 802.11 WLAN Applications,” IEEE Radio Frequency Integrated Circuits Symposium, May 2016.
- [20]Muhammad Asim Ali, Wanod Kumar, Muhammad Arif, “OFDM Receiver Design in the Presence of Both Tx and Rx IQ Imbalance Over Frequency Selective Channels,” IEEE Sixth International Conference on Communications and Electronics, pp. 94-98, July 2016.
- [21]Suchendranath Popuri, Vijaya Sankara Rao, Pasupureddi Johannes Sturm, “A Tunable Gain and Tunable Band Active Balun LNA for IEEE 802.11ac WLAN Receivers,” European Solid-State Circuits Conference, pp. 185-188, September 2016.

- [22] Hanseul Hong, Young Yong Kim, Ronny Yongho Kim, Sung-Hyun Hwang, Seungkeun Park, "A Novel Low Power WLAN Operation scheme for Multiple Wake-Up Receivers," IEEE International Conference on Consumer Electronics, January 2017.
- [23] Seongwon Kim, et al., "FACT: Fine-Grained Adaption of Carrier Sense Threshold in IEEE 802.11 WLANs," IEEE Transactions on Vehicular Technology, Vol. 66, No. 2, February 2017