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A Review on Implementation of Digital Filters on FPGA

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ABSTRACT

Field-Programmable Gate Arrays (FPGAs) have become one of the keydigital circuit implementation media over the last decade.Digital filtering algorithms are implementedusing general purpose digital signal processing chips and application specific integrated circuits (ASICs) for higher rates. Thispaper reviews an approach to the implementation of digital filteralgorithms based on FPGAs.The advantages of the FPGA approach to digital filter implementationinclude higher sampling rates than are available fromtraditional DSP chips, lower costs than an ASIC for moderatevolume applications, and more flexibility than the alternate approaches.The paper also includes a survey of the modern FPGA architecture, and digital filters. The FPGA based digital filter design reduces the complexity and cost by reducing the number of multipliers and adders. Also it provides superior performance to the traditional approaches.

Keywords:FIR, IIR, FPGA,ASIC, VHDL.

I INTRODUCTION

Traditionally, digital signal processing (DSP) algorithms are implemented using general purpose programmable DSP chips for low-rate applications. Alternatively, special purpose fixed function DSP chipsets and application specific integrated circuits (ASICs) are used for high-performance application. Technological amendment by Xilinx on FPGAs in the past few years has opened new paths for engineers to design various applications on FPGAs. The FPGAs assert the high explicitness of the ASIC while avoiding its high development cost and its inability to accommodate design modifications after production. Highly adaptable and design-flexibility, FPGAs provide optimal device utilization through conservation of board space and system power important advantages not available with many stand-alone DSP chips [1].

A large application area is telecommunication, where filters are needed in receivers and transmitters, and an increasing portion of the signal processing is done digitally. However, power dissipation of the digital parts can be a limiting factor, especially in portable, battery operated devices. Scaling of the feature sizes and supply voltages naturally helps to reduce power. For a certain technology, there are still many kinds of architectural and implementation approaches available to the designer.

II DIGITAL FILTERS

Digital Filter is numerical procedure or algorithm that transforms a given sequence of numbers into a second sequence that has some more desirable properties. They are more size and powers efficient than analog filters in various applications as linear phase, very high stop band attenuation, very low pass band ripple. Filter's response must be programmable or adaptive; the filter must manipulate phase and, very low shape factors. There

are two basic types of digital filters, Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters.Block diagram of FIR and IIR filters in terms of basic elements (Adder, multiplier and delays) is shown in Fig 1 and 2 respectively.Moreover in case of analog filters with increase in the order of the filter the number of filter components increases which increases it's complexity. Another disadvantage of analog Filters for which digital filters came in the limelight is that the cut off frequency depends on the values of the filter components like resistor and capacitor values, any change in component values which is technically referred to as drift of components due to time or physical parameters like temperature, changes the cut off frequency of the filter. These problems can be overcome in digital filters whose characteristics depends on the filter coefficients which once programmed for a specific filter order and type do not change with time.Moreover digital filters are advantageous over the analog counterpart in the sense that they have faster roll off, less transition width and less overshoot in case of time domain operations[5].

The digital filter has merge as a strong option for removing noise, shaping spectrum, and minimizing inter-symbol interference in communication architecture. These filters have become popular because their precise reproducibility allows design engineers to achieve performance levels that are difficult to obtain with analog filters [6].

As the FIR system have a lot of good features, such as only zeros, the system stability, operation speed quickly, linear phase characteristics and design flexibility, so that FIR has been widely used in the digital audio, image processing, data transmission, biomedical and other areas. It has a variety of ways to achieve, with the processing of modem electronic technology, taking use of FPGA for digital signal processing technology has made rapid development, FPGA with high integration, high speed and reliability advantages, FIR filter implementation using FPGA is becoming a trend.[6].

Filter properties, design criteria, and theapplications are the important parameters used to decidewhich filter to choose.

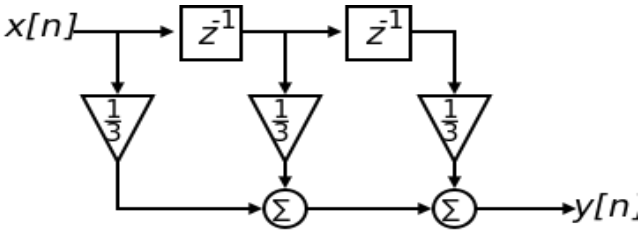

Fig 1 Block diagram of FIR filter

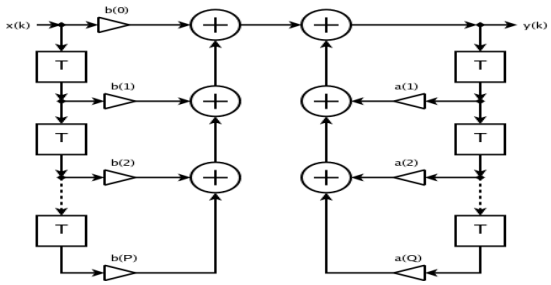

Fig 2 Block diagram of IIR filter

III FPGA

The Field Programmable Gate Array is a type of device that is widely used in electronic circuits. FPGAs are semiconductor devices which contain programmable logic blocks and interconnection circuits. It can be programmed or reprogrammed to the required functionality after manufacturing.They were first introduced almost two and a half decades ago. Since then they have seen a rapid growth and have become a popular implementation media for digital circuits. The advancement in the process technology has greatly enhanced the logic capacity of FPGAs and has in turn made them a viable implementation alternative for larger and complex designs. The architecture of FPGA is shown in Fig. 3. Further, programmable nature of their logic and routing resources has a dramatic effect on the quality of final device's area, speed, and power consumption. Figure 4 shows the design flow of FPGA.

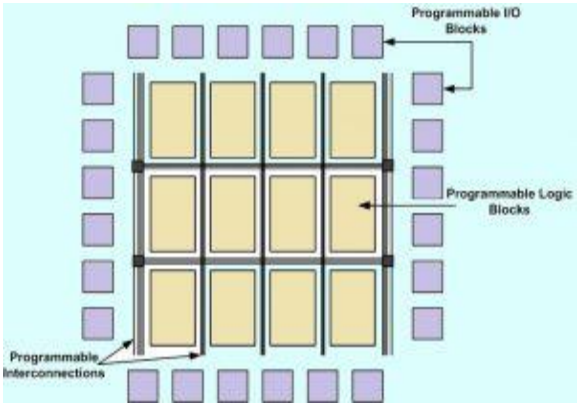

Fig 3Architecture of FPGA

FPGAs are becomingincreasingly popular for rapid prototyping of designs withthe aid of software simulation and synthesis. Softwaresynthesis tools translate high-level language descriptionsof the implementation into formats that may be loadeddirectly into the FPGAs. An increasing number of design changes through softwaresynthesis become more cost effective than similar changes done for hardwareprototypes.FPGAs are widely used in the implementation of fast digital systems for retrieval, processing, storage, and transmission of data.Xilinx, Altera, Lattice, Actel, Quick logic are some of the companies making FPGAs in the world.Verilog and Very High Speed Integrated Circuit HDL (VHDL) are hardware description languages used to design digital logic using FPGAs and CPLDs. FPGAs provide optimal device utilization through conservation of board space and system power.

IV IMPLEMENTATION OF DIGITAL FILTERS ON FPGA

This section concludes that digital filters can be implemented in flexible FPGA based architecture where the coefficients can be programmed and changed when required to implement filters of specific requirement.

The various digital filters are designed to obtain a noise free ECG signal using wavelet toolbox and their performances are compared based on parameters like Signal to Noise Ratio (SNR), Error and Accuracy. Further their performance is validated by using Power Spectrum Density (PSD) and Fast Fourier Transform (FFT) A final summary report on the study of complexity of the structure of filters is presented and realized using MATLAB [10].

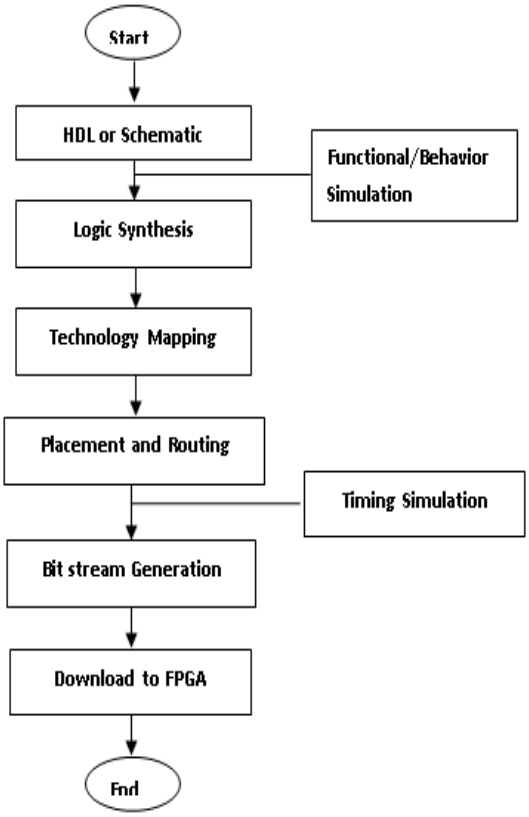

Fig 4 FPGA Design Flow

A reconfigurable FPGA based pipelined FIR filter implemented and analyzed. This realized FIR filter compared for area, power dissipation and data processing rate . For the implementation of FIR filters, Simulation and compilation of the VHDL code written using Mentor Graphics ModelSim. For the synthesis targeting to FPGA Xilinx Virtex II Pro XP2VP30 device and Xilinx ISE Design Suite 10.1 tool is used. For the Power estimation Xilinx Xpower tool is used. Further, FPGA implementation of FIR filter model with respect to power, silicon area, and data processing rate analyzed.[2].

A typical example is mobile communications where hand-held, battery supplied, devices, such as cellular phones, are used. To obtain a long uptime between recharges of the battery for cellular phones, low power consumption is required. Due to the requirements on high data rates in many communication systems, the corresponding subsystems and circuits must have a high throughput as well. Since significant parts of such communication systems are customer products that are produced in large quantities and are sold at low prices, efficient, fast, and reliable design methods as well as low cost circuit implementations are required. The need for miniaturization of systems also requires subsystems with low power consumption. For such integrated systems, the heat dissipation and the cooling becomes a problem. Low power consumption and circuit area are therefore key design constraints [2].

An efficient method for implementation of digital filters targeted on FPGA architectures is presented. The traditional approach is based on application of general purpose multipliers. However, performance of multipliers

implemented in FPGA architectures does not allow to constructs high performance digital filters. Hence distributed arithmetic is demonstrated. In this approach combinational LUT blocks replace general purpose multipliers, it is possible to construct digital filters of very high performance [3].

Since speed is among the chief interest in this era; the main objective is to enhance the speed of the system. Therefore, FIR & IIR digital Filters are being designed using HDL languages.If the speed of the individual block is enhanced the overall speed of the system canbe enhanced. The objective of developing appropriate algorithms in order to attain an effective utilization of the available hardware. Since speed, power and chip area are the most often used measures of the efficiency of an algorithm, there has a strong link between the algorithms and technology applied for its implementation. It hasbeen done by applying the pipelining technique and simulation and synthesis for FPGAs has been accomplished on Spartan 3 series FPGA, target device (XC3S500E) (Speed Grade -4) and Virtex 2P series FPGA, target device (XC2VB50) (Speed Grade -6) from Xilinx.. The comparative analysis of pipelined & non-pipelined FIR and IIR filters performed by using different FPGA's and turned in a consistent quality of output [4].

Nowadays Digital Filters are replacing Analog Filters which are used widely in front end Electronics to remove the unwanted component from the signal and increase the signal to noise ratio. Their widespread popularity is basically because of a set of programmed coefficients derived from the analog filter specifications which can in whole control the filter operation and unlike analog filters the value of bulky capacitors and inductors do not affect the filter operability. Initially digital filters were implemented on PDSP and ASIC. But due to the comparatively lower cost and customized design possibilities, FPGA based system have gained much popularity.Moreover most of the FPGAsare reprogrammable hence by programming different filter coefficients the type of filter implemented can be changed as required [5]

Implementing hardware design in FPGAs is a formidable task. There is more than one way to implement the dsp design for digital filters. Based on the design specification, careful choice of implementation method and tools can save a lot of time and work. There are various toolboxes available to generate VHDL (Verilog) descriptions of the filters which reduce dramatically the time required to generate a solution. Time can be spent valuating different implementation alternatives. Proper choice of the computation algorithms can help the FPGA architecture to make it efficient in terms of speed and/or area [6].

With the advent of personal computer, smart phones, gaming and other multimedia devices, the demand for DSP processors in semiconductor industry and modern life is ever increasing. Traditional DSP processors which are special purpose (custom logic) logic, added to essentially general purpose processors, no longer tends to meet the ever increasing demand for processing power. Today FPGAs have become an important platform for implementing high–end DSP applications and DSP processors because of their inherent parallelism and fast processing speed [7].

Finite Impulse Response filter is mostly used in the digital signaling processing (DSP) applications. In FIR most important parameters are complexity, cost, and power consumption. While the research focused on to resolve this issue by using the Multiple Constant Multiplication (MCM) for optimizes the adder tree in the filter [8].

Now a days the advances in technology leads to use of FPGA for the implementation of Digital Filters. Digital IIR Butterworth filter designed using Simulink in MATLAB environment and implemented using Xilinx System Generator. The Quantization and Overflow are main crucial parameters while designing the filters on FPGA and that need to be consider for getting the stability of the filter. As compare to the conventional DSP the speed of the system is increased by implementation on FPGA. The filer has giventhe good performance for noise removal in ECG Signal [9].

V CONLUSION

Implementation of general purpose DSP implementations often lacks theperformance necessary for moderate sampling rates, and ASICapproaches are limited in flexibility and may not be cost effective. A Verilog implementation of FPGA based digital filters produces appreciable results because of various benefits like low power consumption, higher efficiency, faster etc.Various approacheswhich are surveyed are most effective for implementations with the constraints oflow cost and low power.The modern architecture of FPGA reduces the number of multipliers and suggesting the small chip area. Also it illustrated that the FPGA approach is both flexible and providesperformance comparable or superior to traditional approaches because of the programmability of this technology.

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