International Journal of Advance Research in Science and Engineering
Volume No.07, Special Issue No.03, April 2018
www.ijarse.com
IJARSE
ISSN: 2319-8354

High Gain and Low Power Rail-to-Rail Amplifier

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ABSTRACT

One of the most important building blocks in modern IC design is the operational amplifier. For the portable electrocardiogram (ECG), the operational amplifier is employed to sense and amplify the electrical signal of heartbeat of human body. For the battery powered portable ECG system, low supply voltage environments are required to reduce power consumption and the result is a reduced input common mode range (ICMR) of the op-amp. Complementary differential pairs are commonly used to achieve a rail-to-rail input common mode range in order to overcome the problem of reduced ICMR. However, this complementary differential input pair structure can have a substantial transconductance (g_m) variation problem and a dead zone problem in a low supply voltage environment and an extremely low supply voltage environment respectively. On reduction in supply voltage to a standard CMOS op-amp, the input common mode range and the output swing get reduced drastically. Special circuits have to be used to raise them up to rail-to-rail supply voltage. In this paper design of a low-voltage CMOS rail-to-rail operational amplifier is proposed. For 1V single supply voltage, the Proposed Circuit Technique can be used to avoid the dead zone of input stage. Cadence Virtuoso using 180 nm technology node is used to simulate this work.

Keywords- Operational Amplifier, Low Voltage, Rail-to-Rail, signal compression

I. INTRODUCTION

As there is a decrease in the supply voltage and current of an analog circuit there are certain performance measures of the circuit which will suffer a loss in performance. For example, for lower supply voltages the signal to noise ratio of the circuit will decrease, as the maximum input and output signal for the circuit will be smaller. Also the bandwidth that could be achieved will be reduced as the supply voltage and total current are reduced. There are two possible situations according to the environment of supply voltage. The first situation is about two times the transconductance variation problem with low supply voltage environment and the second is dead zone problem with extremely low supply voltage environment.

To avoid the dead zone problem of op-amp in the extremely low supply voltage environment, many techniques have been proposed and in [1], the input signal compression technique that compresses rail-to-rail input signals to the acceptable input range of the following conventional op-amp has been presented. For some portable biomedical devices, however, higher CMRR is still required to reduce common-mode noise from the human

body as well as reduced supply voltage. A novel proposed circuit technique for 1.8V supply is implemented using Input Signal and Common Mode Elimination Techniques.

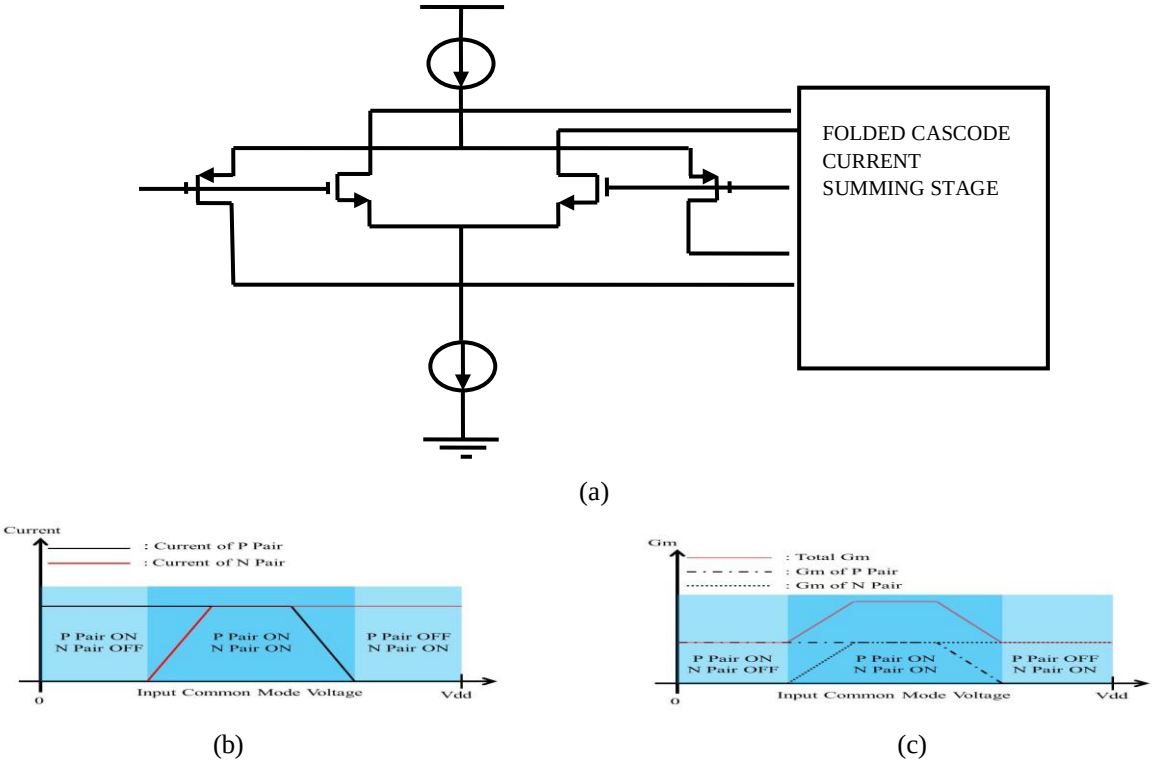

Figure 1. (a) Complementary Differential Pairs (b) Input Stage Current Characteristic with Low Supply Voltage (c) Input Stage Current Characteristic with Extremely Low Supply Voltage

II. INPUT SIGNAL COMPRESSION TECHNIQUE

In [1], the Input Signal Compression Technique has been proposed. The Input Signal Compression Block in Fig 2 compresses rail-to-rail input signals to the input range of the attached conventional PMOS input op-amp.

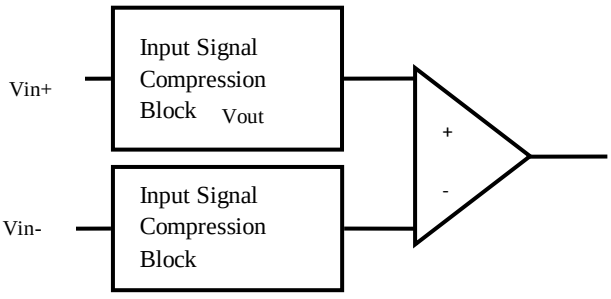

Figure 2. Basic Concept of Input Signal Compression Technique

Fig 3 (a) shows the inside of input signal compression block which is composed of three sub-blocks. The input/output voltage characteristics of each block are shown in Fig 3 (b), (c) and (d). Block 1 consists of a PMOS source follower in the first stage followed by a NMOS source follower in the second stage, and a PMOS source follower in the last stage (Fig3 (b)). This cascade of source followers shifts the input signal and the output voltage of block 1, Vo1, is shown in the graph. The first and the second stage of block 2 are a NMOS and a PMOS source follower, respectively (Fig 3 (c)). At the last stage of block 2, the output voltage Vo2 is constant for low V4 because of source follower operation of the last stage of block 2, while that works as a common-source amplifier which inverts V4 voltage for high V4. Fig 3 (c) shows the overall behavior of block 2.

Two inputs of block 3 are Vo1 and Vo2. Vo3 is the output of block 3 as well as the whole block of signal compression, (Fig 3 (d)). When Vin is low, Vo2 is constant and block 3 operates as a NMOS. When Vin is low, Vo2 is constant and block 3 operates as a NMOS source follower. On the other hand, when Vin is high, Vo1 is constant and block 3 inverts the signal of Vo2. The rail-to-rail input signal Vin is compressed as Vo3 through Input Signal Compression Block.

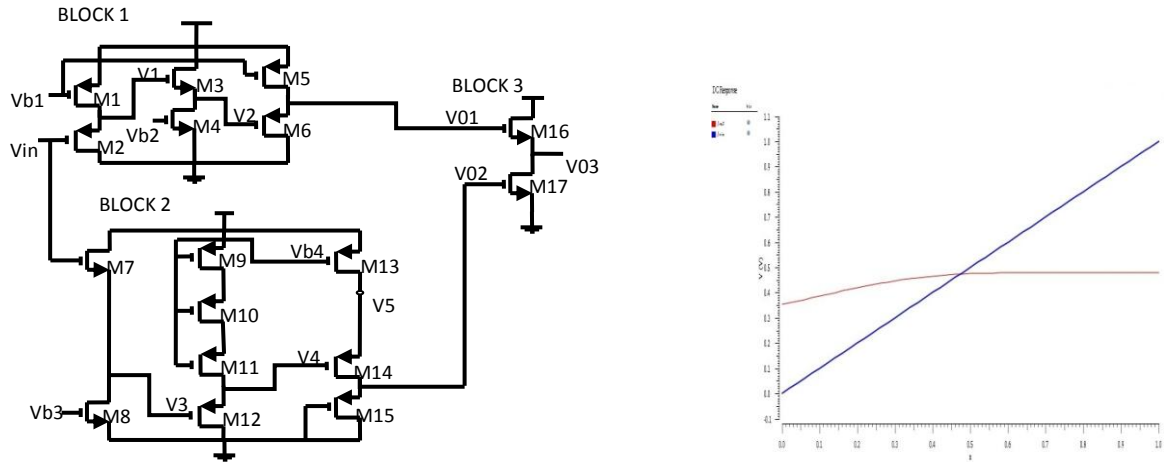

Figure 3 (a) Details of complete Input Signal Compression Block

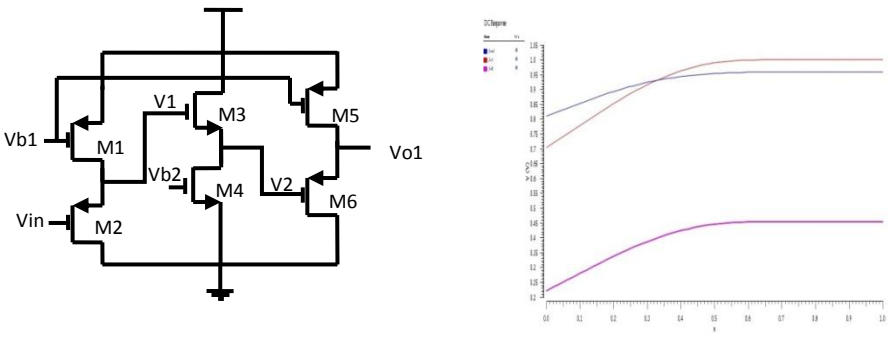

Figure 3 (b) Response of Block 1

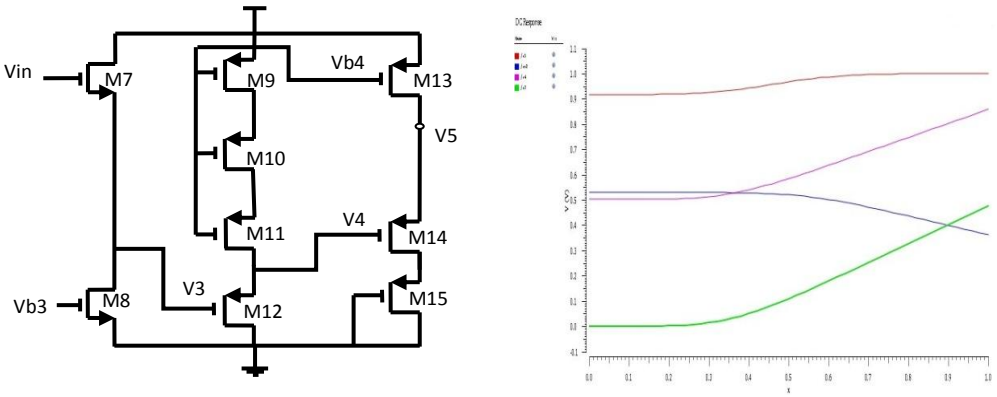

Figure 3 (c) Response of Block 2

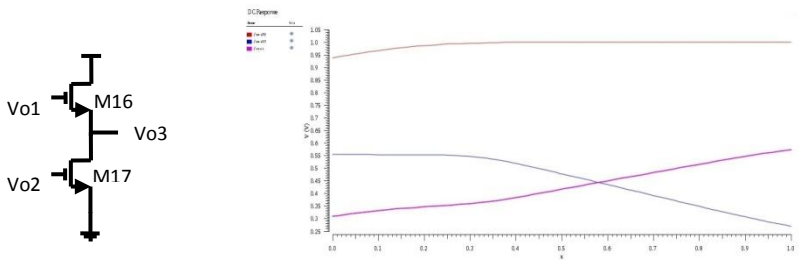

Figure 3 (d) Response of Block 3

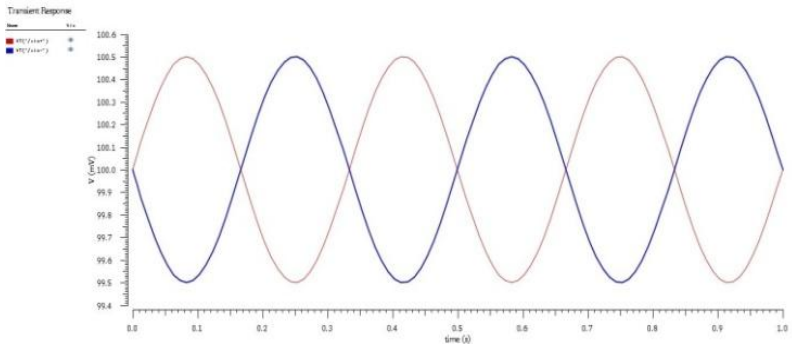

Figure 4. Inputs of Input Signal Compression Blocks

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ISSN: 2319-8354

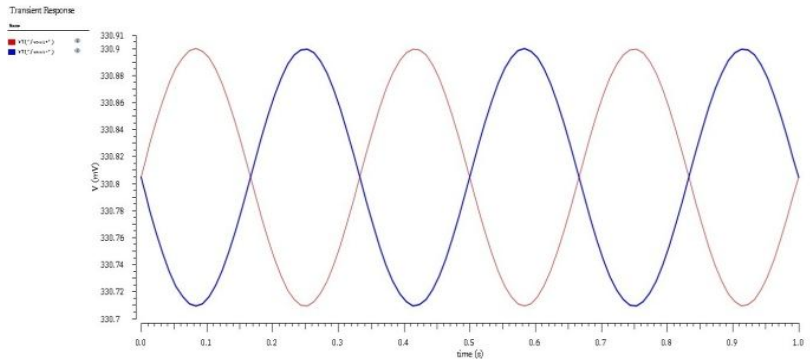

Figure 5. Outputs of Input Signal Compression Blocks

III. COMMON-MODE ELIMINATION TECHNIQUE

Drawback of input signal compression technique is that we cannot achieve additional CMRR advantage from this technique. In Fig 4, the basic concept of novel common-mode elimination technique is shown. In this input signal compression block, signal inverting block, and resistors are used.

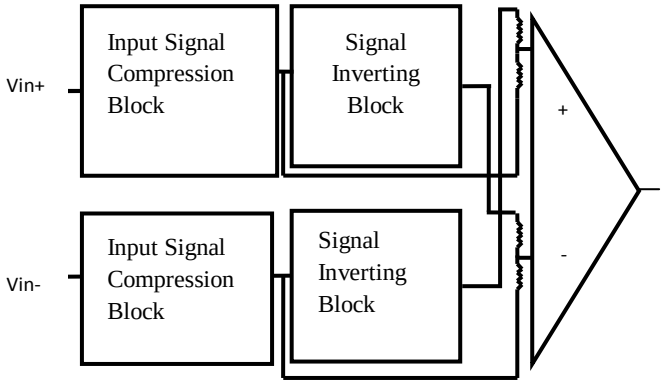

Figure 6. Basic Concept of Common-Mode Elimination Technique

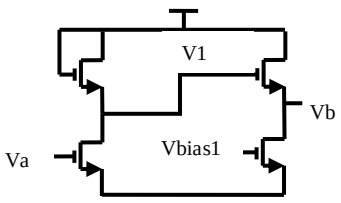

Figure 7. Signal Inverting Block

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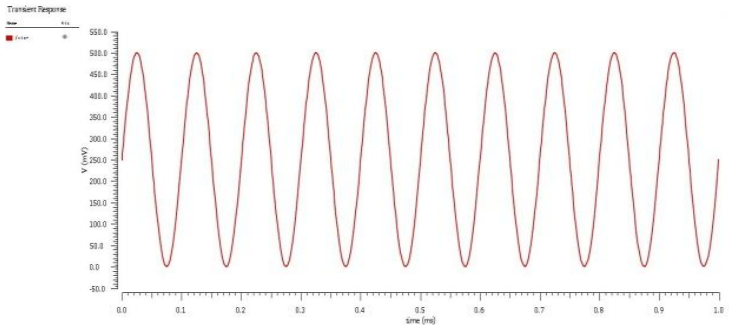

Figure 8. Inputs of Common Mode Elimination Blocks

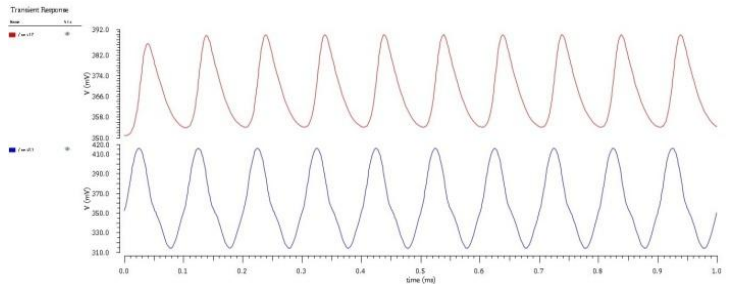

Figure 9. Outputs of Common Mode Elimination Blocks

The compressed input signal is inverted by the first stage of Signal Inverting Block and the second stage shifts that signal to within the input range of the following op-amp. The output of Signal Inverting Block is inverted signal of Input Signal Compression Block. The original differential signal is not eliminated. Instead it is compressed and transferred to the following op-amp. Because outputs of the Input Signal Compression Blocks are cross connected at the resistors stage, differential signal is extracted and transferred to the next stage.

IV. PROPOSED TECHNIQUE

A new input signal compression technique is proposed and is used with signal inverting block and resistors are added. Ultra high CMRR with 1.8V rail-to-rail operation is the biggest advantage of this technique.

In proposed Input Signal Compression Block a differential amplifier that is block 3 is added. Differential amplifiers apply gain not to one input signal but to the difference between two input signals. This means that a differential amplifier naturally eliminates noise or interference that is present in both input signals. Differential amplification also suppresses common-mode signals—in other words, a DC offset that is present in both input signals will be removed, and the gain will be applied only to the signal of interest (assuming, of course, that the signal of interest is not present in both inputs). This is particularly advantageous in the context of IC design because it eliminates the need for bulky DC-blocking capacitors.

Two inputs of block 3 are V_{01} and V_{02} . V_{03} is the output of block 3 as well as the whole block of signal compression.

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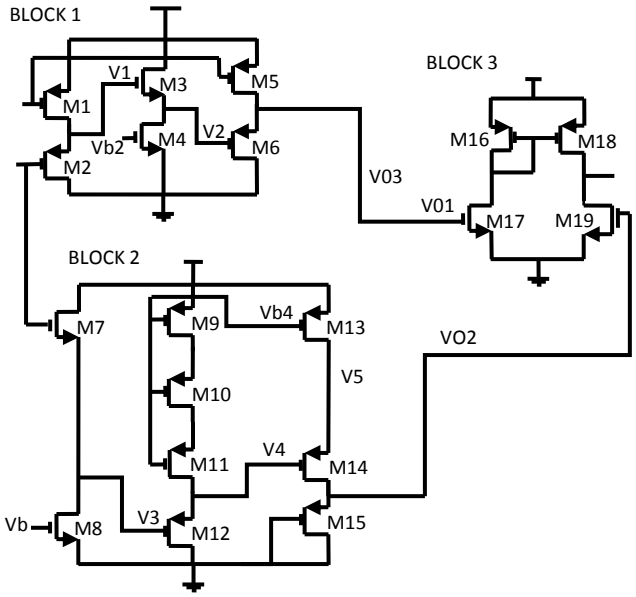

Figure 10. Proposed Input Signal Compression Block

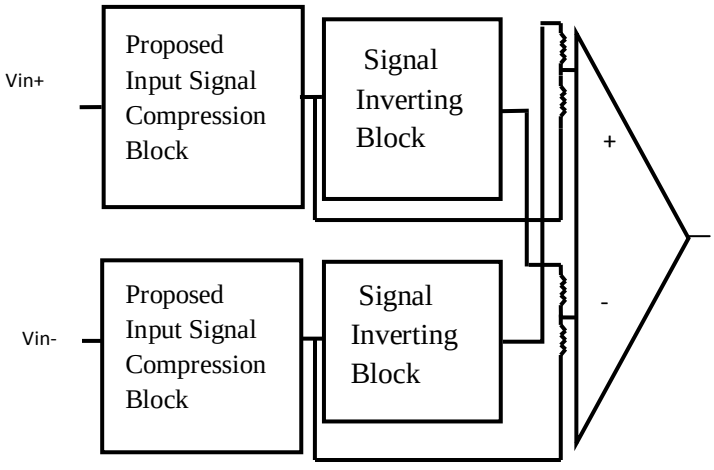

Figure 11. Basic Concept of Proposed Circuit Technique

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In Figure 11 the basic concept of novel proposed circuit technique is shown. First block is the signal compression block of proposed input signal compression technique. Using signal inverting block and resistors,

common mode input signal from 0 to 1V can be kept constant. While differential input signal is extracted and transferred to the following conventional PMOS input differential amplifier. The compressed input signal which is the output signal of input signal compression block is inverted by signal inverting block and using the ratio of two resistors.

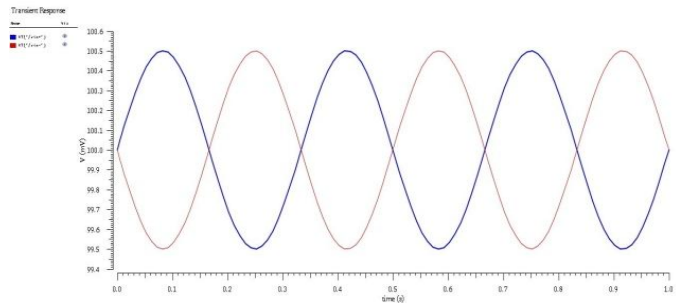

Figure 12. Inputs of Proposed Circuit

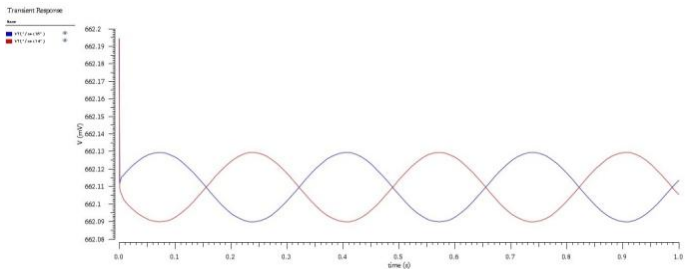

Figure 13. Outputs of Proposed Circuit

Further resistors are replaced by NMOS transistors which improves gain slightly. In many CMOS technologies, it is difficult to fabricate resistors with tightly-controlled values or a reasonable physical size. Consequently, it is desirable to replace such resistance with a MOS transistor. A MOSFET can operate as a small-signal resistor if its gate and drain are shorted. The active resistor can be used in place of polysilicon or diffused resistor to produce a DC voltage drop and /or provide small signal resistance that is linear over a small range. There are many cases where the area required to obtain a small signal resistance is more important than the linearity. A small MOS or BJT device can simulate a resistor in much less die-area than is required with an equivalent polysilicon or diffused resistor[7].

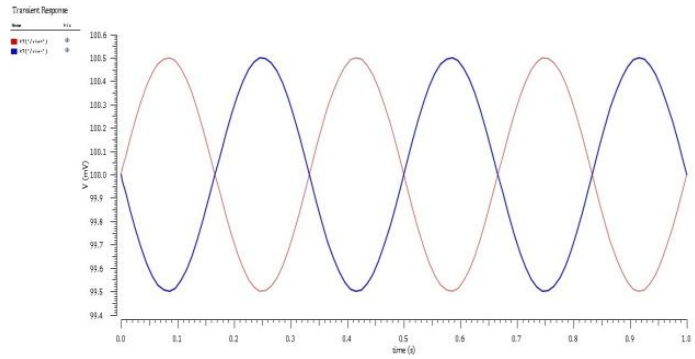

Figure 14. Inputs of Proposed Circuit Technique replaced by NMOS Transistors

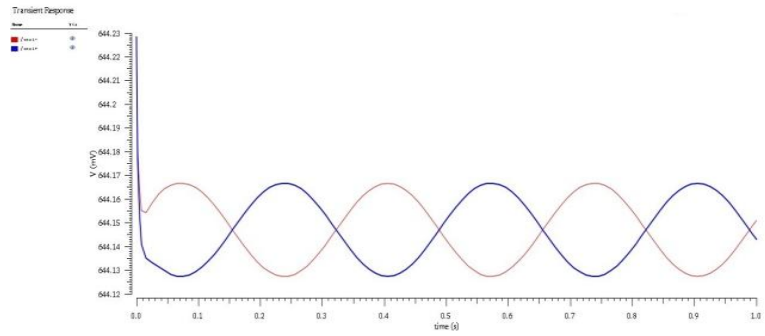

Figure 15. Outputs of Proposed Circuit Technique replaced by NMOS Transistors

V. SIMULATION RESULT

All the circuits in this work have been simulated in cadence virtuso at 180nm node. Results have been summarized in Table 1

Table 1. Comparison of Techniques

Parameters	**Input Signal Compression Technique**	**Common Mode Elimination Technique**	**Proposed Circuit Technique**	**Proposed Circuit Technique Resistors replaced by NMOS Transistors**
Supply Voltage	1.8V	1.8V	1.8V	1.8V
Gain	57.315dB	57.2357dB	59.11dB	59.174dB
CMRR	88.7dB	89.9174dB	113.6945dB	113.75dB
3dB frequency	60.4025Hz	50.6946Hz	45.2448Hz	37.641Hz
Average Power Consumption	28.7µW	29.8 µW	25.06µW	25.069µW
Phase Margin	13.938°	12.927°	10.932°	14.904°

VI. CONCLUSION

Four rail-to-rail op-amp techniques for the portable ECG amplifier are discussed in this paper. The gain, bandwidth, and CMRR of all novel techniques are considered for the ECG system and especially, for the portable electronic biomedical device, operation in the low supply voltage environment is the main consideration of this research for low power consumption. Two rail-to-rail op-amp techniques, the Common Mode Elimination Technique and the Input Signal Compression Technique, are proposed for the extremely low supply voltage environment and overcome the dead zone problem. A novel circuit technique is proposed in this paper. Proposed input signal compression technique is used and signal inverting block and resistors are added. Ultra high CMRR with 1.8V rail-to-rail operation is the biggest advantage of this technique. The bandwidth of this technique is quite low, but for some portable biomedical applications like portable ECG, this bandwidth is sufficient but low power and high CMRR are mandatory.

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