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Simulation study of CMOS Compound Pair Amplifier

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ABSTRACT

In the present paper we study about the parameter and characteristic analysis of Low Power and high speed CMOS compound pair circuit in 0.18 micrometer Technology. The proposed circuit work for very low input voltage signal like pulse rate of heart beat with higher gain wide band frequency response. We have also study about transient and AC response at various temperatures. This circuit shows excellent temperature stability in the temperature range -50, 27 and 100 ° C. It is found that proposed circuit works as amplifier at radio frequency region.

Keywords: CMOS compound Pair, temperature stability, radio frequency, gain and bandwidth.

I.INTRODUCTION

In CMOS integrated circuits many factors are control the possible speeds for example, dimension of devices, logic circuit style, clocking strategy, architecture clock distribution etc. To pursue high speed and integrated density the dimension of MOS transistors are scaled down continuously. The delay in a CMOS circuit will be inversely proportional to the scaling factor α if all dimensions are reduced without changing physics [1]. However there are physical geometrical [2,3] and cost limits on scaling down transistors. Therefore we should tap the potential of the most popular technique. CMOS devices having two important characteristics like high noise immunity and low static power consumption as CMOS devices do not produce as much waste heat as other forms of logic, like transistor–transistor logic (TTL) or NMOS logic[4,5,6,7].

The present paper provides the study of low input voltage with high output voltage gain at higher frequency. In present investigation we have used additional circuit element inductor as output load of CMOS compound pair amplifier thus in present module both gain and bandwidth are increased at high frequency.

II. CIRCUIT

The proposed CMOS compound pair amplifier circuit shown in the Fig.1 have been simulated having atransient as well as a.c. input signal Vdc=1.8uV and Vpulse, Ci=1µf, Ri=500Ω, R1=47kΩ, R2=5KΩ, R3=10kΩ, Rs=2kΩ Rl=10kΩ, Vd=5Vdc, Cs=10µf, Co=10µf and the CMOS as combination of PMOS and NMOS is used as an active component to design the circuit.

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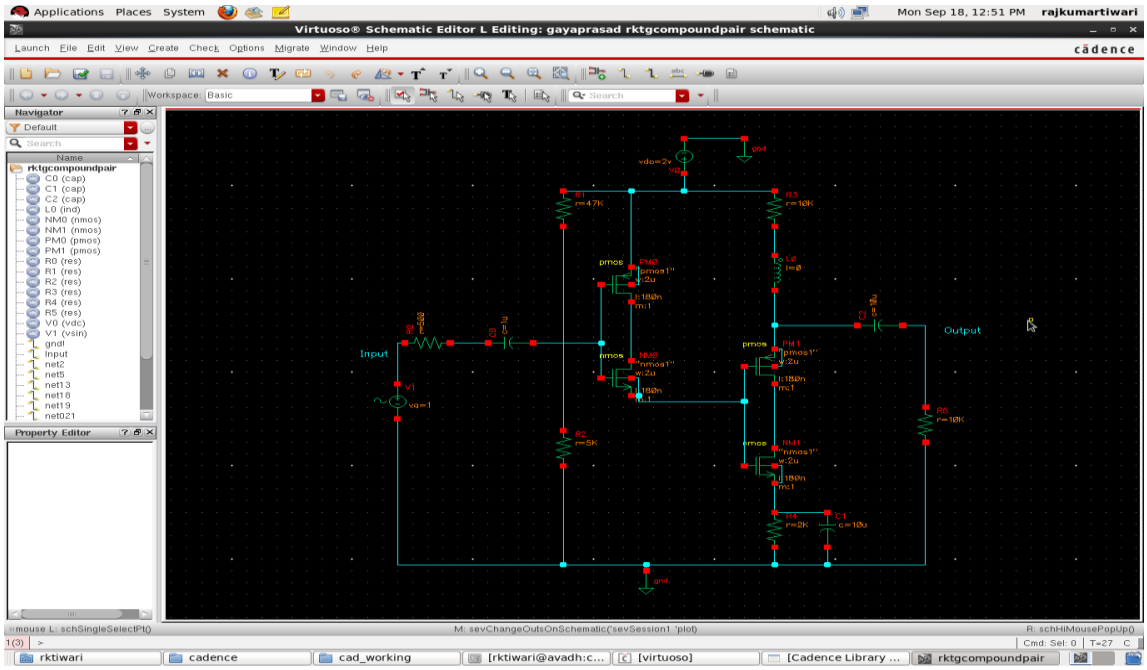

Fig.1 CMOS Compound pair amplifier

III. RESULTS AND DISCUSSIONS

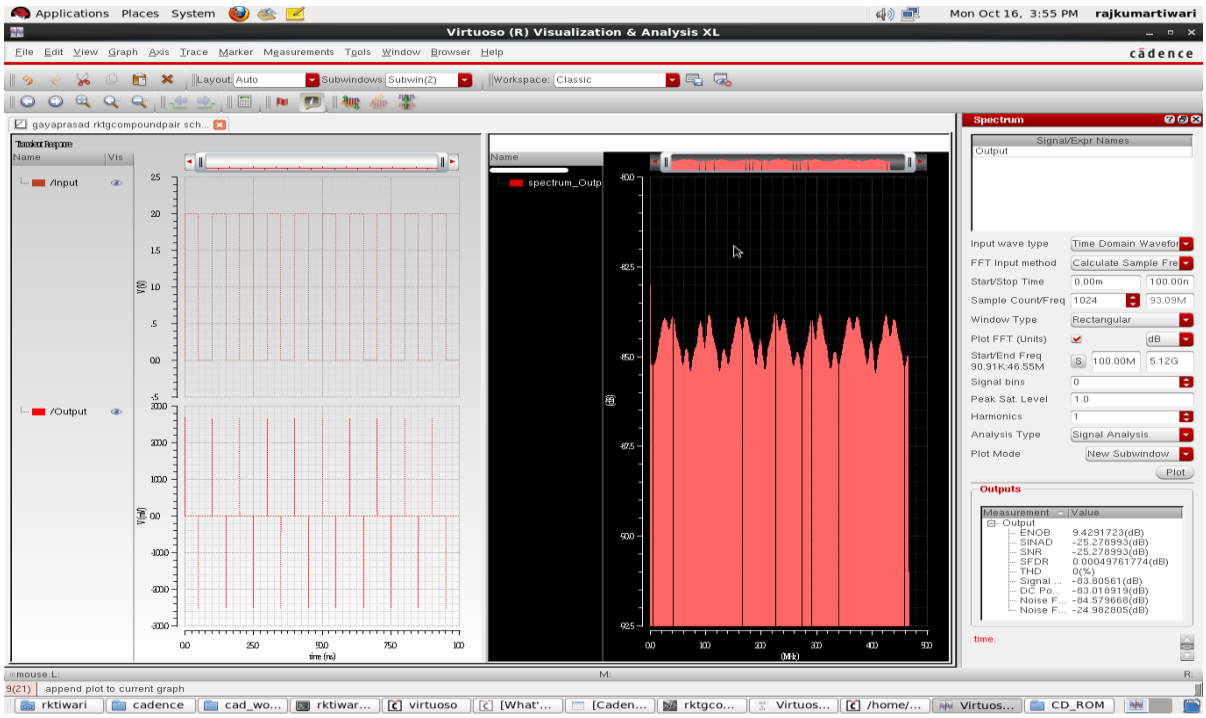

Fig.2 Transient analysis of CMOS Compound pair amplifier

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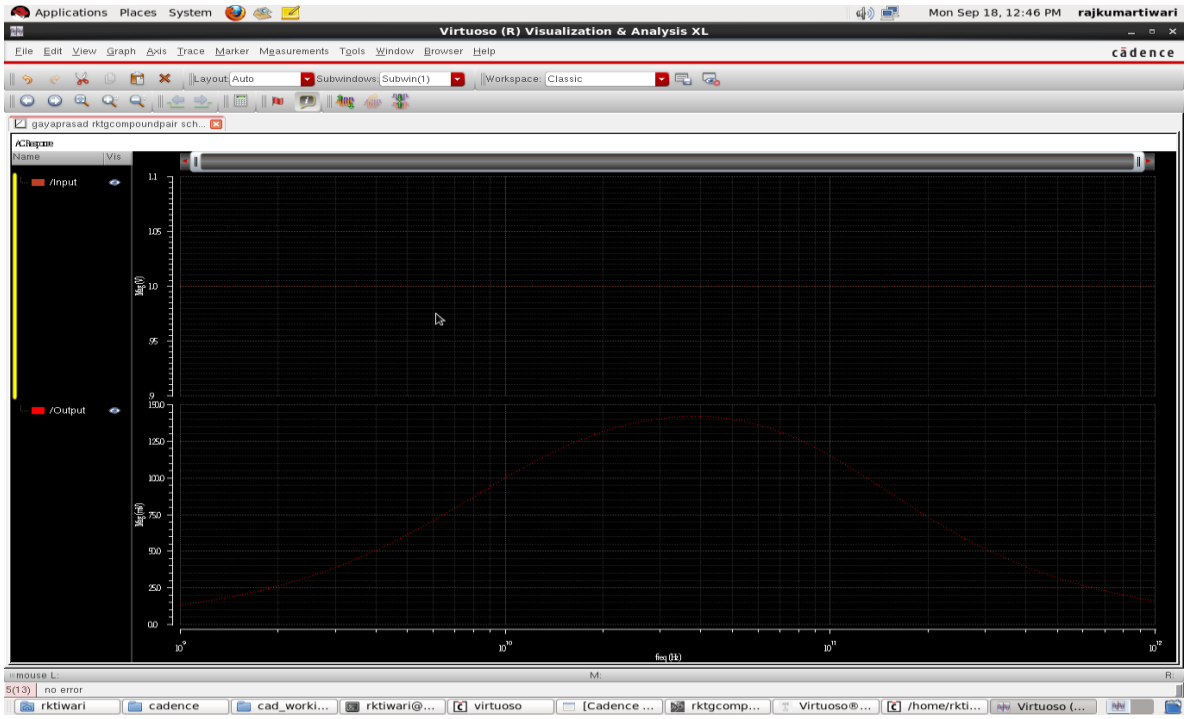

Fig.3 A.C. Analysis of CMOS Compound pair amplifier

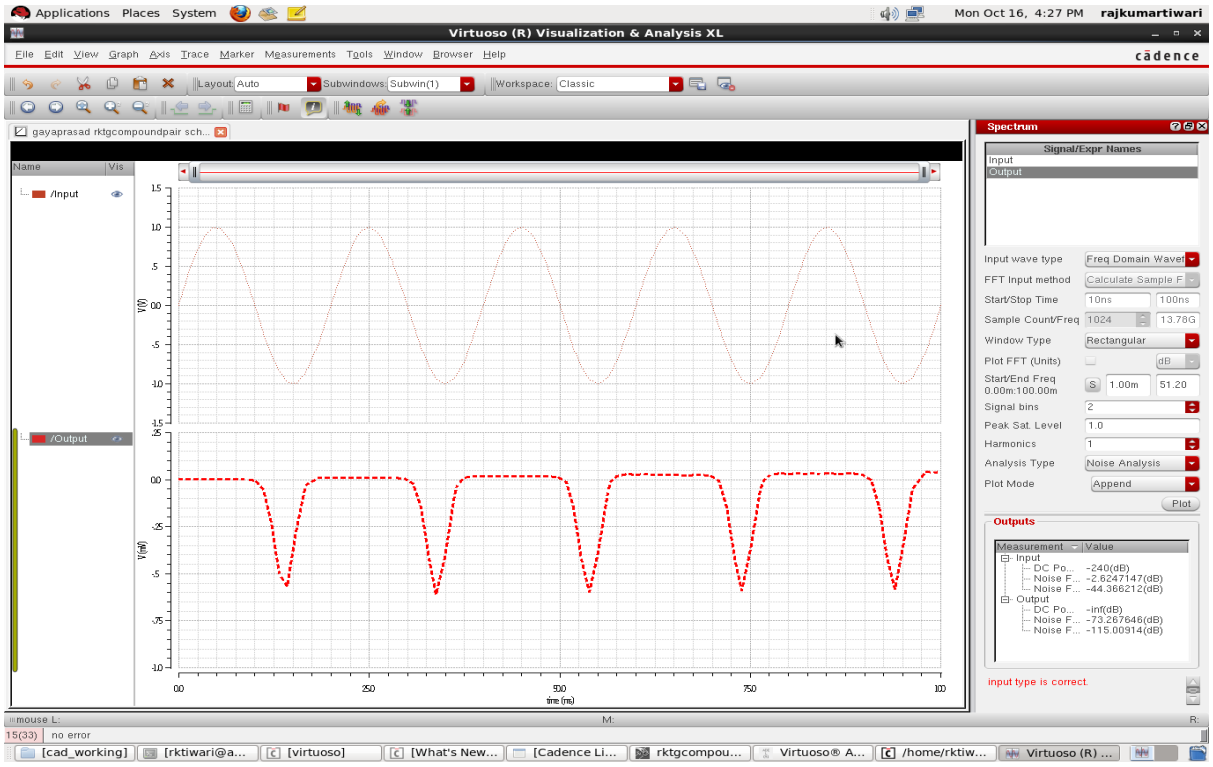

Fig.4 Transient analysis of CMOS compound pair amplifier with sine wave.

Proposed CMOS compound pair amplifier circuit provide better response of transient analysis with pulse wave at low input voltage as shown in fig.2. The AC analysis of the compound pair amplifier at high frequencies shown in fig.3, it shows that the circuit work as a wide band circuit at high frequency. This circuit also work as a radio frequency amplifier. Circuit play an important role with sine wave at various frequency ranges and give better response as shown in fig.4. This circuit shows excellent temperature stability in the temperature range -50, 27 and 100˚ C. Fig. 5 shows the comparative study of the compound pair amplifier at various values of inductor. The value of voltage gain shifted from high frequency range to low frequency range with the value of inductance 10nH to 10H respectively. The important outcome of the present study is that one can use proposed new CMOS compound pair amplifier circuit for very high (Terahertz reason) frequency as well as for very low frequency with proper choice of inductance. Table1 shows the voltage gain of proposed CMOS compound pair amplifier at various values of inductor at output capacitor 10µf.

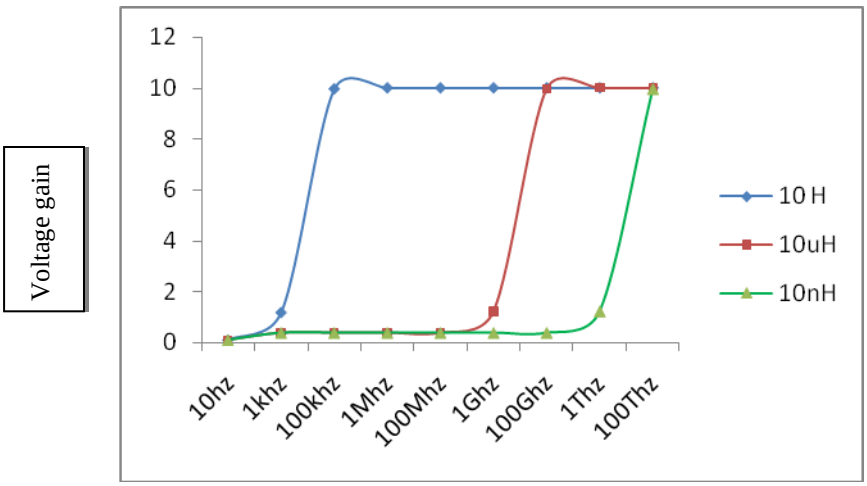

Fig.5 voltage gain of proposed circuit with various value of inductor at Co=10µf.

IV. TABLE

L	10hz	1khz	100khz	1Mhz	100Mhz	1Ghz	100Ghz	1Thz	100Thz
10 H	0.085	1.17	9.961	10	10	10	10	10	10
10uH	0.085	0.368	0.368	0.369	0.369	1.206	9.96	10	10
10nH	0.085	0.368	0.368	0.368	0.368	0.368	0.368	1.208	9.96

Table:1 Voltage gain at various values of Inductor.

V. CONCLUSION

From above discussion it is concluded that the proper choice of the circuit element play an important role to make CMOS compound pair amplifier with inductor more flexible and versatile. Due to high voltage gain and wide band proposed circuit can be used as voltage amplifier for low voltage and high frequency applications and communication module. As the proposed CMOS compound pair amplifier circuit is working at 1.8uVac so present proposed CMOS Compound pair amplifier can be also used to design low voltage high speed reversible logic devices. Circuit shows excellent temperature stability in the temperature range -50, 27 and 100° C. Due to its property of low power dissipation, such devices are capable to design reversible quantum computing electronic devices. This is demand of coming future reversible technology.

VI. ACKNOWLEDGMENT

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