International Journal of Advance Research in Science and Engineering
Volume No.07, Special Issue No. (01), January 2018
www.ijarse.com
IJARSE
ISSN: 2319-8354

DESIGN AND IMPLEMENTATION OF EFFICIENT LOW POWER POSITIVE FEEDBACK ADIABATIC LOGIC

Indumathi.S[1], Aarthi.C[2]

[1]PG Scholar, VLSI Design, Sengunther Engineering College, (India)

[2]Associate Professor, Dept of ECE, Sengunther Engineering College, (India)

ABSTRACT

The continuously growing quest for miniaturization of circuit technology, one of the prime focuses of the research has shifted in the direction of ultra low power circuit designs. Over the years, adiabatic circuit designs have been studied and found to be effective in achieving low power in VLSI circuits. The project can explain some of the adiabatic logic families such as ECRL, 2N-2N2P and PFAL. And presents a new adiabatic logic circuit based on PFAL logic family. The aim of project is comparing the effectiveness of proposed adiabatic logic circuit, in terms of power dissipation, over other adiabatic logic families by simulating different logic gates using these logic families. All the simulations are done using LTSPICE tool and HSPICE Simulator at 65nm technology at 500MHz and 1GHz frequency range. Comparative results are presented at different frequencies, which show least power dissipation for the proposed logic circuit.

Keywords—Adiabatic circuit, Low power, ECRL,PFAL,2N-2N-2P

I.INTRODUCTION

This template, modified in MS Word 2007 and saved as a "Word 97-2003 Document" for the PC, provides authors with most of the formatting specifications needed for preparing electronic versions of their papers. All standard paper components have been specified for three reasons: (1) ease of use when formatting individual papers, (2) automatic compliance to electronic requirements that facilitate the concurrent or later production of electronic products, and (3) conformity of style throughout a conference proceedings. Margins, column widths, line spacing, and type styles are built-in; examples of the type styles are provided throughout this document and are identified in italic type, within parentheses, following the example. Some components, such as multi-leveled equations, graphics, and tables are not prescribed, although the various table text styles are provided. The formatter will need to create these components, incorporating the applicable criteria that follow.

Complementary metal oxide semiconductor, abbreviated as CMOS is a technology for constructing integrated circuits. CMOS technology is used in micro processors, micro controllers, static RAM and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters and highly integrated transceivers for many types of communication.

CMOS is also referred to as complementary symmetry metal oxide semiconductor (COS-MOS). The word "Complementary symmetry" refer to the fact that the typical design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or N-type metal-oxide-semiconductor logic (NMOS) logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in Very-large-scale integration (VLSI) chips.

CMOS circuits are constructed in such a way that all P-type metal-oxide-semiconductor (PMOS) transistors must have either an input from the voltage source or from another PMOS transistor. Similarly, all NMOS transistors must have either an input from ground or from another NMOS transistor.

The composition of a PMOS transistor creates low resistance between its source and drain contacts when a low gate voltage is applied and high resistance when a high gate voltage is applied. On the other hand, the composition of an NMOS transistor creates high resistance between source and drain when a low gate voltage is applied and low resistance when a high gate voltage is applied. CMOS accomplishes current reduction by complementing every N MOSFET with a P MOSFET and connecting both gates and both drains together. A high voltage on the gates will cause the N MOSFET to conduct and the P MOSFET to not conduct, while a low voltage on the gates causes the reverse. This arrangement greatly reduces power consumption and heat generation.

However, during the switching time, both MOSFETs conduct briefly as the gate voltage goes from one state to another. This induces a brief spike in power consumption and becomes a serious issue at high frequencies.

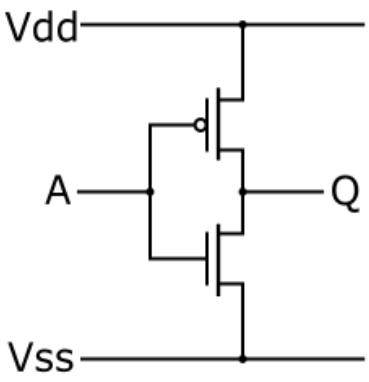

Fig. 1 Static CMOS inverter

Consider above Static CMOS inverter, when an input is connected to both a PMOS transistor (top of diagram) and an NMOS transistor (bottom of diagram). When the voltage of input A is low, the NMOS transistor's channel is in a high resistance state. This limits the current that can flow from Q to ground. The PMOS transistor's channel is in a low resistance state and much more current can flow from the supply to the output. Because the resistance between the supply voltage and Q is low, the voltage drop between the supply voltage and Q due to a current drawn from Q is small. The output, therefore, registers a high voltage.

On the other hand, when the voltage of input A is high, the PMOS transistor is in an OFF (high resistance) state so it would limit the current flowing from the positive supply to the output, while the NMOS transistor is in an ON (low resistance) state, allowing the output from drain to ground. Because the resistance between Q and ground is low, the voltage drop due to a current drawn into Q placing Q above ground is small. This low drop results in the output registering a low voltage. In short, the outputs of the PMOS and NMOS transistors are complementary such that when the input is low, the output is high, and when the input is high, the output is low. Because of this behaviour of input and output, the CMOS circuit's output is the inverse of the input. The power supplies for CMOS are called V_{DD} and V_{SS}, or V_{CC} and Ground (GND) depending on the manufacturer. V_{DD} and V_{SS} are carryovers from conventional MOS circuits and stand for the drain and source supplies. These do not apply directly to CMOS, since both supplies are really source supplies.

V_{CC} and Ground are carryovers from TTL logic and that nomenclature has been retained with the introduction of the 54C/74C line of CMOS.

As the advancement in technology continues over the years, transistors have reached to atomic size. This reducing size and continuously increasing integration density, however, concerns the designers with the increasing power dissipation. A number of techniques have already been proposed for reducing power dissipation.

The two important types of power dissipation in VLSI circuits are,

1) Static power dissipation and

2) Dynamic power dissipation.

While static power dissipation is due to internal leakages in devices during the off state of a circuit, dynamic power dissipation is because of the energy loss during charging and discharging of the output node capacitance of a transistor when switching takes place. Lately, dynamic power dissipation has been the primary concern of designers. Different technologies have been introduced over the years which are sub-threshold logic, multi-threshold logic and adiabatic logic circuit. Adiabatic logic, a promising alternative to CMOS, is a novel low power circuit technology. The term ‘adiabatic’ comes from ‘thermodynamics’, which describes a process wherein which no energy exchange with the environment, and hence, no dissipation energy loss takes place. Whereas in semiconductor devices, the transfer of charge between different nodes is the process of energy exchange and different techniques can be utilized so as to minimize this energy loss due to charge transfer.

International Journal of Advance Research in Science and Engineering
Volume No.07, Special Issue No. (01), January 2018
www.ijarse.com
IJARSE
ISSN: 2319-8354

While fully adiabatic operation would be the ideal condition of a circuit operation, in practical cases partial adiabatic operation of circuit gives acceptable performance without much complexity.

II.EXISTING METHODOLOGY

A. Adiabatic Logic Family

Adiabatic Logic is the term given to low-power electronic circuits that implement reversible logic. The term comes from the fact that an adiabatic process is one in which the total heat or energy in the system remains constant. Research in this area has mainly been fuelled by the fact that as circuits get smaller and faster, their energy dissipation greatly increases a problem that adiabatic circuits promise to solves. Adiabatic logic can be achieved by ensuring that the potential across the switching devices is kept small. This can be achieved by charging the capacitor from a time-varying voltage source or constant current source. Here, R represents the resistance of the PMOS network. A constant charging current corresponds to a linear voltage ramp. Assuming that the capacitance voltage V_c is 0 initially. The variation of the voltage as a function of time can be found as,

$V_c(t) = (I_s . t) / 2$

Then, Charging current $I_s = (C . V_c(t)) / 2$

B. Types Of Adiabatic Logic Families

Most research has focused on building adiabatic logic out of CMOS. However, current CMOS technology, though fairly energy efficient compared to similar technologies, dissipate energy as heat, mostly when switching. Several designs of adiabatic CMOS circuits have been developed. Adiabatic logic circuits are also use current nano-materials such as silicon nano wires or carbon nano tubes since nano-electronics are expected to dissipate a great amount of heat.

There are 2 types of adiabatic logic families:

1. Fully adiabatic logic family.
2. Quasi adiabatic logic family.

Fully adiabatic logic:

Fully adiabatic logic family circuits lose their energy due to leakage currents through non-ideal switches.

Quasi adiabatic logic:

Quasi adiabatic logic family circuits suffer from the non-adiabatic energy loss in some regions of operations that is usually proportional to the capacitance driven and the square of the threshold voltage. There are following classified families of adiabatic logic:

1. Positive Feedback Adiabatic Logic.
2. Efficient Charge Recovery Logic.
3. Adiabatic 2N-2N2P Logic.

International Journal of Advance Research in Science and Engineering
Volume No.07, Special Issue No. (01), January 2018
www.ijarse.com
IJARSE
ISSN: 2319-8354

C. Positive Feedback Adiabatic Logic

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery. The general schematic of the PFAL gate is shown in Figure 2. The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS M1-M2 and two NMOS M3-M4, that avoids a logic level degradation on the output nodes out and /out. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs.

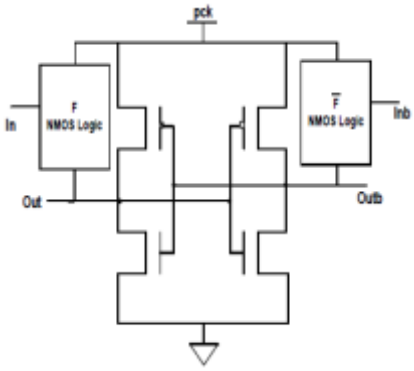

Fig. 2 Basic structure of Positive Feedback Adiabatic Logic (PFAL)

The functional blocks are in parallel with the PMOSFETs of the adiabatic amplifier and form a transmission gate. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs.

D. PFAL Based NOT Gate

The inverter (NOT circuit) performs the operation called inversion or complementation. The NOT operation changes one logic level to the opposite logical level. When the input is Low, the output is high. When the input is high, the output is low. The inverter changes one logic level to the opposite level. In terms of bits, it changes a 1 to a 0 and 0 to 1. When a High level is applied to an inverter input, a low level will appear on its output. When a low level is applied to its input, a High will appear on its output. PFAL based NOT gate is shown in figure 3.

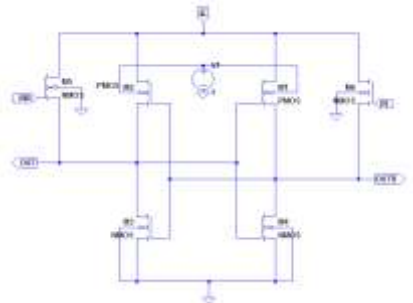

Fig. 3 Schematic diagram of PFAL based Inverter

International Journal of Advance Research in Science and Engineering
Volume No.07, Special Issue No. (01), January 2018
www.ijarse.com
IJARSE
ISSN: 2319-8354

E. PFAL Based NAND Gate

NAND gate is an electronic circuit which has two or more inputs but only one output. The NAND gate is the natural implementation for the simplest and fastest electronic circuits. The output is HIGH if at least one of its inputs is LOW. The output is LOW only when all the inputs are HIGH. The term NAND is a contraction of NOTAND. The NAND gate is a combination of an AND gate followed by NOT gate. For 2 input NAND gate, two NMOS transistors connected in series is taken as pull down network and two PMOS transistors connected in series is taken as pull up network. PFAL based NAND gate structure.

This circuit works similar to CMOS technology based circuit and also reduces power by recycling the energy instead of discharging it to ground.

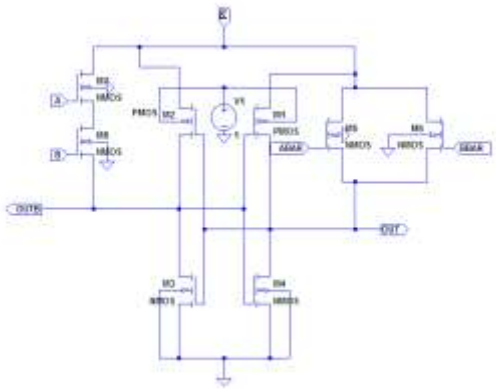

Fig. 4 Schematic diagram of PFAL based NAND Gate

F. Efficient Charge Recovery Logic

Efficient charge recovery logic consists of two cross couple PMOS transistors in the pull up section where as the pull down section is constructed with a tree of NMOS transistors. Its structure is similar to Cascade Voltage Switch Logic (CVSL) with differential signalling. The logic function in the functional block can be realized with only NMOS transistors in the pull down section. The basic inverter in ECRL logic can be constructed as shown in figure 5 and 6.

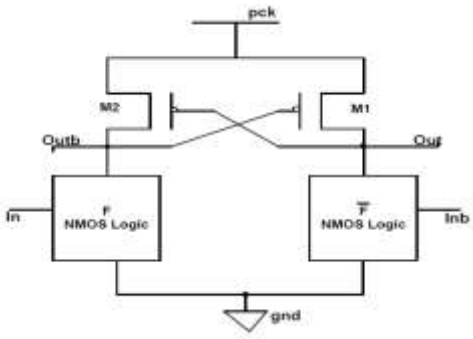

Fig. 5 Basic structure of Efficient Charge Recovery Logic (ECRL)

International Journal of Advance Research in Science and Engineering
Volume No.07, Special Issue No. (01), January 2018
www.ijarse.com
IJARSE
ISSN: 2319-8354

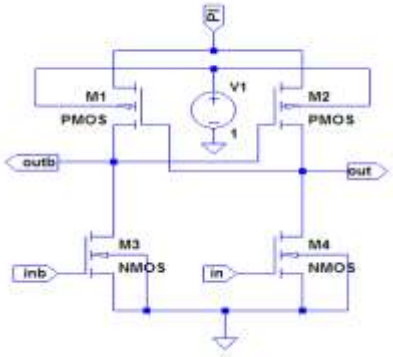

Fig. 6 Schematic diagram of ECRL inverter

The schematic of ECRL inverter, NMOS transistors N1 and N2 implement the inverter logic whereas P1 and P2 allow the output nodes to discharge into the 'VCLK'. Assuming that the 'in' signal is at logic high and 'in' is at logic low, when the power-clock supply 'VCLK' rises from o to VDD, voltage at 'out' remains at VSS i.e. low due to switching ON of the N1 transistor. The voltage at the 'out' node capacitance follows the 'VCLK' signal. When the power-clock reaches VDD level, the outputs hold valid logic levels. These values are maintained during the hold phase. After the evaluation or hold phase, the 'VCLK' falls down to a ground level, the 'out' node capacitance discharges adiabatically into the power-clock supply recovering the energy. Again like CAL logic style, N1 and N2 can be replaced with NMOS logic trees to perform switching involved in the evaluation of an arbitrary binary function is shown in figure 7.

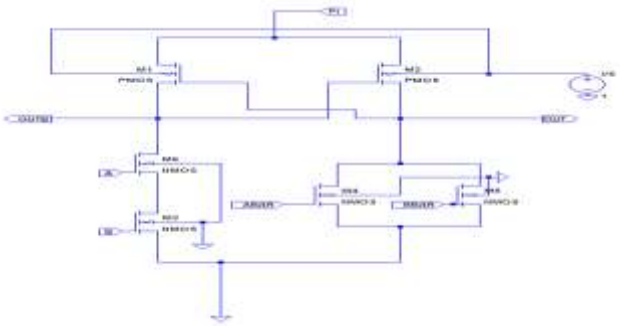

Fig.7 Schematic diagram of ECRL NAND

III.PROPOSED METHODOLOGY

The circuit is similar to the PFAL logic circuit with the latch comprising of two PMOS transistors and two NMOS transistors. And the NMOS logic functional blocks are connected in parallel with the PMOS transistors of the latch forming the transmission gates similar to PFAL logic. The difference lies in the pull-down block. An NMOS transistor forming a diode and a DC voltage source connected between the pull-down NMOS transistors and the ground. The diode connected at the bottom of NMOS tree acts as an active load which provides a high impedance path to the power clock.

International Journal of Advance Research in Science and Engineering
Volume No.07, Special Issue No. (01), January 2018
www.ijarse.com
IJARSE
ISSN: 2319-8354

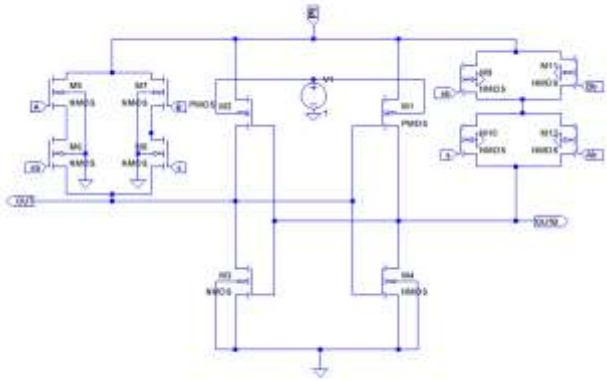

Fig. 8 Schematic diagram of 2:1MUX using conventional PFAL

Thus it controls the discharging path by reducing the rate of discharge of internal nodes of the logic circuit. And the positive DC voltage source is connected between the diode and the ground, to further incorporate the advantage of level shifting technique in the proposed logic circuit. Level shifting technique reduces the gate to source voltage at the output transistors and thus reduce gate current and leakage current, providing further lower power dissipation as compared to conventional PFAL logic family.

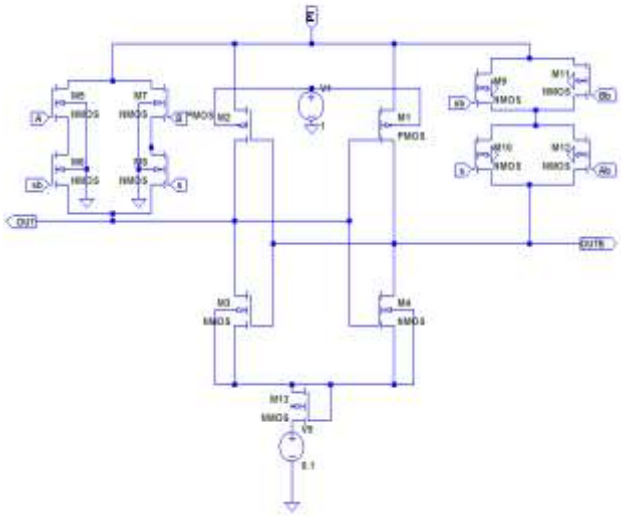

Fig. 9 Schematic diagram of 2:1 MUX using proposed DCDB-PFAL

Different logic gates are implemented using adiabatic logic families discussed in this paper and then by using the proposed DCDB-PFAL logic circuit. Finally a combinational logic circuit, 2:1 MUX, has been implemented using conventional PFAL and proposed DCDB-PFAL logic. Circuit diagram for both are shown in figures 8 and 9.

International Journal of Advance Research in Science and Engineering
Volume No.07, Special Issue No. (01), January 2018
www.ijarse.com
IJARSE
ISSN: 2319-8354

IV.SIMULATION AND RESULTS

In order to see the effectiveness of proposed DCDBPFAL logic circuits over existing adiabatic logic families discussed above, different logic gates have been simulated, first using existing adiabatic logic families (ECRL, 2N-2N2P, PFAL) and then by using proposed DCDB-PFAL logic as discussed in this paper. Finally, 2:1 multiplexer circuit is implemented and calculations are done for effectiveness in terms of power dissipation between them, at different operating frequencies and at different values of DC voltages for the voltage source connected in the proposed logic. All the simulations are done using HSPICE Simulator at '65nm' technology.

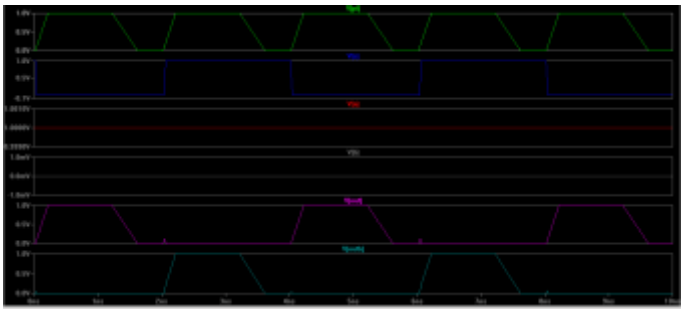

Fig.10 Waveform of PFAL 2:1 MUX

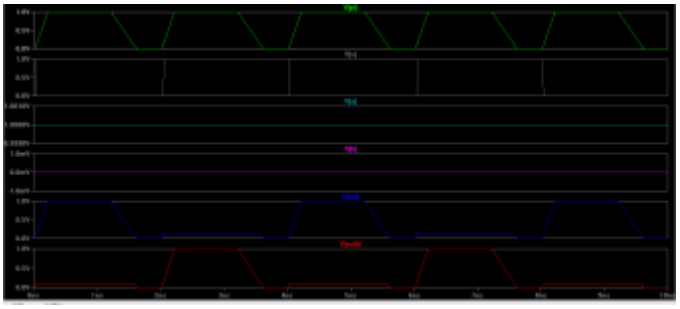

Fig. 11 Waveform of proposed DCDB PFAL 2:1 MUX

TABLE I. ANALYSIS OF ENERGY AND POWER IN ECRL, 2N-2N2P AND PFAL INVERTERS WITH PROPOSED DCDB-PFAL INVERTER

Parameter	Adiabatic Inverter Circuits			
	2N-2N2P	***ECRL***	***PFAL***	***Proposed DCDB-PFAL***
Energy	-11.072pJ	-6.132pJ	-10.098pJ	-5.2078 pJ
Power	-22.231nW	-12.286 nW	-20.177 nW	-10.606 nW

TABLE II. ANALYSIS OF ENERGY AND POWER IN ECRL, 2N-2N2P AND PFAL INVERTERS WITH PROPOSED DCDB-PFAL INVERTER

Parameter	Adiabatic Inverter Circuits			
	2N-2N2P	***ECRL***	***PFAL***	***Proposed DCDB-PFAL***
Energy	-9.391pJ	-7.1191pJ	-10.454pJ	-6.1768pJ
Power	-18.8nW	-14.536nW	-20.892nW	-12.348nW

TABLE III. COMPARISON OF ECRL, 2N-2N2P AND PFAL NAND WITH PROPOSED DCDB-PFAL NAND

Parameter	Adiabatic MUX Circuits	
	PFAL	**Proposed DCDB-PFAL**
Energy	-17.204pJ	-8.083pJ
Power	-34.414nW	-16.392nW

V.CONCLUSION

In this work, undergoes different adiabatic logic families. Different logic gates have been implemented using different logic families and using proposed DCDB-PFAL logic at different frequencies and for different values of dc voltages for the new logic circuit. Finally a combinational circuit 2:1 MUX has also been implemented for the proposed and the conventional logic. From the simulation of existing logic families we have seen that PFAL logic family provides much lower power dissipation as compared to ECRL and 2N-2N2P logic family. And from the simulations carried out in this paper we have seen that the proposed DCDB-PFAL logic circuits it offers significant power reduction over all other logic families and achieves even better performance and much lower power dissipation than PFAL logic family. It can be seen from different graphs plotted, that as the dc voltage is varied between 0.1V to 0.3V, power first decreases up till around 0.25V and then increases gradually. The proposed DCDB-PFAL logic can be used in devices which need ultralow power for their working such as hearing machine, pacemaker and other medical purpose devices. As the quest for ultra-low power circuit designs goes on increasing, these improved circuit technologies would prove to be very useful in serving the need for ultra low power circuit designing.

REFERENCES

[1] M.L. Keote, P.T. Karule, "Design and Implementation of Energy Efficient Adiabatic ECRL and Basic Gates," International Conference on Soft Computing Techniques and Implementations- (ICSCTI), Oct 8-10, 2015.

[2] K. Roy and Y.Ye," Low Power Circuit Design using Adiabatic Switching Principle", ECE Technical Reports, Purdue University, Indiana, as accessed on April, 2013.

[3] Y. Moon and D.K. Jeong, "An efficient charge recovery logic circuit," IEEE Journal of Solid-State Circuits, Vol. 31, 1996, pp. 514-522 as accessed on October, 2014.

[4] S.K. Kelly and J.L. Wyatt, "A Power Efficient Neural Tissue Stimulator with Energy Recovery," IEEE Transactions on Biomedical Circuits and Systems, Vol.5, No. 1, pp. 20-29, Feb. 2011.

[5] D. Shinghal, A. Saxena and A. Noor, "Adiabatic Logic Circuits: A retrospective," MIT International Journal of Electronics and Communication Engineering, Vol. 3, No. 2, pp. 108–114, August 2013.

[6] S.P. Kushawaha and T.N. Sasamal, "Modified Positive Feedback Adiabatic Logic for Ultra Low Power VLSI," IEEE International Conference on Computer, Communication and Control (IC4-2015).

[7] R. Singh, A. Sharma and R. Singh, "Power Efficient Design of Multiplexer based Compressor using Adiabatic Logic," International Journal of Computer Applications (0975 – 8887), Vol. 81, No. 10, pp.75-87.

[8] B. H. Calhoun, S. Khann and R. Mann, "Sub-threshold circuit design with shrinking CMOS devices," IEEE International Symposium on Circuits and Systems, Taipei, pp. 2541–2544, 2009.

[9] S. Hemantha, A. Dhawan and K. Haranath, "Multi-threshold CMOS design for low power digital circuits," 2008 IEEE Region 10 Conference on TENCON, pp. 1-5, Hyderabad, 2008.

[10] Minakshi Sanadhya and Vinoth Kumar.M, "Recent Development in Efficient diabatic Logic Circuits and Power Analysis with CMOS Logic", 2015 Elsevier International Conference on Recent Trends in Computing, pp. 1299 – 1307.

[11] Arpan Chaudhuri, Mamia Saha and Moumita Bhowmik, "Implementation of Circuit in Different Adiabatic Logic", 2015 IEEE International Conference on Electronics and Communication System (ICECS 2015), pp.353-359.

[12] Pragati Upadhyay and Vishal Moyal, "Implementation of Low Power Inverter using Adiabatic Logic", 2016 International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 5, Issue 6, pp.4521-4527.

[13] Anu Priya and Amrita Rai, "Adiabatic Technique for Power Efficient Logic Circuit Design", 2014 International Journal of Electronics & Communication Technology, IJECT Vol. 5, Issue Spl-1, pp.70-78.

[14] Bhakti Patel and Poonam Kadam, "Comparative Analysis of Adiabatic Logic Techniques", 2015, International Conference on Computer Technology, pp.20-24.