International Journal of Advance Research in Science and Engineering
Volume No.06, Special Issue No.(01), December 2017
www.ijarse.com
IJARSE
ISSN: 2319-8354

DESIGN OF LOW POWER ELECTRONICS CIRCUIT FOR VLSI APPLICATION

Malik Aziz Ullah[1] , Dr. R.P. Singh[2]

[1]Research Scholar, Sri Satya Sai University of Technology and Medical Sciences, (India)

ABSTRACT

A conventional CMOS logic circuit design approach depends upon charging the output capacitive nodes to the supply voltage or discharging it to the ground. This is one of the most used methods in VLSI designs. There are various techniques to design low power circuits both at system level as well as at circuit level to reduce power consumption. One of the major sources of power dissipation is the charging and discharging of capacitor. Every time when a capacitor is discharged to ground, an amount of energy = ½ C stored in the capacitor is lost. We can reduce this power dissipation by restoring this energy to the source instead of discharging to the ground.

Another way of reducing the power dissipation is to design the circuit in such a way that the charging of the capacitive node takes place very slowly. It has been observed that by charging the capacitor slowly, the energy require is lesser than faster charging method. Adiabatic circuits use the above two methods viz. slow charging of capacitor and discharging, and recycling of charge to minimize the power consumed. Several Adiabatic designs have been designed and tested in this paper.

Most of them achieve significant power savings in comparison to conventional CMOS designs. The major drawbacks of these circuits include complex design for achieving simple operations, requirement of multiple clocks and requirement of complimentary input signals for controlling the charging and discharging process. The Current work is based on an existing adiabatic logic style known as PFAL (Positive Feedback Adiabatic Logic) and ECRL (Energy Efficient Charge Recovery Logic) which are simple and doesn't require complimentary signals or complex clocking.

"In the last few decades due to the ever growing demand for portable and small sized devices, integrated circuits require electronic circuit design methods to implement integrated circuits with low power consumption. The ever-growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude.

Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems." If we want a design for low-power consumption to be successful, it is important

to have a thorough understanding of the sources of power dissipation, the factors that affect them, and the methodologies and techniques that are available to achieve optimal results. Therefore, this thesis starts with the sources of power dissipation in a integrated circuit. We present —we believe— the most important low-power methodologies and power optimization techniques available. Low-power design can be applied on various different levels, such as the architectural level, the gate level, and the technology level.

Apart from that, also a number of alternative logic-design styles are presented to report on their characteristics regarding power consumption. This chapter could as well be utilized by others as a quick study in the field of low-power/power-aware design. Passive losses due to leakage currents are in focus with on-going shrinking of microelectronic circuits. Power-gating does not supply power to the inactive circuits from the power supply.

Uncritical paths within a complex system can be equipped with higher devices, allowing for a trade-off of speed for passive losses. Apart from these circuit level methods to reduce leakage losses also new transistor models are presented to minimize leakage losses in circuits. Adiabatic Logic technique is one of the best circuit design methods to reduce energy consumption in different operations. Analysis on the gate level suggests a major cutdown of losses in adiabatic logic as compared to static CMOS. Out of a large numbers of adiabatic topologies only a few satisfy our requirements , as those are compatible to a static CMOS design flow and robust with respect to P-V-T variation and apply a manageable number of clocked power supplies that can be generated in an energy efficient manner.

The reduction in size of the circuit can also save energy by a large magnitude. As the gate capacitance depends upon the size of transistor, by scaling down the transistor size also scales down the gate capacitance which ensures a reduction in power consumption, but the current drive of the logic gates are also affected by decreasing the size which can be a major source in slowing down the operation.

Power consumption in the circuit is proportional to the switching frequency of the circuit and also on the load capacitance. This is valid for every signal path present in a system, whether it is a clock signal, a data pin, or an address line. Hence we can reduce the power consumption by reducing the number of transition occurring. So a correct choice of the number representation can have a great impact on the switching activity.

Significant power saving can be achieved by using a gray code as minimum changes occur in gray code as compared to BCD or any other representation. Many such coding techniques have been reported that results in different power savings. To reduce activity in synchronous logic clock gating is used. Clock gating is done by a control signal applied to a logic block; when some particular blocks are not in use clock signal is not supplied to them, this helps in reducing the clock signal activity and thus decrease the power consumption. Since power lost due to clock signal activity is substantially high this method saves a considerable amount of energy. This technique can be also be used to other signals which contributes to high power dissipation.

II STATEMENT OF THE PROBLEM

The current study is done to analyze the Design of low power electronics circuit for VLSI application.

III LIMITATIONS REVIEW

1. The study was delimited to analyze the Design of low power electronics circuit for VLSI application.
2. The study was also de-limited to VLSI.

The facts discussed in this study were based entirely on the responses to the questionnaire therefore, ascertaining the genuineness of the responses was identified as the limitation of the study.

IV HYPOTHESIS

On the basis of research finding, literature reviews, expert opinion and scholar's own understanding of the problem, it was hypothesized that the VLSI is efficient for low power electronics.

V EXPLANATION

Leakage current

Leakage components of current are always present in CMOS circuit even if the no switching activity is present. This is a major contributor in power dissipation for small sized device. In current days technologies the leakage current is a major source of power dissipation.

Sleep transistor

Supply gating or “sleep transistor” is an effective method used to reduce both active and standby leakage power. It follows the same concept as clock gating technique, a high threshold value transistor is used in gating the power supply.

VI SIGNIFICANCE OF THE STUDY

The power supply is not provided to the logic blocks which are in OFF mode. We can scale down the leakage current by a factor of up to 1000 by using this method. There are several limitations to this method. The high threshold value transistor decreases the performance of the circuit. Again the virtual supply rails tend to decrease the noise immunity level. We need to design a local power grid for the supply rails so that the logic states won’t change when the virtual supplies fail.

Two main parts of an adiabatic system are (i) Digital core design made up of adiabatic gates and the power-clock signal generator. We have used two adiabatic families in this paper. The most important aspect of the adiabatic system is clock-signal generation, High saving factors can be achieved by an optimal generation of four-phase power-clock. " Two adiabatic logic families are discussed in the current paper, one is Positive Feedback Adiabatic Logic (PFAL) and the other is the Efficient Charge Recovery Logic (ECRL). Both operate in the same four-phase power-clock supply.

VII OBJECTIVES OF THE STUDY

Objectives of the current research work are as follows:

1) To examine the VLSI application.

2) To study the low power electronics circuit.

3) To study the Design of low power electronics circuit for VLSI application.

VIII REVIEW

Zallen et al. (2013)[1] described that for the electrical measurements, specimens in the form of squares, 30x30 mm2 were cut from the composite blocks with a thickness of about 3 mm. Three identical samples for each filler concentration utilized for measuring electrical resistivity/conductivity.

Kirkpa et al. (2013)[2] described that Copper electrodes with silver coating on the surfaces of electrodes were used in order to ensure a good electrical contact with samples. The samples employed for electrical measurements were in form of square blocks, which were sandwiched between circular copper electrodes.

Lux et al. (2013)[3] described that the D.C. volume (bulk) conductivity of samples was measured with two point method as resistivity of specimens is enough high, employing Alternating Polarity Test, which is a novel technique to measure the high resistance with excellent repeatability compare to conventional two point method in literature.

Avrom et al. (2006)[4] described that the electrical leads from the meter were fixed to copper rods of designed assembly for electrical conductivity measurements, which is very close to ASTM D257 for measurement of high resistance.

Suvrna et al. (2010)[5] described that the Alternating Polarity Resistance/Resistivity test is designed to improve high resistance/resistivity measurements. These measurements are prone to large errors due to background currents. By using an alternating stimulus voltage, it is possible to eliminate the effects of these background currents. When this test is run, the V-Source will alternate between two voltages (V-OFS + V-ALT) and (V-OFS - V-ALT) at timed intervals (measurement-time).

Mazain et al. (2005)[6] described that current measurements are taken at the end of each of these alternations and after calculation of Icalc resistance values are computed. Icalc is a weighted average of the latest four current

measurements, each at the end of a separate alternation. The resistance value is then converted to a resistivity value if the meter has been configured for resistivity measurements.

Liu et al. (2006)[7] described that experimental study of A.C. electrical conductivity measurements may provide valuable information about the conduction mechanisms of epoxy/chopped carbon fiber (CCF) composites. The values of these effects can be understood from the variation in electrical conductivity with frequency. The range of the frequency that of concern to this work is 102 -106 Hz in controlled environment.

Abdallah et al. (2012)[8] described that to study and measure the effect of CCF wt% and frequency of applied electric field on the A.C electrical conductivity of epoxy/CCF composite HP 4284A programmable multi-frequency LCR meter is used with LABVIEW software in controlled environment.

Psarras et al. (2013)[9] described that the sample holder is situated with two copper electrodes having silver coating on the surfaces of electrodes to ensure better electrical contact with specimens was used. Samples were sandwiched between silver coated copper electrodes having 1cmx1cmarea. The high and low specimen holder terminals were connected to multifrequency LCR Meter (model HP-4284A).

Donnelly et al. (2013)[10] described that application of a high voltage can irreversibly decrease the resistivity. As was mentioned above, a polymer layer exists between filler particles and/or their agglomerates. Therefore an electrical current usually flows in the composite through the agglomerates separated by the polymer gaps. It should be noted that voltage across the gap is expected to be higher than the macroscopic voltage, V, by a factor, M, equal to the ratio of the average size of the conducting aggregate to the average gap width.

Brown et al. (2014)[11] described that if the factor M or voltage V is large enough, dielectric breakdown can take place. This phenomenon was observed for polymer composites filled with carbon black. The average size of the conductive agglomerates in these composites was approximately 1 μm.

Sun et al. (2012)[12] described that there is a distribution of the inter-fiber contacts by the gap width as was discussed in literature. Some of the fibers are in direct contact with each other whereas others are separated. “Direct contact” means that there are no polymer gaps between adjacent fibers.

Pham et al. (2013)[13] described that because the fiber diameter is one order of magnitude greater than the agglomerate size in composites a larger voltage can exist across the gap in composites. If this voltage is great enough it can result in local dielectric breakdown of the polymer layer in the gap.

Kotsilkova et al. (2005)[14] described that during dielectric breakdown, an irreversible damage in the form of carbonization of the polymer occurs which usually gives rise to the formation of a conducting pathway. So, it is most possible that the large diameter of the fibers is the main reason why local dielectric breakdown takes place in composite with carbon fibers.

Schadler et al. (2012)[15] described that the breakdown/threshold takes place at 5% of CCF loading. After breakdown phenomena resistivity of all composites irreversibly decreased. Beyond that resistivity decreases gradually. Such behaviour can be explained qualitatively as follows: in composites with a high content of CCF, most of the fibers are

in direct contact with each other and, because of this, breakdown does not decrease the resistivity value significantly.

Berriot et al. (2012)[16] described that in the composite with moderate CCF content, breakdown is more effective since a lot of the fibers are separated and breakdown generates the contacts between them. In order to clarify the type of the conduction mechanism, the current-time characteristics were studied for the composites with different weight percent content of CCF.

Xiong et al. (2013)[17] described that the Tg dependence on the CCF-content is presented in Fig. 7 for the post curing condition (75°C, 24 h). At low filler contents, Tg increases up to a maximum value (at about 7% w/w) of filler content, and afterwards decreases.

Zhang et al. (2014)[18] described that a similar behavior was observed in poly (vinyl alcohol)/clay composites. It can be qualitatively explained by the coexistence of the two mechanisms (namely interfacial constrains and free volume increase) which can be responsible for the Tg shifting. In any composite the two mechanisms are in dynamic equilibrium.

Ahmad et al. (2013)[19] described that the equilibrium point depends on many factors (filler's amount, size, etc.) and in that way it analogically affects the Tg. According to the first mechanism, a short-range, highly immobilized layer of a few nm thick is developed near the surface of the fillers. In this interaction region of the polymer layer surrounding the fillers, the conformational entropy and the chains kinetics are significantly altered.

Hussain et al. (2013)[20] described that the polymer chains in this region are under constrain because of the interfacial polymer-filler interactions and therefore Tg of the composites has been shifted to higher temperatures. Based on the concept of free volume, the increase of the filler content increases the free volume due to loosened molecular packing of the chains. This extra created free volume assists the large-scale segmental motion of the polymer.

IX PROCEDURE & STATISTICAL ANALYSIS

PFAL is designed by the cross coupling of two inverters, which is the latch element. They store the output state when the input signal gradually decreases. A cross coupled PMOS pair is used in case of ECRL based on Cathode Voltage Switch Logic (CVSL). PFAL and ECRL use logic block constructed from NMOS. Logic blocks are connected from the power clock Φ to the output nodes for PFAL and from the output to Ground for ECRL.

PFAL is a dual-rail logic family constructed using a pair of cross coupled inverters. The voltage is supplied using power-clock instead of static DC supply. This logic is constructed using NMOS devices which are attached between the power-clock and the output.

Complementary inputs are given to these NMOS transistors; this produces a low resistance between the power-clock and the asserted output. The non-asserted path is given a high impendence. When the voltage difference between

these two points is substantially high then only the operation is performed. Using this technique we can recover the outputs by using reverse-flowing data, thus we can decrease the power loss due to leakage. PFAL shows the best properties among the MOSFET only logic families.

There are several approaches to reduce the stand by leakage current like MTCMOS (Multi Threshold CMOS) and VTCMOS (Variable Threshold CMOS). These schemes cannot suppress the active leakage power. Another approach is a dual threshold voltage approach, which is to partition a circuit into critical and non critical gates and use low Vth transistors only in the critical gates. The drawback of this scheme is that the leakage current cannot be sufficiently suppressed since the large leakage current always flows through the low Vth transistors.

Processors have been able to increase clock frequency to run faster as IC circuits have become smaller. A faster clock boosts performance, but unfortunately also increases power levels. So turning off the clock, or slowing down the clock whenever excess CPU time is available can be used to reduce power levels. Many processors have hardware support to vary the clock frequency or even turn off the clock (i.e., Sleep mode).

REFERENCES

[1] R. Zallen, “The Physics of Amorphous Solids,” Chap. 4, Wiley, New York, 2013.

[2] S. Kirkpa Trick, “Percolation and Conduction”, American Physical Society, Reviews of Modern Physics, Volume 45, Issue 4, pp. 574-588, 2013.

[3] F. Lux, “Models proposed to explain the electrical conductivity of mixtures made of conductive and insulating materials”, Journal of Materials Science,Volume28, Issue 2, pp. 285-301, 2013.

[4] Avrom I. Medalia, “Electrical Conduction in Carbon Black Composites”, Rubber Chemistry and Technology, American Chemical Society: Vol. 59, Issue 3, pp. 432-454, 2006.

[5] R. Padmd Suvrna and K. Ragha, "A simple technique for a.c. conductivity measurement", Journal of Al-Nahrain University, Vol.25, Issue 7, pp.647-651, 2010.

[6] Ban Mazain Al-shabander, "Study the electrical properties for Epoxy resin reinforced with fiber glass", Department of Physics, college of science, university of Baghdad. 2005.

[7] Y. Liu and A. Gong, "Compressive Behavior and Energy Absorption of Metal Porous Polymer Composite with Interpenetrating Network Structure", Transactions of Nonferrous Metals Society of China, Vol. 16, pp.439 -4 43, 2006.

[8] M. Al-Haj Abdallah, Y. Alramadin ,M. Ahmad, A. Zihlif, S. Jawad and A. Alnajjar, “Electrical Characterization of Metal Fiber-Polyester Composite", International Journal of Polymeric Materials, Vol. 37, pp. 33 - 42, 2012.

[9] G.C.Psarras, E.Manolakaki and G.M. Tsangaris, “Dielectric dispersion and a conductivity in-Iron particles loaded polymer composites", Composites Part A: Applied Science and Manufacturing, Vol. 34, Issue 12, pp.1187-1198, 2013.

[10]Donnelly, K.P. Varlow and B.R., "Nonlinear dc and ac conductivity in electrically insulating composites" IEEE, Dielectrics and Electrical Insulation, Vol. 10, Issue 4, pp. 610-614, 2013.

[11]Brown J., Rhoney I. and Pethrick R. A.: "Epoxy resin based Nanocomposites: Diglycidil ether of bisphenol A (DGEBA) with triethylenetetramine (TETA)", Polymer International, Vol. 53, pp.2130–2137, 2014.

[12]Cao Y. M., Sun J. and Yu D. H., "Preparation and properties of nano-Al2O3 particles/polyester/epoxy resin ternary composites", Journal of Applied Polymer Science, Vol. 83, pp.70–77, 2012.

[13]Pham J. Q., Mitchell C. A., Bahr J. L., Tour J. M., Krishanamoorti R. and Green P. F., "Glass transition of polymer/single-walled carbon nanotubes composite films", Journal of Polymer Science, Part B: Polymer Physics, Vol.41, pp.3339–3345, 2013.

[14]Kotsilkova R., Fragiadakis D. and Pissis P., "Reinforcement effect of carbon nanofillers in an epoxy resin system: Rheology, molecular dynamics and mechanical studies", Journal of Polymer Science, Part B: Polymer Physics, Vol. 43, pp. 522–533, 2005.

[15] Ash B. J., Schadler L. S. and Siegel R. W., "Glass transition behavior of alumina/polymethylmethacrylateNanocomposites", Materials Letters,Vol.55,pp. 83– 87, 2012.

[16]Berriot J., Montes H., Lequeux F., Long D. and Sotta P., "Evidence for the shift of the glass transition near the particles in silica-filled elastomers", Macromolecules, Vol.35, pp. 9756–9762, 2012.

[17]Xiong M., Gu G., You B. and Wu L., "Preparation and characterization of poly (styrene butylacrylate) latex/ nanoZnOnanocomposites", Journal of Applied PolymerScience,Vol. 90, pp.1923–1931, 2013.

[18]Sun Y., Zhang Z., Moon K-S. and Wong C. P., "Glass transition and relaxation behavior of epoxy nanocomposites", Journal of Polymer Science, Part B: Polymer Physics, vol.42, pp. 3849–3858, 2014.

[19]Subcommittee Do2. Fo of Active Standard ASTM (838), "Standard Test Method for Bulk Density of As-Manufactured Carbon and Graphite Shapes", ASTM, vol.05.05, pp. 838-896, 2010.

[20]American Society for Testing and Materials; "Standard Test Method for DC Resistance of Conductance of Insulating Materials"; ASTM D257; 7CFR 1755.860(e) (5).