MOS CURRENT MODE LOGIC BASED PRIORITY ENCODERS

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ABSTRACT

This paper proposes efficient circuit realizationsfor priority encoders in MOS Current Mode logic (MCML) style. The MCML based realization of look ahead priority encoder and ripple carry priority encoder are presented. Two different realization for a particular priority encoder are given based on the series-gating approach and the fundamental cell based approach. The proposed circuits are simulated in PSPICE using 180 nm CMOS technology parameters. It is found that the proposed circuits exhibits the correct functionality. Also, the performance of the proposed circuits is compared in terms of power, propagation delay and power delay product. The performance comparison with the CMOS counterparts has also been included. It is found that the fundamental cell based priority encoders outperforms with reference to the series gating MCML based and the static CMOS based encoders.

Keywords: digital circuits, mixed-signal design, PFSCL, Fundamental cell, priority encoder

I. INTRODUCTION

MOS Current Mode Logic (MCML) circuits has enabled the design of circuits suited to the new digital information age. The style possesses features like frequency independent power consumption, low switching noise which makes it appropriate to design digital circuits for mixed-signal applications in comparison to CMOS logic style [1-4]. Their application areas include microprocessor design, mobile communication and optical transmission links etc.In microprocessors they are employed in the design of datapath as well as the control path of the processor. A large variety of arithmetic circuits such as adder, multiplier, decoder, flip flops, shift registers etc have been implemented in the logic style [5-8].

This paper focusses on the implementation of priority encoders in MCML logic style. The traditional MCML topology is based on the series-gating approach consisting of stacked source-coupled transistor pairs. This arrangement puts a limit on the minimum supply voltage value. A technique wherein the minimum power supply value is reduced in comparison to the traditional approach has been suggested in literature. This technique is based on the use of triple-tail cells and the uses a new cell named as fundamental cell [9-11]. In this

paper, MCML implementation of the priority encoders based on the traditional series-gating approach and the fundamental cell is proposed.

In this paper, the basics and working of priority encoders are briefly reviewed in section 2. Then the concept of MCML technique are briefly discussed in section 3. Thereafter section 4 presents the simulation results for the proposed MCML priority encoders. The simulations are performed in PSPICE using 180 nm CMOS technology parameters. The last section 5 concludes the paper

II. PRIORITY ENCODERS

A priority encoder is a combinational circuit wherein the output is produced according to the priorities assigned to the input lines [9]. Therefore, when an input with a higher priority is present, all other inputs with a lower priority will be ignored.Priority encoders are extensively employed in number of decision making components used in computer systems and other sub-systems. Thus, in situations wherein several processes, modules, or units request a single hardware (or software) resource in the system, a decision is made to allow a single request to use such a resource by the encoder. It is generally employed to implement a prioritized selection function in which the resource is granted to the request with the highest priority according to the selection function specified or coded. Some of the application includeenergy-efficient adaptive hybrid cache,a leakage energy reduction addressable memory design,bank structure in complex memories

To illustrate the working mechanism of a priority encoder, it is assumed that it is a circuit which is used to arbitrate among N units requesting to access a shared resource [20]. Each unit $i$request by sendinga bit A_i and receives a bit Y_i *in response which indicat*es whetehr the access has been gratnted or not. It is obvious that the access will be granted to a single unit with highest priority. If the least significant bit of the input corresponds to the highest priority, the logic for a priority encoder with 4 input lines can be expressed as follows:

$$Y_1 = A_1 \tag{1}$$

$$Y_2 = A_2 *(\sim A_1) \tag{2}$$

$$Y_3 = A_3 *(\sim A_2)*(\sim A_1) \tag{3}$$

$$Y_N = A_N *(\sim A_{N-1})*\ldots\ldots*(\sim A_1) \tag{4}$$

There different types of priority encoders available in literature which are rated on the basis of speed and power. Some of the available priority encoders are look ahead priority encoder, ripple priority encoder, increment priority encoder, Sklansky priority encoder

2.1 Look Ahead Priority Encoder

The purpose to design a look ahead priority encoder is to minimize the propagation delay of the priority status during the worst case operation, hence increasing the speed of the circuit. A multilevel look- ahead structure shortens the critical path.
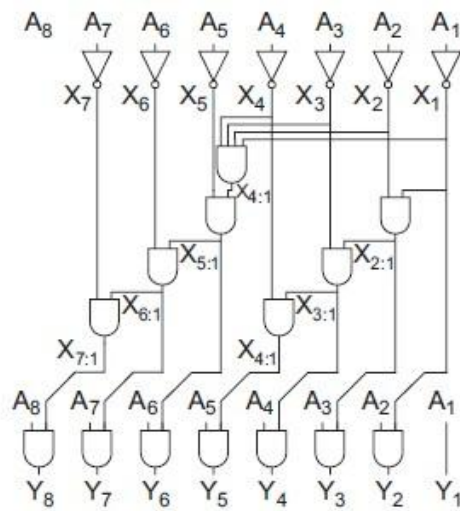
Fig. 2: Look ahead Schematic Diagram

2.2 Ripple Priority Encoder

They are widely used when meeting timing constraints because they use the least energy and have the simplest design in which the logic-out of one bit is simply connected as the logic-in to the next.
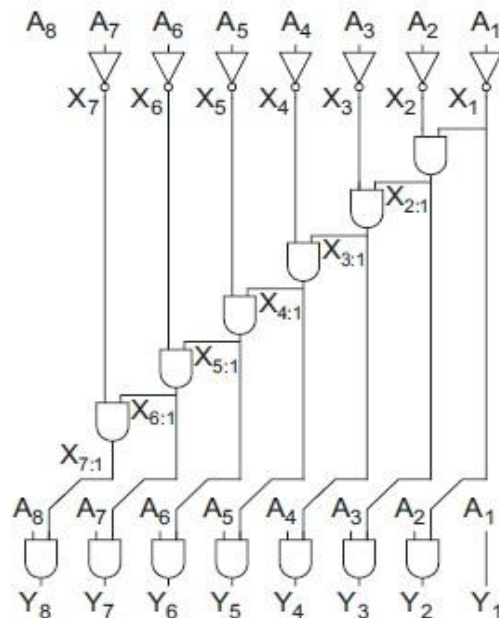

Fig. 3: Ripple Schematic Diagram

III. MOS CURRENT MODE LOGIC (MCML) STYLE

MCML style is a differential style that operates on the principle of current steering. The basic architecture of a MCML gate consist of a pull down network(PDN), load resistance and a constant current source. The logic function is realized in the PDN based on the series gating approach. The schematic of a CML inverter with inputs (v_{in1} and v_{in2}) and outputs (v_{out1} and v_{out2}) is shown in Fig. 3. The PDN comprises of source coupled transistor pair (M2-M3), the current source use an NMOS transistor M1 operating in saturation region whereas the passive resistors R1, R2 act as load for the inverter circuit. The bias current I_{SS} is completely steered to one of the two output branches depending on the differential input voltage. The current steered in the inverter is converted into the differential output voltage ($v_{out} = v_{out1} - v_{out2}$), through the passive resistors R1 and R2.

The series-gating approach is used to realize MCML gates [27]. It is a systematic and a general approach wherein an arbitrary logic function F(Y1,....Yn) is implemented as an network of source-coupled transistor pairs having all transistor paths associated with the 2^n possible input combinations and then properly connecting each of the upper drain nodes to the output nodes. This is illustrated in Fig. 4. Based on this concept, it is possible to realize basic combinational gates such as exclusive-OR (XOR) gate, 2:1 multiplexer (MUX) etc. and sequential circuits such as D latch. The corresponding realizations are depicted in Fig. 5.
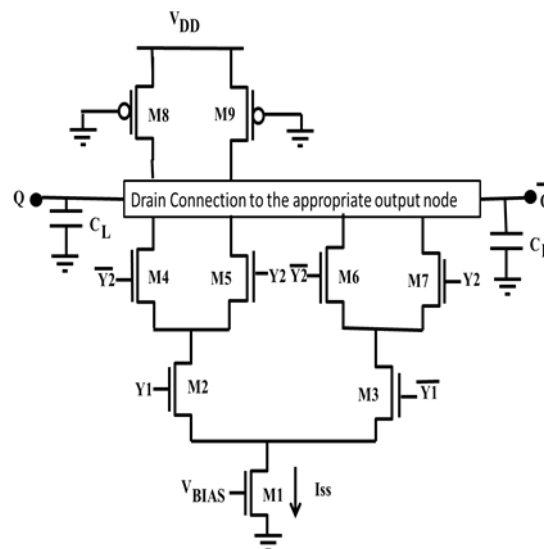

Fig. 4 A generalized two level MCML gate

Another approach named as fundamental cell based approach is used to realize combinational gates such as an exclusive-OR (XOR) gate, 2:1 multiplexer (MUX). It consists of two triple-tail cells (M3, M4, M7) and (M5, M6, M8) biased by separate current sources of $I_{SS}/2$ value. The transistors M7 and M8 are driven by the differential input B and are connected between the power supply terminal and the common source terminal of transistor pairs (M3 – M4) and (M5– M6) respectively. A XOR gate with differential inputs A and B (Fig. 6) is examined.A high voltage on differential input B turns ON the transistor M7, and deactivates the transistor pair (M3 – M4). At the same time, the transistor M8 turns OFF so that the transistor pair (M5 –M6)generates the

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output according to the differential input A. Similarly, the transistor pair (M3 - M4) gets activated for low differential B voltage and produces the corresponding output.
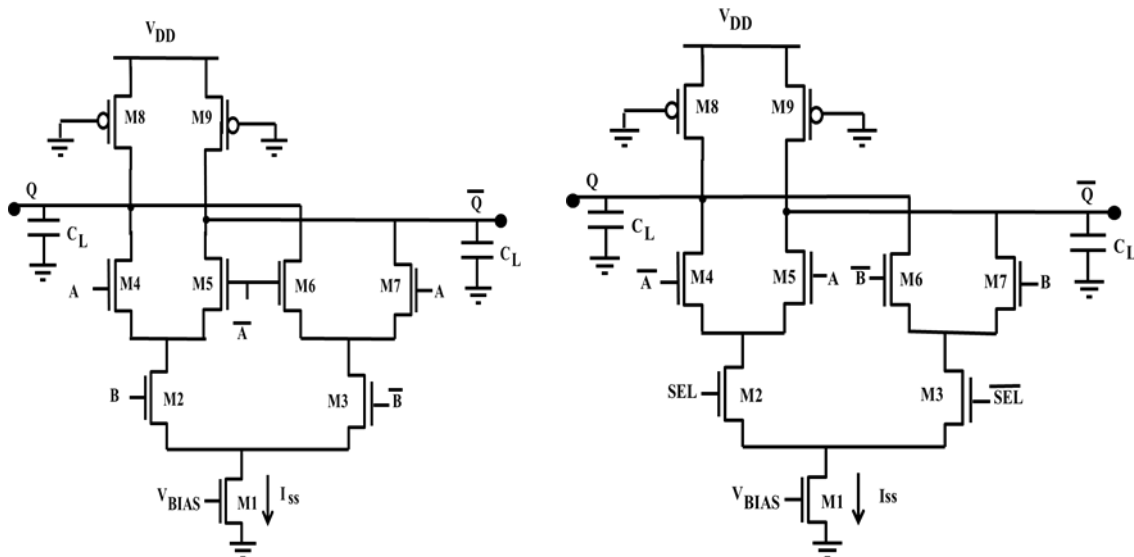
(a)   (b)
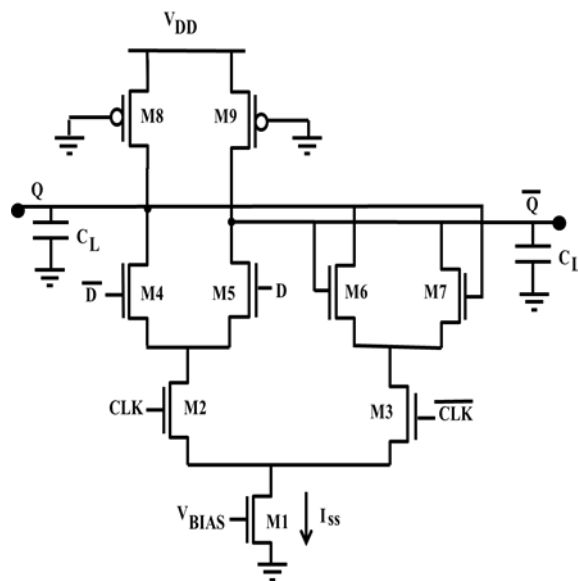
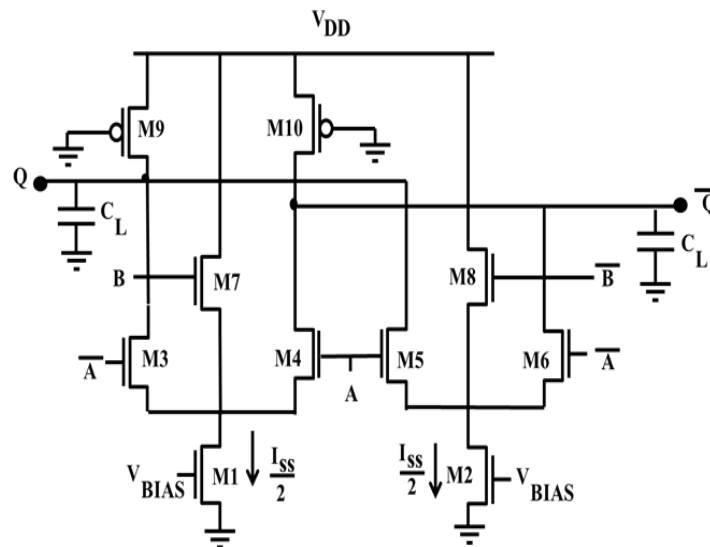(c)

Fig. 5 MCML gates a) XOR gate b) MUX c) D latch

Fig. 6 Fundamental cell based two input XOR gate

The traditional unbalanced and series-gate approach followed to implement MCML gates does not lead to significant power reduction. However, alternative approaches can be exploited to build MCML gates with are reduced supply voltage. This is because in the series- gate approach, V_{dd} must be sufficiently high to ensure that all transistors work out of the saturation region, according to number of stacked levels .One technique that allows for a V_{dd} reduction with respect to traditional MCML gates is the triple-tail approach that appears to be the most promising of all since it operates with the lowest supply voltage. Therefore, in the following analysis only triple-tail approach will be considered and accordingly it will be referred to as the low-voltage topology.

IV. SIMULATION RESULTS

The look ahead and ripple carry priority encoder circuits shown in Fig, 1 and Fig. 2 are implemented in MCML style using traditional; series gating approach as well as fundamental cell based approach. All the simulations are performed in PSPICE using 180-nm CMOS technology [10]. For allthesimulations, someconditions common to all design are thelengthof MOS transistorsis constant and is equal to 0.18µm.Thevoltage swing, Vswingis constant, V_{swing}=400mV. Theconstant current of 100 µA is maintained in all the MCML gates.

The functionality of the proposed MCML priority encoder is verified through simulation. The simulation graph for encoders based on series gating approach are shown in Fig. 7. It can be seen that both the encoders are exhibitingthe correct functionality. The simulations for the encoders based on fundamental cellare also performed. Similar waveforms were observed which are not shown for the sake of the brevity. properly. The performance of the proposed encodersis measured in terms of the propagation delay, power consumption and power delay product (PDP). For the purpose of fair comparison, the simulation results for the CMOS based encoders have also been included. A performance comparison between the CMOS and MCML based encoders is shown in Fig 8. The results clearly indicates that the MCML based encoders outperforms the CMOS based encoders. Also, a performance comparison between the two encoders realized using the traditional and the

fundamental cell based approach is also done. The results are summarized in Table I.It is found that the fundamental cell based priority encoder shows lower values pertaining to the delay and power. Thus, it is clear that the encoder realizations based on the fundamental cell based approach will results in efficient encoder design.
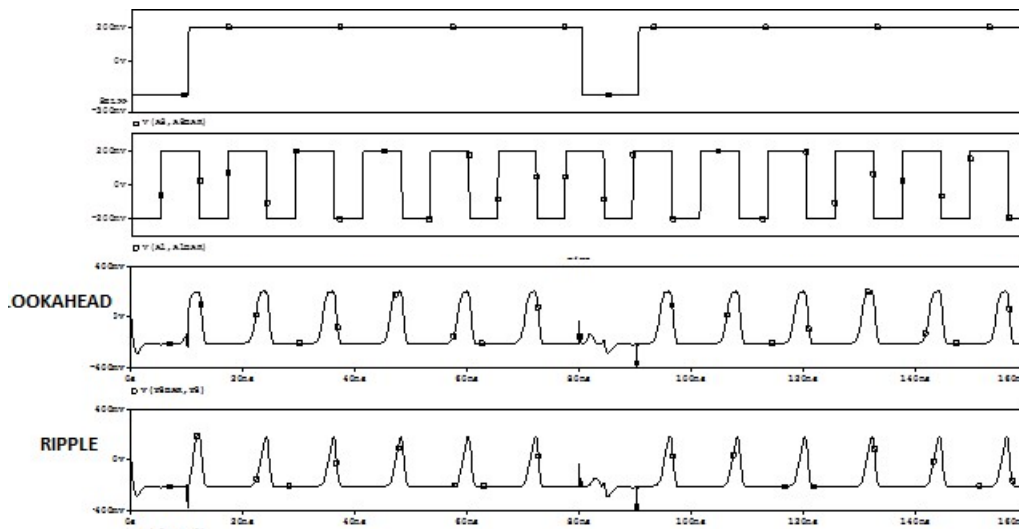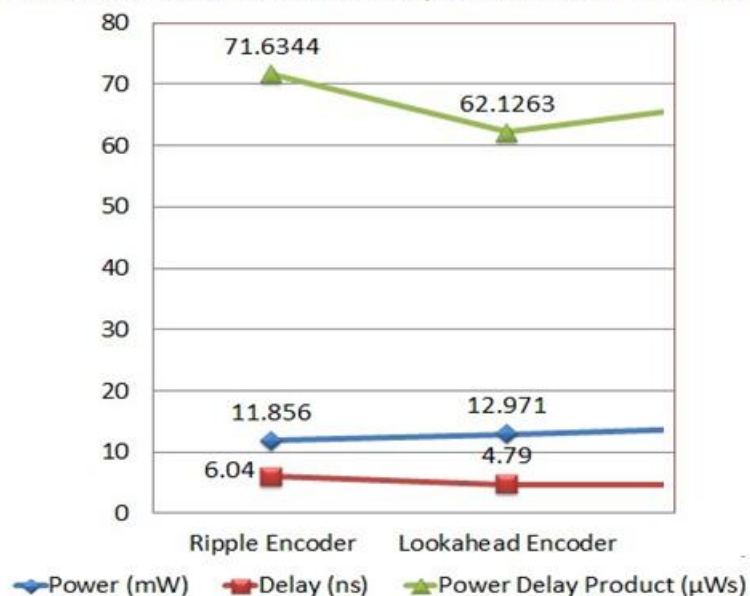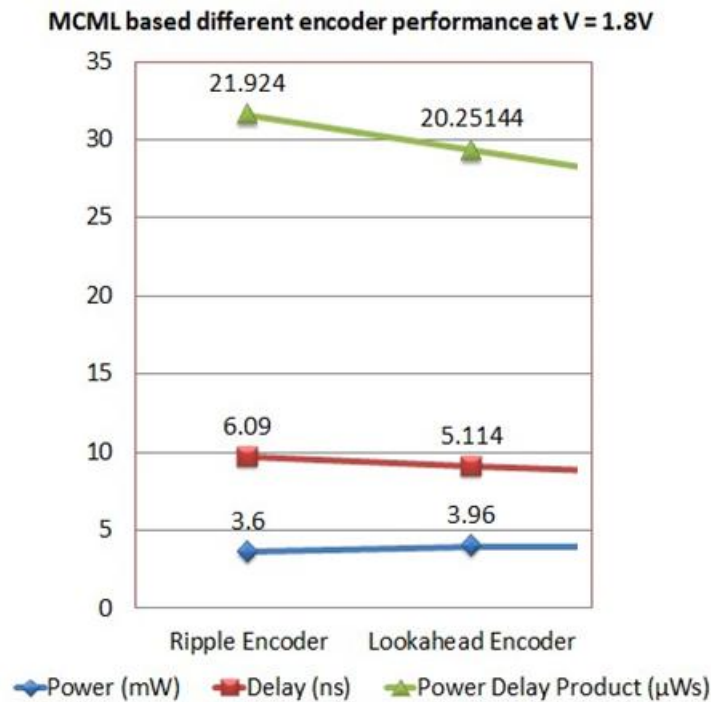

Fig. 7 Simulation waveform for the proposed MCML priority encoders based on the series gating approach

(a)

(b)

Fig. 8 Performance comparison of CMOS and MCML based priority encoder

Table. I:Powerconsumptionfor differentencoders at differentvoltagesupply.

Encoder	V=1.8V	V=1.4V	V=1.1V
Power			
Lookahead	3.96mW	3.08mW	2.42mW
Ripple	3.6 mW	2.8 mW	2.2 mW
Delay			
Lookahead	2.95 ns	. 5.157 ns	. 5.114 ns
Ripple	3.09 ns	6.15 ns	6.09 ns

V. CONCLUSION

In this paper MCML based realization of priority encoders in MOS Current Mode logic (MCML) style are proposed. The two types of encoders named as look ahead priority encoder and ripple carry priority encoder are presented. The MCML circuits based on the series-gating approach and the fundamental cell based approach are realized. The functionality of the proposed circuits is verified through simulation in PSPICE using 180 nm CMOS technology parameters. It is found that the proposed circuits exhibits the correct functionality. Also, their performance is compared in terms of power, propagation delay and power delay product. The results for the CMOS counterparts has also been included. It is found that the fundamental cell based priority encoders shows the lowest value in all the considered performance parameters. Hence, fundamental cell based priority encoders can be used to design mixed-signal applications.

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