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SURVEY OF VLSI MULTIPLIERS

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ABSTRACT

Low Power VLSI circuit has become important criterion for designing the energy efficient electronic designs for high performance and portable devices. In the majority of DSP application the critical operations are the multiplication. Multiplier is the most useful operation required in many hardware computations. Efficient implementation of multipliers is required in many applications. Functioning of a system depends on the performance of multiplier thus multipliers to be fast and consume less area in hardware. In this paper, comparative study of different multipliers is done.

Keywords: Low power, VLSI,DSP, multiplier.

I. INTRODUCTION

In today's digital signal processing and various other applications.Multipliers play an important role. Even in high performance systems such as microprocessor, DSP etc., addition and multiplication of two binary numbers is fundamental and most often used arithmetic operations. According to the Statics more than 70% instructions in microprocessor and most of DSP algorithms perform addition and multiplication. So, these operationdominates execution time. The demand of high speed processing has been increasing as a result of expanding computer and signal processing applications [1]. Low power consumption is an important issue in multiplier design. By reducing the number of operation we can reduce significant power consumption thereby reducing dynamic power which is a major part oftotal power consumption,Sothe need of high speed and low power multiplier has increased [2]-[3]. The Multiplier main block is arithmeticunit. The number of addition operation is performed by a multiplier concept. The different types of multipliers are Wallace tree multipliers,baughwooleymultiplier,braun multiplier, booth multiplier,vedic multiplier, array multiplier, serial multiplier, serial parallel multiplier [4].

II. WALLACE TREE MULTIPLIER

The partial-sum adders can also be rearranged in a tree like fashion, thereby reducing both the critical path and the needed number of adder cell. This structure is called the Wallace tree multiplier. A Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integer numbers.

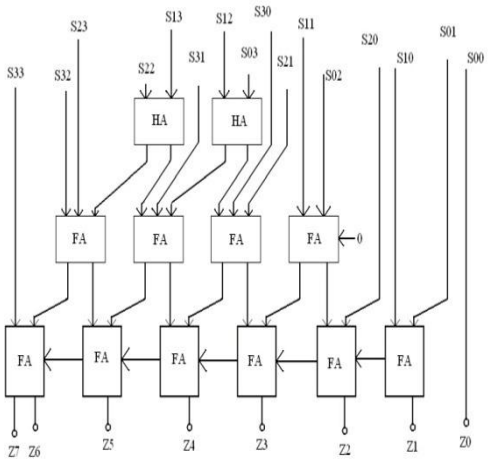
The Wallace tree multiplier has three steps to be followed,

- Multiply each bit of one of the arguments, by each bit of the other, yielding results.
- Reduce the number of partial products to two by layers of full and half adders.

- Group the wires in two numbers, and add them with a conventional adder.

The tree multiplier realizes substantial hardware savings for larger multipliers. The propagation delay is reduced as well. In fact, it can be shown that the propagation delay through the tree is equal to O (log3/2 (N)). While substantially faster than the carry-save structure for large multiplier word lengths, the Wallace multiplier has the disadvantage of being vary irregular, which complicates the task of an efficient layout design. The given four types of multiplier architecture are designed with seven different kinds of adder cell namely 14 transistors full adder cell, 20 transistors full adder cell, 28 transistors full adder cell, conventional full adder cell, New improved 14T full adder cell, transmission functional full adder cell and transmission gate full adder cell. Based on the extensive simulations, Except the Wallace tree multiplier, the other multipliers do not provide low power dissipation for all possible input combinations. Thus the multiplier using 14T adder improves the new power dissipation by 27% when compared to the other multipliers architecture. Wallace tree multiplier using new improved 14T adder cell dissipates small amount of power, which shall be called as low power multiplier. The performance many of the larger circuits is strongly dependent on the functioning of the multiplier circuits that have been used [6]. Also its Speed is improved by 47.8% when compared to the other multiplier types.

The Wallace tree multiplier using new improved 14-transistor adder circuits presented in this research are good candidates to build these large systems, such as high performance FIR filters with low power consumption. In transistor count will small increase of this adder. It can significantly reduce the latency of the systems. Also the area occupied by Wallace tree multiplier using new improved 14T adder is reduced significantly as compared to other types of multiplier architectures. Thus, multiplier analysis, it is concluded that the implementation of the NEW adder in the multiplier structure give the demanding results.



III. BAUGH WOOLEY MULTIPLIER

It is based on the concept of unsigned binary multiplication. It specifies algorithm that all possible in terms. It created first, and then sent through an array of half-adders and full-adders with the Carry-outs chained to the next most significant bit at each level of addition. Using baughwooley multiplier negative operands may be multiplied [5].

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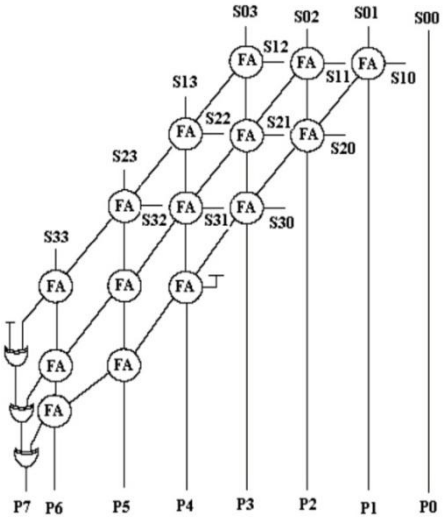
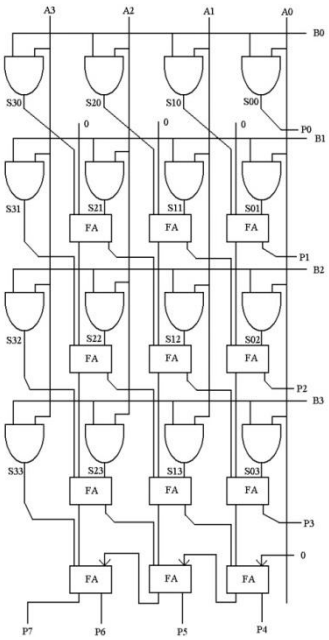


IV. BRAUN MULTIPLIER

Braun multiplier is a parallel multiplier, it is also called as carry save array multiplier, and it is easy to design. The structure consists of array of AND gates and adders arranged in the iterative way and no need of logic registers. This can be called as non – addictive multipliers.

In the internal structure, each product can be generated in parallel with the AND gates, and each partial product can be added with the sum of partial product which has previously produced by using the row of adders. All the partial products are computed in parallel, then collected through a cascade of Carry Save Adders. By the depth of the carry save array the completion time is limited and by the carry propagation in the adder. Note that this multiplier is only suited for positive operands.



BRAUN MULTIPLIER

V. BOOTH MULTIPLIER

The procedure for multiplying binary integers in signed -2's complement representation is given by booth multiplication algorithm.

Algorithm

1. The multiplicand and multiplier are placed in the m and Q registers respectively. A 1 bit register is placed logically to the right of the LSB (least significant bit) Q0 of Q register. This is denoted by Q-1. A and Q-1 are initially set to 0.The two bit Q0 and Q-1 is checked by control logic.

2. If the two bits are same (00 or 11) then all of the bits of A, Q, Q-1 are shifted 1 bit to the right. If they are not the same and if the combination is 10 then the multiplicand is subtracted from A and if the combination is 01 then the multiplicand is added with A. In both the cases results are stored in A, and after the addition or subtraction operation, A, Q, Q-1 are right shifted [7].

3. The shifting is the arithmetic right shift operation where the left most bit namely, An-1 is not only shifted into An-2 but also remains in An-1. This is to preserve the sign of the number in A and Q. The result of the multiplication will appear in the A and Q.

The Booth multiplier is multiplied by two numbers, the numbers are either signed or unsigned numbers. The Braun multiplier is used to multiply only the unsigned numbers; this is the one drawback of Braun multiplier. But booth multiplier multiply with both numbers.

VI. VEDIC MULTIPLIER

The structure of vedic Multiplier is a Vertical Crosswise. It generates all partial products and their sum in one step. Since the partial products and their sum are calculated in Parallel. The Vedic Multiplier is one of the fastest multiplier. The Vedic Multiplier works under Algorithmic basis [9].

Algorithm

- Divided the Multiplicand A and Multiplicand B into two equal parts, each consisting of [N to (N/2) + 1] bits and [N/2 to 1] bits respectively, where first bit parts indicates the MSB and other represents LSB.
- Represents the parts of A as Am and Al and parts of B as Bm and Bl. Now represents A and B as Am Al and BmBl respectively.
- For example AXB we have general format as shown in below.
  - *Am Al*
  - *BmBl*
- These inputs are multiplied with Vertical and Crosswise basis,
  - *Am x Bm, Am x Bl, Al x Bl*
  - *Al x Bm*
- The individual multiplication products can be obtained by the partitioning method and applying the basic building blocks.
- The Booth and Vedic Multipliers are used to Signal Processors (DSPs) etc.,

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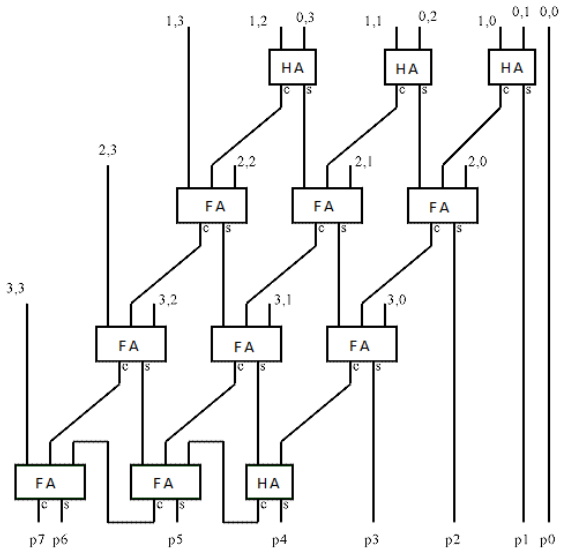
VII. ARRAY MULTIPLIER

Array multiplier is an efficient layout of a combinational multiplier. Array multiplier is well known due to its regular structure. Multiplier circuit is based on repeated addition and shifting procedure. By using a combinational circuit that forms the product bit all at once thus making it a fast way of multiplying two numbers, the multiplication of twobinary number can be obtained with one micro-operation.sinceonly delay is the time for the signals to propagate through the gates that forms the multiplication array.

By the multiplication of the multiplicand with one multiplier digit each partial product is generated [10]. The partial product are shifted according to their bit sequences and then added. The summation can be performed with normal carry propagation adder. N-1 adders are required where N is the no. of multiplier bits.Byconsidering two binary numbers A and B of m and n bits in array multiplier. There are mn summands that are produced in parallel by a set of mn AND gates. n x n multiplier requires n(n-2) full adders, n half-adders and n2 AND gates. Also, the worst case delay would be (2n+1) td in array multiplier. Array Multiplier gives more power consumption as well as optimum number of components required, but delay for this multiplier is larger.As area is also increased it requires larger number of gates. As the result this array multiplier is less economical. Thus, it is a fast multiplier but hardware complexity is high.

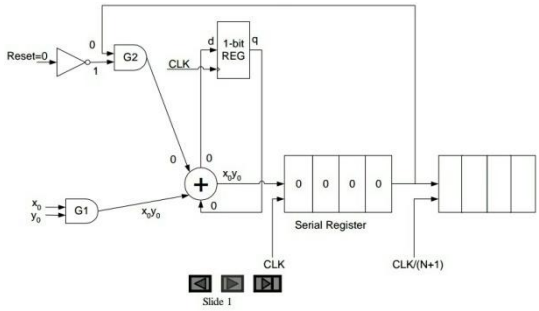


ARRAY MULTIPLIER

SERIAL MULTIPLIER

In Serial MultiplierWhen area and power is importantand delay can be tolerated the serial multiplier is used. In this multiplier circuit uses one adder to add the m * n partial products. In the multiplicand and Multiplier inputs have to be arranged in a special manner synchronized with circuit behavior as shown on the inputs to be presented at different rates [11].It depending on the length of the multiplicand and the multiplier. Two clocks

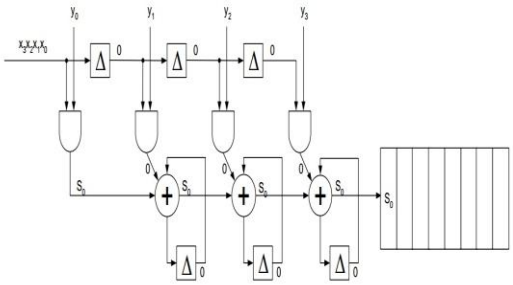
are used, one to clock the data,the other one for the reset. In delay is O (m,n) by using first order approximation. With this circuit arrangement the delay is given as D =[(m+1)n + 1] .



SERIAL MULTIPLIER

VIII. SERIAL PARALLEL MULTIPLIER

One is serial and other one operand is fed to the circuit in parallel. N partial products are formed each cycle. On successive cycles, each cycle does the addition of one column of the multiplication table of M*N PPs. The final The general architecture of the serial/parallel results are stored in the output register after N+M cycles [12]. While the area required is N-1 for M=N.



IX. CONCLUSION

Parallel multiplier have more option when compare to serial multiplier has been concluded .To be efficient in speed, power and area in digital designs Vedic Multiplier is seen with respect to other multipliers.

Here we concluded that for large binary number multiplication sequential multiplier by studying different multiplier it perform greater than the combinational multiplier.

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