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SYNTHESIS OF SEQUENTIAL CIRCUITS BY REVERSIBLE LOGIC

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ABSTRACT

Reversible gates are the building blocks of quantum computation and is gaining importance in recent years due to its low power consumption, nanotechnology,advance computing etc.we proposed a new model of designing and synthesis of sequential circuits for D,JK,T Flip-Flop and counters using reversible logic. All circuits have been Modeled and verified using VERILOG and MODEL-SIM.

Keywords: counter, flip-flop, garbage output, quantum cost, reversible gates

I. INTRODUCTION

As Moore's law continues to hold, miniaturization of integrated chips continues to take place. This leads to more power dissipation. On further investigation Bennet showed that information is lost when the input vector cannot be uniquely recovered from its output vectors and the energy dissipated is directly linked with the number of bits lost. Heat dissipation can be prevented if reversible circuits are used. Information loss can be prevented if the input bits can be completely recovered from the output. Hence the property of reversibility, will be an important aspect in future circuit design and it is important to realize technology that is capable of operating at such atomic levels while following the property of reversibility to ensure low power dissipation. However, reversible logic is suffering from two problems. Firstly, there is a shortage of technology with which reversible gates[can be built. Work is continuing in this field. Secondly, though a lot of research is being done on how to design combinational circuits using reversible logic, very few work is being done in the area of sequential reversible logic implementations.In fact when TommasoToffoli first characterized reversible logic in his 1980 work 'Reversible Computing' he stated that "Using invertible logic gates, it is ideally possible to build a sequential computer with zero internal power dissipation". R. Landauer states that traditional logic operations dissipate heat due to the loss of information bits. It is proved that each bit of information loss generates kTln2 joules of heat energy; where k is Boltzmann's constant and T is the absolute temperature at which computation is performed. C. H. Bennett showed that energy dissipation problem can be avoided if all the gates in the circuits are reversible. This is because reversible logic makes every step of computation to be completely reversible, so that no information is lost at any step of computation. Research is going on reversible logic and a good amount of research work has been carried out in the area of reversible combinational logic. There is not much work in area of sequential circuit like flip flops and counters. A counter is a sequential circuit capable of counting the number of clock pulses that have arrived at its clock input . This paper proposes a novel of n bit

reversible counter. The efficiency of the proposed design is proved with the help of proper theorems and algorithms.

II. REVERSIBLE LOGIC SYNTHESIS:

A reversible circuit is a circuit in which the number of output vectors is equal to the number of input vectors and there is a one to one mapping between each input and output vector. For example let an input vector I_V and an output vector O_V be defined as follows:

2.1 Cost Metrics:

The cost metrics in logic circuits include the quantum cost, delay and the number of garbage outputs.

2.2 Quantum cost:

The quantum cost of circuit is defined in terms of the number of primitive gates used.

2.3 Garbage output:

The number of unused or unwanted outputs which are obtained to satisfy the condition of reversibility is called the garbage output.

III. BASIC QUANTUM GATES:

3.1Feynman Gate:

Also known as the Controlled NOT Gate or CNOT Gate, this gate is a multi-qubit gate and also one of the most important quantum gates. Any quantum circuit can be implemented using only this gate and this gate is considered the universal gate for a quantum circuit. It consists of a control and target qubit and changes the value of the target depending on the value of the control. The quantum cost of CNOT Gate is Two input vectors A and B are mapped to the corresponding output vectors P and Q. Here, the input A is the control which determines whether the target input B is to be complemented or not through the XOR operation.

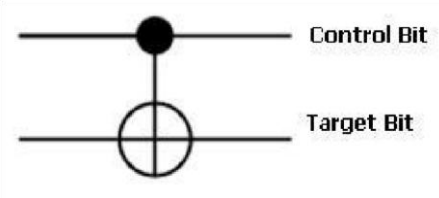

Fig.1 CNOT Circuit

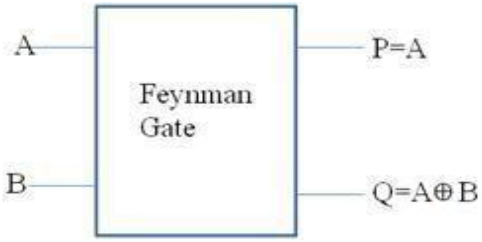

Fig.2 CNOT: Block Diagram

The Double Feynman Gate is similar to the Feynman Gate in operation but has an extra input vector. Correspondingly the quantum cost is 2.The block diagram of Double Feynman gate is shown below.

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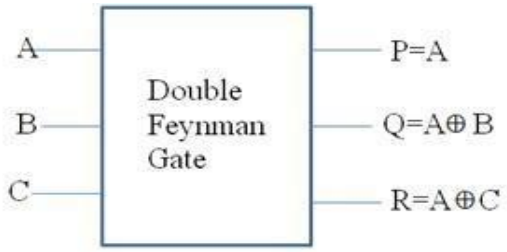

Fig.3 Double Feynman Gate

3.2 Fredkin Gate :

Similar to the Toffoli gate, it has a quantum cost of 5 and the input and output vectors I(A, B, C) andO(P, Q, R) are related as shown in the figure below.

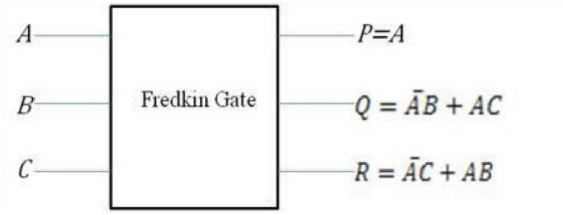

Fig.4 Fredkin Gate Block Diagram

The Fredkingate can be used to swap the inputs at the output or to perform the if-else condition. In the above figure, if the value of A=1, we get Q=C and R=B. Hence the inputs get swapped at the output. There is also a 4-input Fredkin gate, whose block diagram is shown below. The quantum cost of the 4 input Fredkin Gate is 5.

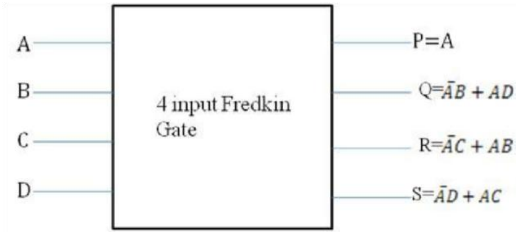

Fig.5 Block Diagram of 4-Input FredkinGate

3.3Peres Gate:

The Peres Gate[8] incorporates the functions of both the CNOT and the Toffoli gate and is therefore useful for a large number of quantum operations. The Quantum Cost of Peres Gate is 4.

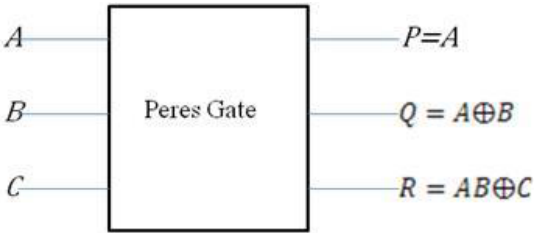

Fig.6 Block Diagram of Peres Gate

The Pauli-X gate acts on a single qubit. It is the quantum equivalent of a NOT gate (with respect to the standard basis |0, |1, which privileges the Z-direction)

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It equates to a rotation of the Bloch Sphere around the X-axis by p radians. It maps |0 to |1 and |1 to |0. It is represented by the Pauli matrix: X= 1001

IV. RELATED WORKS:

Thapliyal proposed a circuit of D Flip Flop using seven reversible gates with eight garbage outputs. the circuit is shown is shown in fig.7

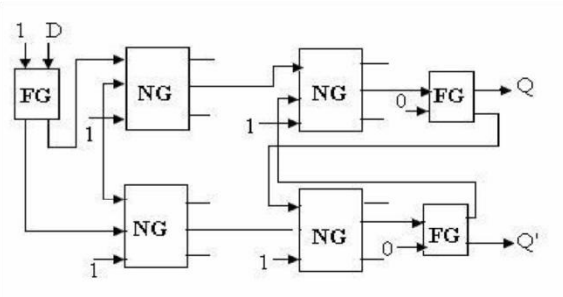

Fig.7 Reversible D Flip Flop with 7 gates

Ali proposed an improved version of Thapliyal's reversible D Flip Flop which was a realization of the conventional D Flip Flop sequential circuit. Ali proposed a new gate, BME gate which was used to optimize the existing reversible circuit based on the number of reversible gates used and the garbage outputs produced. The number of gates was reduced to four and the number of garbage outputs was also reduced to four. A RS Flip Flop was used for the implementation of this circuit. The optimized circuit is shown below.

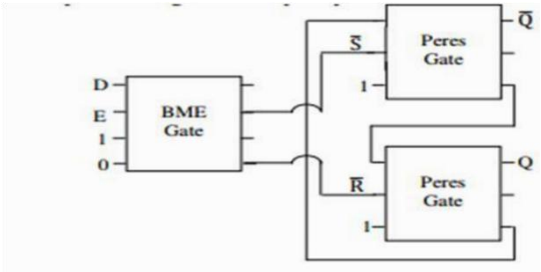

Fig.8 Reversible D Flip Flop with 3 Gates

Thapliyal also proposed circuits of JK and T Flip Flop.The circuits are shown in figures respectively. Both the circuits are designed using ten reversible gates.

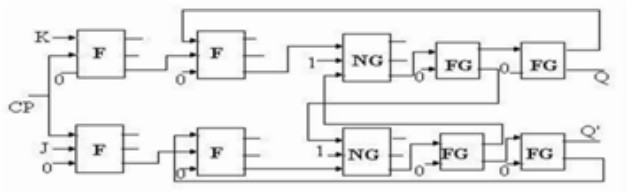

Fig.9 Reversible JK Flip Flop

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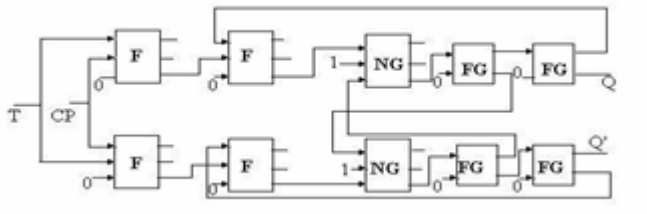
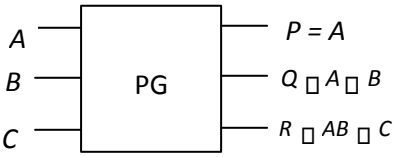


Fig.10 Reversible T Flip Flop

V. QUANTUM ANALYSIS OF POPULAR REVERSIBLE GATES:

Several reversible logic gates have been designed till now. Some popular reversible gates and their quantum equivalent diagrams are shown in Fig.1. Feynman gate (FG) is the only 2*2 gate which has 1 as the quantum cost. Peres gate (PG) has 4 as the quantum cost is one of 3*3 gates.,Selim Al Mamun(SAM) gate has 4 as the quantum cost and Toffoli gate (TG) has 5 as the quantum cost.



(a)2*2 feynman gate

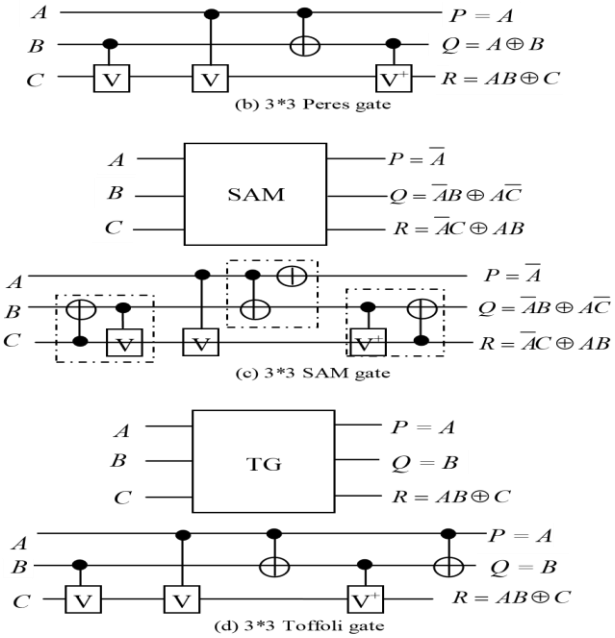


Fig.11Quantum Analysis of Popular Reversible Gates

VI. PROPOSED METHOD

6.1 Synchronous Counters:

synchronous counters is different from asynchronous counters in that clock pulses are applied to the inputs of all the flip-flops at a time.A flip-flop is complementing depending on the input value T and the clock pulse. The

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flip-flop in least significant position is complemented with every clock pulse. A flip-flop in other position is complemented only when all the outputs of preceding flip-flops produces 1.

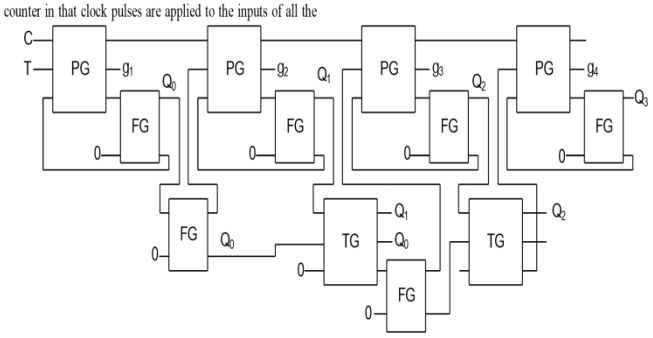

Fig.12 Proposed Synchronous Counter using Reversible Gates

6.2 D Flip-flop:

The logical expression of D flip flop can be reduced to

$Q(t+1) = \overline{CLK}.Q(t) + CLK.D$

In reversible logic, the D flip flop can be implemented by using just one 4-input Fredkin gate. By making the third input 0, the above equation can be obtained, as shown in the figure below

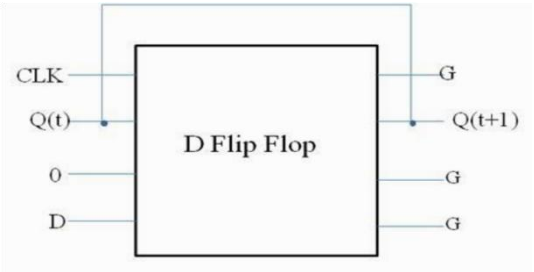

Fig.13 Proposed D Flip Flop using Reversible Gates

6.3 JK Flip- flop:

Similarly, the derived equation of JK flip flop is given $Q(t+1) = \overline{CLK}.Q(t) + CLK\left(J.\overline{Q(t)} + \bar{K}.Q(t)\right)$

JK flip flop can be implemented using two 3-input Fred-kin gate and a Pauli X-gate which is the quantum equivalent of CMOS NOT gate.

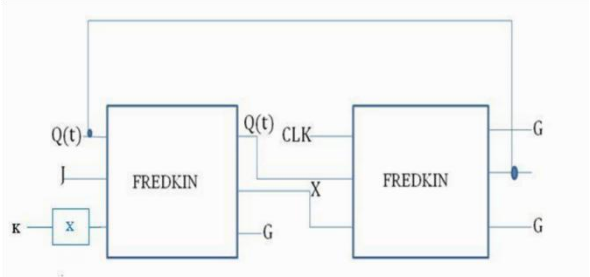

Fig.14 Proposed JK Flip Flop using Reversible Gates

6.4 T Flip-flop:

T flip flop is implemented using a CNOT and a 3-input

Fredkin gate. The derived equation of T flip flop is given by

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$$Q(t+1) = CLK.\left(T \oplus Q(t)\right) + \overline{CLK}.Q(t)$$

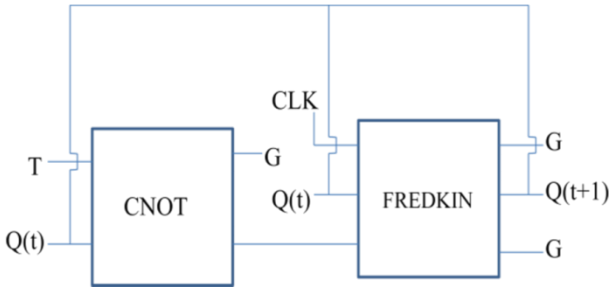

Fig.15 Proposed T Flip Flop using Reversible Gates

In the given quantum circuit, the CNOT is used for theoperation T⊕Q(t) which is fed into the Fredkin Gate whose output is controlled by the CLK value.

VII. RESULT ANALYSIS

Table 1:Evaluation of the proposed D Flip-flop:

D – Flip flop	No.of gates	Garbage outputs
Proposed circuit	8	9
Existing one	None in literature	None in literature

Table 2: Evaluation of the proposed T Flip-flop:

T Flip-flop	No.of gates	Garbage outputs
Proposed circuit	11	13
Existing one	None in literature	None in literature

Table 3: Evaluation of the proposed JK Flip-flop:

JK Flip-flop	No.of gates	Garbage outputs
Proposed circuit	9	11
Existing one	None in literature	None in literature

Table 4: Evaluation of the proposed Synchronous counter:

4bit synchronous counter	Quantum cost	delay	Garbage outputs
proposed	34	34	5
Khan	35	35	4

VIII. CONCLUSION

The proposed reversible design is utilized for efficiently designing D, JK , T Flip-Flops and synchronous counters. Flip-Flops are important memory elements and are used in several circuits like RAM, Logic Blocks of FPGA. By comparing the existing designs with the proposed ones, it has been observed that the proposed designs are less costly in terms of the number of gates and the number of garbage outputs. The proposed designs are highly optimized. Thus, the resulting reversible sequential circuits are more cost effective.

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