International Journal of Advance Research in Science and Engineering
Volume No.06, Issue No. 10, October 2017
www.ijarse.com
IJARSE
ISSN: 2319-8354

128 BIT MODIFIED CARRY SELECT ADDER USING BINARY TO EXCESS-ONE CONVERTER

M.Srinivasaperumal[1], S.Pavithra[2],

V.S.Kavya Lekshmi[3], K.MohammedArshad[4]

1,2,3,4 Dept. of ECE , SNS College of Technology

Coimbatore,(India)

ABSTRACT

Design of power-efficient and high-speed data path logic systems are one of the most substantial areas of research in VLSI system design in many data-processing processors Carry Select Adder (CSLA) is one a fastest adders used to perform arithmetic functions. The upcoming technologies depicts that there is a scope for reducing the area and power consumption in the CSLA. To significantly reduce the area and power of the CSLA this work uses a simple gate level modification . Based on this modification CSLA architecture have been developed and can be compared with the regular CSLA architecture. However,the regular CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input, then the final sum and carry are selected by the multiplexers (mux). The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA to achieve high speed and low power consumption. The results analysis shows that the proposed CSLA structure is better than the regular CSLA.

Keywords: Carry Select Adder (CSLA),Ripple Carry Adders (RCA), VHDL Modelling & Simulation.

I. INTRODUCTION

In the main area of research in VLSI system design, area and power reduction in data path logic systems play a major role. .For high performance processors and systems High-speed additionand multiplication havealways been a fundamental requirement.The speed of addition in digital adders is limited by the time needed to propagate a carry through the adder. Only after the preceding bit position has been summed and a carry propagated into the next position the sum for each bit position in an elementary adder is generated sequentially.The production of carries has become the major speed limitingfactor in any adder. And also many authors have considered the addition problem. The CSLA is used in many computational systems to moderate the problem of carry propagation delay to generate the sum. by independently generating many carries and then select a carry . However, the CSLA is not area efficient as it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input and then the final sum and carry are selected by the multiplexers (mux). Inorder to runover above problem, the basic idea of the proposed work is by using n-bit binary to excess-1 code converters (BEC) to advance the speed of addition. This logic can be put in to action with any type of adder to further improve the speed. Using BEC instead of RCA in

the regular CSLA to acquire lower area and power consumption. The lesser number of logic gates than the Full Adder (FA) structure is the main advantage ofBEC.

II. LITERARYREVIEW

This model depicts a 16 bit modified carry select adder shows reduction in area coverage and power consumption when compared to regular carry select adder with increase in delay. The reduced number of gates in the work offers the reduction of area and the total power. 16 bit area efficient CSLA is designed which provides 32% reduction in area when compared with R-CSLA and 12.5% reduction in area when compared with M-CSLA. If the number of bits has been further increased a great reduction in area and power consumption can be expected [1].

The Carry Select is one of the fastest adders used in many data processing processors to perform fast arithmetic functions [2]. The modified square root carry select adder has been developed by making some changes in gate level by downsizing the field and power diminution. The modified SQRT CSLA has slightly larger delay. The area and power of 64 bit modified SQRT CSLA are reduced by 17.4% and 15.4% respectively.

The distinguished results shows that the power delay product and also the area delay product of the contemplated design show a decrease for all sizes which testifies the success of the method and not the mere trade-off of delay for power and area [3].

III.FUNDAMENTAL ADDER BLOCK

Ripple Carry Adder (RCA) shows the compresseddesign but their estimation time is prolonged. Carry Look-Ahead Adder (CLA) is used in time critical applications to derive fast results but it leads to increase in area. But the carry select adder provides a compromise or bridgeway between the small areas but longer delay of RCA and large area with small delay of Carry Look Ahead adder.

Ripple Carry Adder consists of cascaded "N" single bit full adders. Output carry of previous or preceding adder becomes the input carry of next or succeeding full adder. Therefore, the carry of this adder traverses longest path called worst case delay path through N stages. Fig. 1 shows the block diagram of Ripple carry adder. The delay of the adder increases with the value of Nin a linear way. RCA in spite of having an advantage of covering least area, it has the lowest speed amongst all the adders because of large propagation delay. Now CSLA postulates aadvanced way to get around this linear dependency that is to assume all possible values of input carry i.e. 0 and 1 and figure out the result in prior.Result can be selected using the multiplexer stage once the original value of carry is known. To develop the partial sum and carry by overbearing input carry Cin=0 and Cin=1,the standard CSLA makes use of dual RCA's then the multiplexers select the final sum and carry.

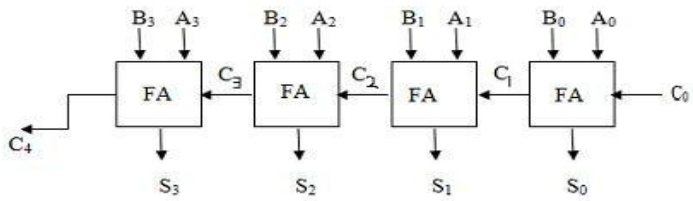


Fig. 1 4-bit Ripple Carry Adder

International Journal of Advance Research in Science and Engineering
Volume No.06, Issue No. 10, October 2017
www.ijarse.com
IJARSE
ISSN: 2319-8354

IV. BEC

The key action of the CSLA is accessed by using the 4-bit BEC along with the multiplexer. One input of the 8:4 multiplexer gets as it input (B3, B2, B1, and B0) and another input of the multiplexer is the BEC output [1]. This produces the two possible sectional results in parallel and according to the control signal Cin, the multiplexer is used to select either the BEC output or the direct inputs. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols NOT, & AND, XOR) X0 = ~B0 X1 = B0 ^ B1 X2 = B2 ^ (B0 & B1) X3 = B3 ^ (B0 & B1 & B2) The basic idea of this work is to use Binary to Excess- 1 converter (BEC) instead of RCA with Cin=1 in conventional CSLA BEC uses less number of logic gates than N-bit full adder structure inorder to optimise area and power. N-bit RCA is replaced by N+1 bit BEC .Therefore, Modified CSLA has low power and less area than conventional CSLA. CSLA has been picked for correlation with modified design using BEC as it has more stabilised delay, less area and low power. In order toreduce the delay, area and power, the design is modified by using BEC instead of RCA with Cin=1. Further also, the parameters like delay, area and power can be lessened.

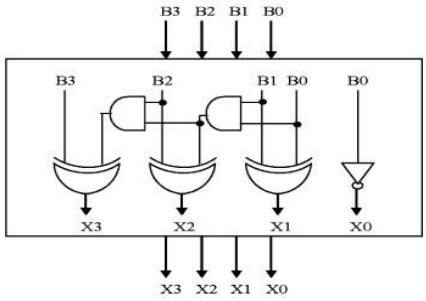


Fig.2. 4-b BEC

Table1. Truth table of 4-bit Binary to Excess-1Converter

Binary Logic $B_0\ B_1\ B_2\ B_3$	Excess-1 Logic $X_0\ X_1\ X_2\ X_3$
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

International Journal of Advance Research in Science and Engineering
Volume No.06, Issue No. 10, October 2017
www.ijarse.com
IJARSE
ISSN: 2319-8354

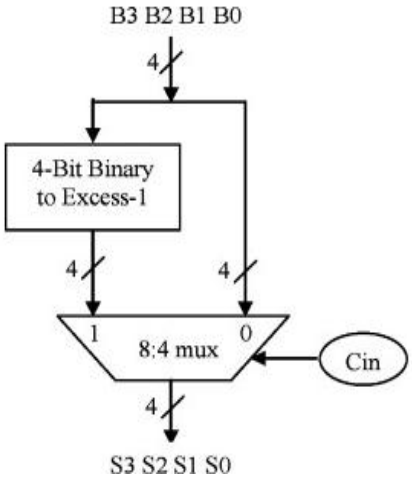


Fig. 3 4-bit BEC with 8:4 mux

V. ARCHITECTURE OF 16BIT MODIFIED LINEAR CARRY SELECT ADDER

This modified linear CSLA has 3 blocks namely RCA, BEC and MUX .Each block does different operations. For example, RCA does the addition operation which delivers the carry separately. The main advantage is that it eliminates the propagation delay which generally occurs in the regular CSLA. The main composition of BEC is AND(&), NOT(~) and XOR (^).The use of BEC in the CSLA resulted in better area efficiency. On the other hand, it is also utilised to reduce the propagation delay that occurs in the conventional CSLA. In the 16 bit modified linear CSLA, BEC has been used to obtain better power efficiency. The ripple carry adder generally consists of full adders. In this design, a 4 bit ripple carry adder containing four full adders is used. Full adder does the general operation of adding the binary numbers and giving out the carry along with the sum.

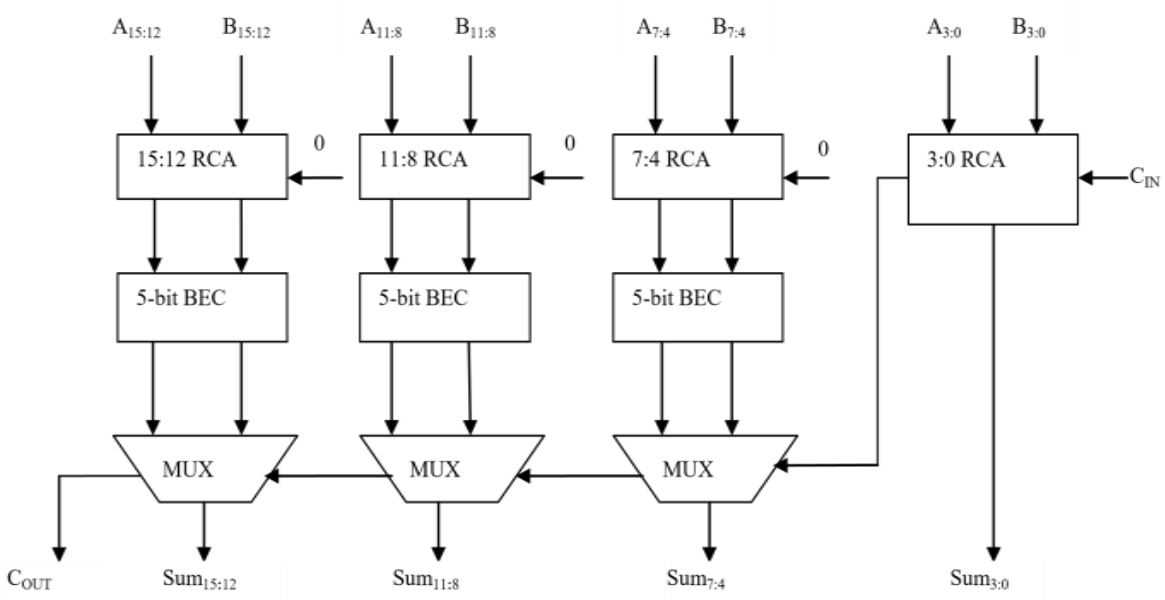


Fig.4 Block Diagram of modified 16bit linear Carry Select adder

International Journal of Advance Research in Science and Engineering
Volume No.06, Issue No. 10, October 2017
www.ijarse.com
IJARSE
ISSN: 2319-8354

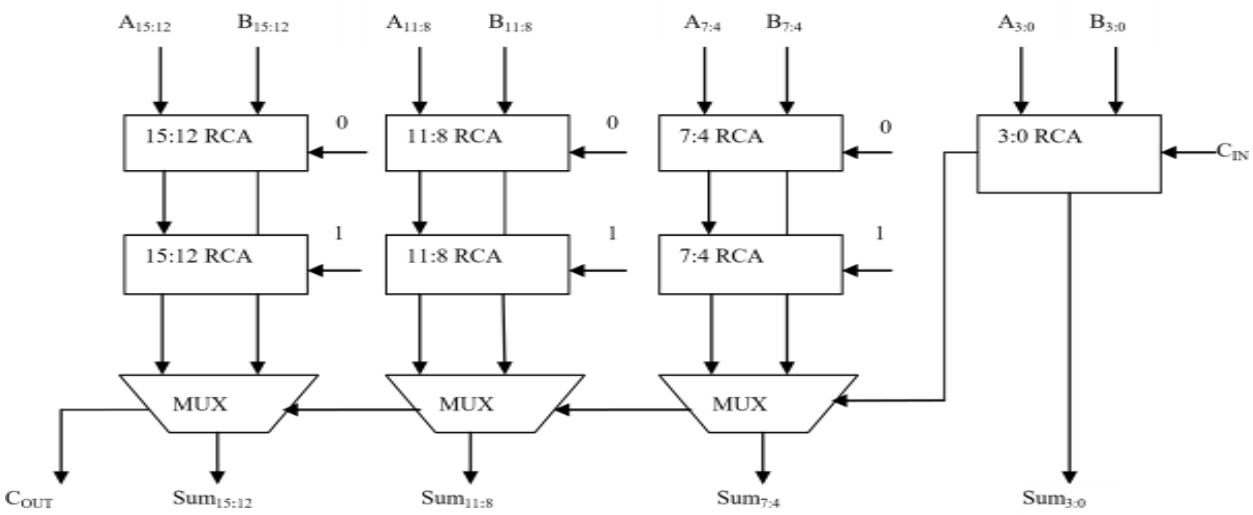


Fig. 5 16-bit conventional carry select adder

VI. ARCHITECTURE OF 128-BIT CSLA

A 16-bit carry select adder(CSLA) can be refined in two different sizes namely uniform block size and variable block size. The number of bits required for BEC logic is 1 bit, similarly a 32, 64 and 128-bit can also be developed in two modes of different block sizes. Ripple-carry adders are the thick and most compressed full adders, but their performance is circumscribed by a carry that should broadcast from the least significant bit to the most-significant bit. The various CSLA can also be developed by using ripple carry adders.

The significance of the BEC logic stems from the large silicon area subjection when the CSLA with large number of bits are designed. The Boolean expressions of the 8-bit BEC is listed improved up to 40% to 90%, by performing the additions in parallel, and reducing the maximum carry delay. The design of the 128-b regular CSLA is shown in Fig. 6. It has five groups of RCA. The delay and area interpretation of each group are shown in Fig. 3, in which the numerals with in specify the delay values, e.g., sum2 requires 10 gate delays.

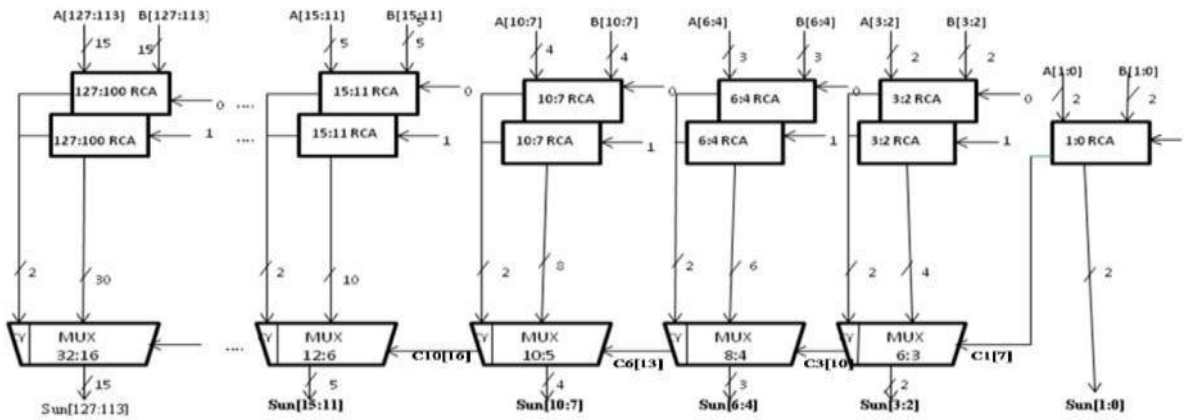


Fig .6 Architecture of Regular 128-b CSLA

International Journal of Advance Research in Science and Engineering
Volume No.06, Issue No. 10, October 2017
www.ijarse.com
IJARSE
ISSN: 2319-8354

VII. MODIFIED ARCHITECTURE OF 128-BIT LINEAR CSLA

In this design, some of the RCA blocks are replaced with the BEC, that leads to reduced area and propagation delay .The propagation delay and area count of the modified linear CSLA for a range of bits are compared and analysed. The results are clearly demonstrated.Low power, less delay and reduced area than all the other adder structures. It is also slightly faster than all the other adders. In this way, the transistor enumeration of proposed CSLA is reduced having reduced area and low power which makes it elementary and efficient for VLSI hardware utilisation.

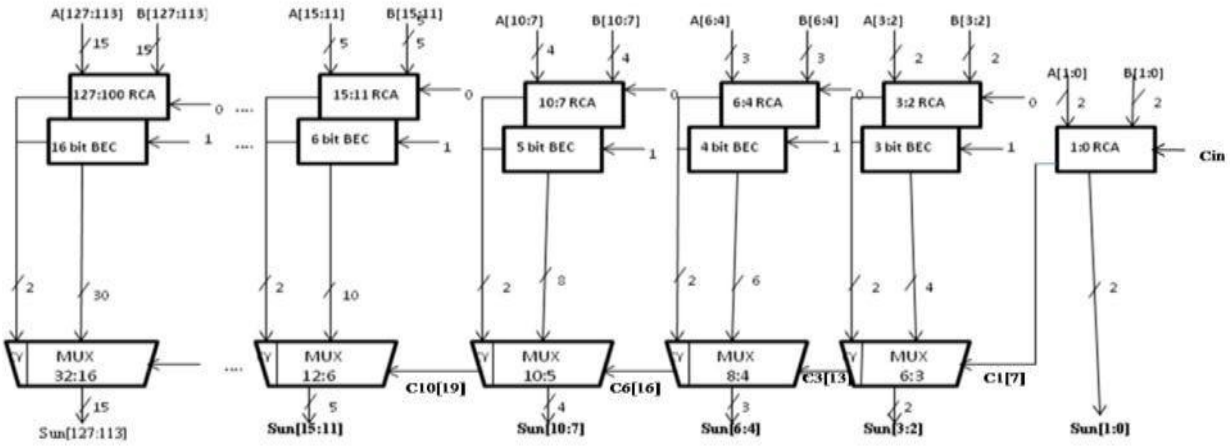


Fig.7 Modified architecture of 128 bit

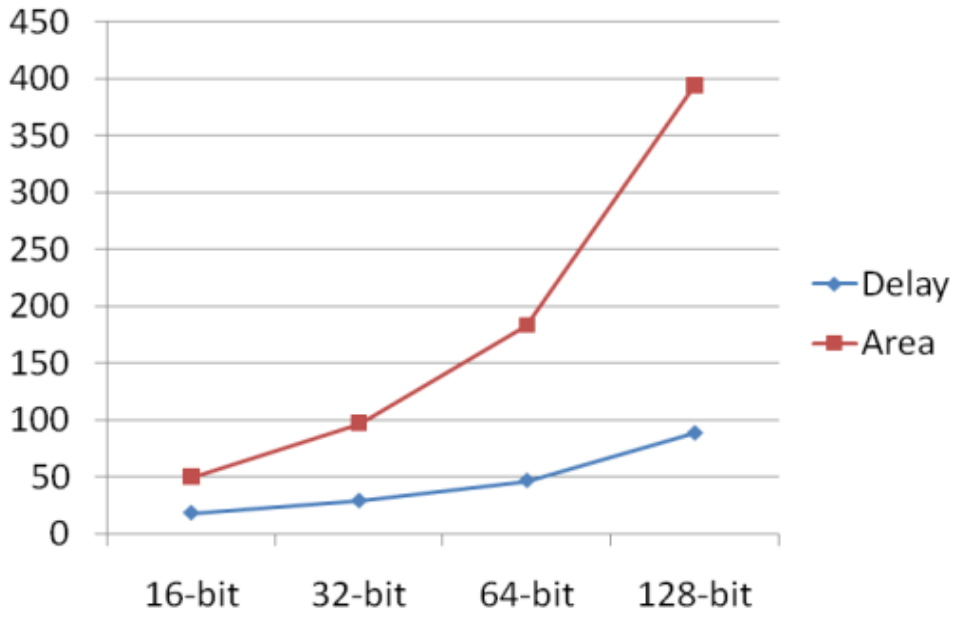
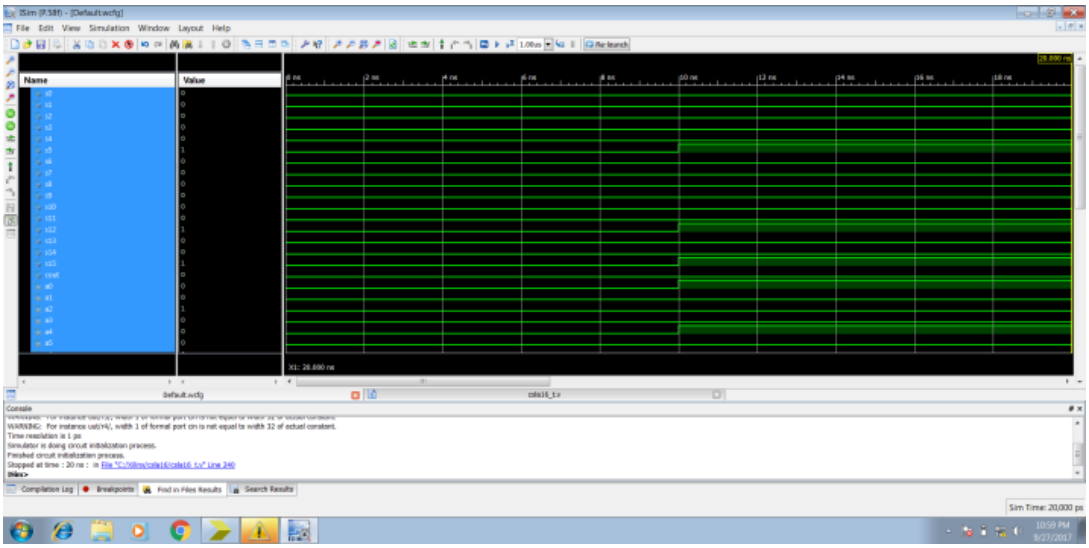


Fig.8 Area and delay of 128 bit linear CSLA

International Journal of Advance Research in Science and Engineering
Volume No.06, Issue No. 10, October 2017
www.ijarse.com
IJARSE
ISSN: 2319-8354

VIII. SIMULATION RESULTS



The design scheduled in this paper has been developed using Verilog-HDL and synthesised in Xilinx ISE. The simulation result for the above itemized 128 bit modified linear carry select adder is depicted using Xilinx software. The simulated files are trucked in to the synthesised tool and the corresponding values of delay and area are noted.

IX. CONCLUSION AND FUTURE WORK

This work presents a Efficient Architecture of modified linear Carry Select Adder simple approach to reduce the area, delay Design by Common Booleanand power of CSLA architecture.The conventional carry select adder has the disadvantage of more power consumption and occupying more chip area. The proposed CSLA using common Boolean logic has low power, less delay. The reduced number of gate of this work offers the great advantage in the optimisation of area and total power. By increasing the number of bits,the great shrinkage in the area and power can be scheduled.

REFERENCES

[1] AkhileshTyagi, "A Reduced Area Scheme for Carry-Select Adders", IEEE International Conference on Computer design, pp.255-258, Sept 1990

[2] BehnamAmelifard, FarzanFallah and MassoudPedram, "Closing the gap between Carry Select Adder and Ripple Carry Adder: a new class of low-power high-performance adders", Sixth International Symposium on Quality of Electronic Design, pp.148-152. April 2005.

[3] B.Ramkumar, Harish M Kittur and P.MaheshKannan, "ASIC implementation of Modified Faster Carry Save Adder", European Journal of Scientific Research, vol.42, pp.53-58, 2010

[4] J. M. Rabaey, "Digital Integrated Circuits- A Design Perspective", New Jersey, Prentice-Hall, 2001..

[5] KuldeepRawat, TarekDarwish. andMagdyBayoumi, "A low power and reduced area Carry Select Adder", 45th Midwest Symposium on Circuits and Systems, vol.1, pp. 467-470,March 2002.

[6] M.Moris Mano, "Digital Design", Pearson Education, 3rd edition, 2002.

[7] O. J. Bedrij, "Carry-Select Adder", IRE transactions on Electronics Computers, vol.EC-11, pp. 340-346, June1962.

[8] Youngjoon Kim and Lee-Sup Kim, "64-bit carry-select adder with reduced area", Electronics Letters, vol.37, issue 10, pp.614-615, May 2001.

[9]. T.-Y. Chang and M.-J. Hsiao,"Carry-Select Adder using single Ripple-Carry Adder", Electronics letters, vol.34, pp.2101-2103, October 1998.

[10] Youngjoon Kim and Lee-Sup Kim, "A low power carry select adder with reduced area", IEEE International Symposium on Circuits and Systems, vol.4, pp.218-221, May 2001.