

Design and Analysis of 4bit Array Multiplier using 45nm Technology:

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ABSTRACT

In digital signal processors multipliers play a major role because, high multiplication process is carried out in hardware part in digital circuits. Array multiplier also requires less space for implementation in ICs and is an efficient way of multiplication in digital integrated circuits [3-4]. In this paper we have designed and analysed a four bit array multiplier using 45nm CMOS process. Array multiplier consumes less power and is highly efficient in terms of speed. In this work a 4-bit array multiplier and its functionality is verified using Xilinx ISE Tool. In order to analyse the speed and power a 4-bit array multiplier is simulated using SPICE Tools with a supply voltage of 1volt the room temperature simulation results indicates the 4-bit multiplier consumes a power of 160 μ w and has a delay of 185pS for 45m CMOS process.

Keywords— array multiplier, , digital processor, full adders power and delay &45nm technology

I. INTRODUCTION

The demand for portable and embedded digital signal processing systems (DSP) has been increasing as a result of the speed growth of semiconductor technology and also due to the expanding of computers, televisions, computer aided gadgets and signal processing applications. Increasing the speed and reducing the power consumption are most essential requirements for present and next generation processors. The customization and optimization at all levels of the design is essential for the minimum usage of power consumption for all the digital integrated circuits and systems. The main optimization includes the semiconductor and its processing technology which is used to implement in the digital circuits, the circuit style and its topology and the architecture for implementing the circuits [6-9]. Digital multipliers are the commonly used circuits in applications such as digital signal processing for convolution, Fast Fourier Transform (FFT), digital filters and microprocessors in its arithmetic and logic unit. Increasing the speed is more essential since multiplication process dominates the execution time of most digital signal processing applications. In many digital signal processing applications, the multiplier lies in the critical delay path and ultimately determines the performance of the processor. The speed, delay and power consumption of Multipliers are more important in digital signal processors as well as in general processors since it dominates the chip power consumption and operation speed. There are architectures that are proposed in literature to perform multiplication, each offering different advantages and having trade off in terms of speed, power consumption, and area and circuit complexity. Let A0, A1, A2, A3 and B0, B1, B2, B3 be the two four bit binary numbers to be

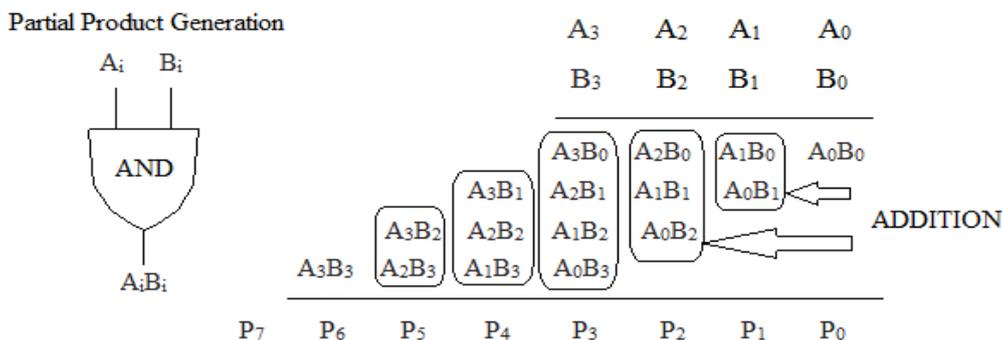


Fig-1 [conventional multiplication process] [10]

The above figure represents the conventional multiplication done at proper manner in above, the conventional array multiplier in multiplied in 4x4 multiplier and the outputs are P0, P1, P2, P3, P4, P5, P6 and P7.

II. ARCHITECTURE OF MULTIPLIER

The computation speed of blocks in digital signal processors (DSP) have increased dramatically over the past four decades resulting from the rapid advancement of various technologies. The execution speed of multipliers depends on two factors, one is the semiconductor technology used and the other is the multiplier architecture [5]. Multiplication process involves a more series of repeated additions. Therefore adders are the basic building blocks of digital multipliers. Increasing the speed of the adder, results in an increase in the speed of the multipliers. The area of the multipliers can be minimized by reducing the number of transistors required for implementing full adder circuits. Array multiplier has a unique and little modified process compared to conventional multiplication process. The proposed 4 bit array multiplier are discussed below,

III. PROPOSED 4-BIT ARRAY MULTIPLIER

The structure of 4 x 4 Bit Array Multiplier is shown in fig.2. and fig.3. The working array multiplier is based on the principle of shift and algorithm. In this Multiplier, the partial products can be generated using AND gates and the summation of partial products can be performed using Full Adders and Half Adders. In an $n \times n$ array multiplier, $n \times n$ and gates computes the partial products and the addition of partial products can be performed by using $n \times (n-2)$ full adders and n half adders [10]. The bit array multiplier is easy to design and it uses a pipelined architecture. Since the worst case delay of the bit array multiplier is proportional to the width of the multiplier, the speed performance will be degraded for wide fan-in multipliers

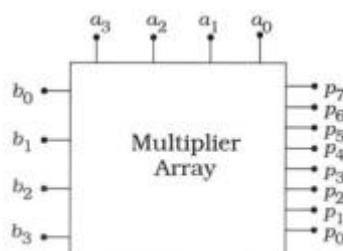


Fig-2 Array multiplier [2]

A. SCHEMATIC DIAGRAM OF ARRAY MULTIPLIER:

The Schematic diagram of 4 bit array multiplier is given below with a full schematic below:

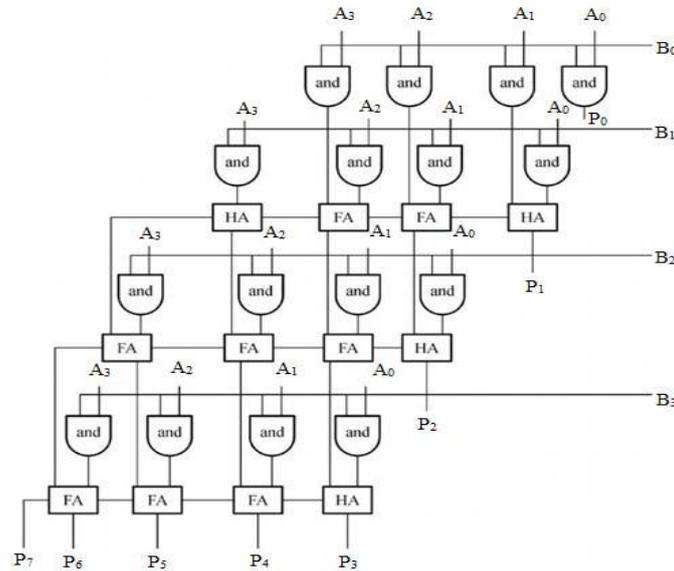


Fig.3 Schematic Diagram Representation [10]

B. SIMULATION RESULTS:

The simulations have been proven for 4-bit array multiplier through Xilinx ISE Tool and results are displayed below:

Case1: In this case we have given inputs and outputs as;

Input: A0=0; A1=0; A2=0; A3=0; B0=0; B1=0; B2=0; B3=0.

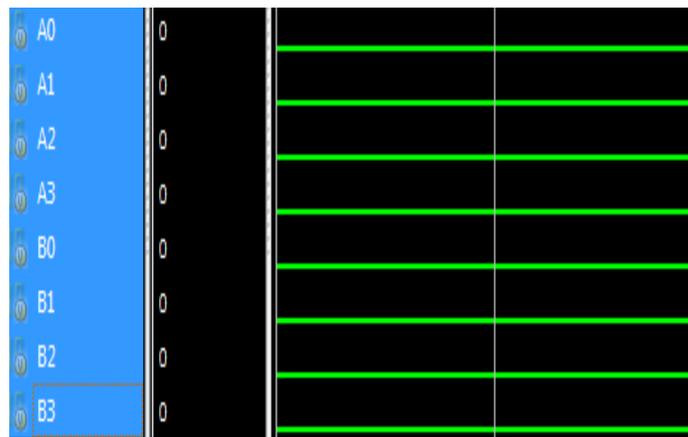


Fig.4 Input simulation Result

Output: P0=0; P1=0; P1=0; P2=0; P3=0; P4=0; P5=0; P6=0; P7=0:

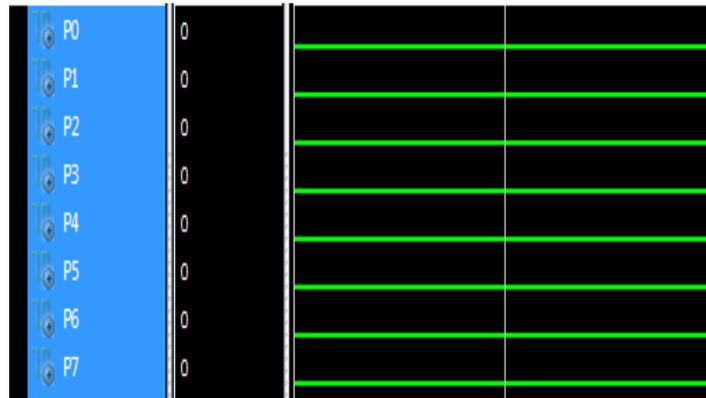


Fig.5 Output Simulation Result

Case2: In this case we have given inputs and outputs as;

Input: A0=1; A1=1; A2=1; A3=1; B0=1; B1=1; B2=1; B3=1.

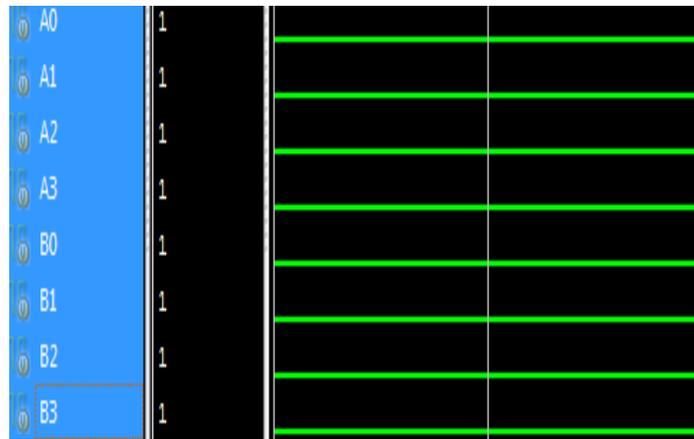


Fig.6 Input Simulation Result

Output: P0=1; P1=0; P1=0; P2=0; P3=0; P4=0; P5=1; P6=1; P7=1.



Fig.7 Input Simulation Result

Case3: In this case we have given inputs and outputs as;

Input: A0=0; A1=0; A2=1; A3=1; B0=0; B1=0; B2=1; B3=1.

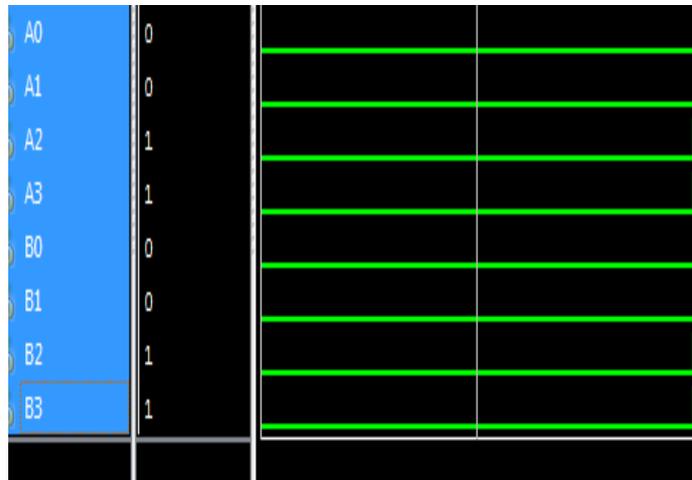


Fig.8 Input Simulation Result

Output: P0=1; P1=0; P2=0; P3=0; P4=0; P5=1; P6=1; P7=1.



Fig.9 Output Simulation Result

The Power and Delay characteristics are observed using SPICE Tool and the Results are verified they are displayed in TABLE-1:

Multiplier	Delay(pS)	Power(μ w)
Array Multiplier	185pS	160 μ w

IV. CONCLUSION:

Thus, In this paper we have designed and analyzed the 4-bit Array Multiplier using 45nm CMOS process its functionality were verified using Xilinx ISE Tool and its Power and Delay characteristics were calculated using SPICE Tools under 45nm CMOS process.



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KARTHIKEYAN.A received his B.Tech., degree specialized in Electronics and Communication Engineering in Bharathiyar College of Technology, Karaikal in the year 2008 under Pondicherry University, Pondicherry, and M.E., degree in VLSI Design in SNS College of Technology, Coimbatore in the year 2012 under Anna University, Chennai. He is now working as Assistant Professor in the Department of Electronics and Communication Engineering, SNS College of Technology, Coimbatore, Tamilnadu, India. Currently he is pursuing Ph.D. in Anna University, Chennai. His area of interest includes Wireless Sensor Networks, VLSI Design Techniques and Computer networking. He is a Life Member of the International Society for Research and Development (MISRD), International Association of Engineers (MIAENG) and International Association of Computer Science and Information Technology (MIACSIT).



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