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Multi-Threshold Based Low Power Dual Edge Triggered Flip-Flop

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ABSTRACT

Digital circuit design is streamlined process used to improve the performance of a circuit for a particular application. Fast speed, minimum power dissipation and less area are the desirable characteristics of a digital circuit, in general. To meet a particular standard of speed, a compromise in power dissipation and speed is required. Timing elements such as Flip-flop are used as clock generators. These consume almost 50% of the total system power. In this paper, a low power dual edge triggered D flip-flop is proposed. The circuit complexity is reduced by using less number of transistors. Multi-threshold technique is employed to reduce the power dissipation of the proposed circuit.

Keywords: Double Edge Triggered, Low Power, Multi-threshold, Single Edge Trigger.

I. INTRODUCTION

In electronics, Flip-flop (FF) is a circuit which stores the information in the form of digits in all digital circuits. There are two types of flip-flop, One is single edge triggered (either positive or negative edge triggered) and other is double edge triggered (both positive edge and negative edge triggered). Flip-flop consists of pulse generator for strobe signal and a latch is used to store data. If the clock pulses are narrow then latch works as an edge triggered flip-flop. Conventionally, Single Edge Triggered (SET) flip-flop implemented as two oppositely phased latch triggered either on rising edge or falling edge. During first half cycle first latch loads data and passes to second latch during the next half cycle. Hence, SET flip-flop becomes ideal at one edge. Hence, Double Edge Triggered (DET) flip-flops are designed to overcome this drawback. Double edge triggered (DET) flip-flop provides same data as single edge triggered flip-flop at half the clock frequency [1]. In other words we can say, DET flip-flop works on lower clock frequency than SET. It become better to use DET flip-flop as consumes less power and becomes faster than SETFF. Power consumed by flip-flop is the major concern and there are three major sources of the power dissipation in digital CMOS circuits as summarized in following equation

$$P_{total} = P_t(C_L.V.V_{dd}.f_{clk}) + I_{sc}.V_{dd} + I_{leakage}.V_{dd} \quad (1)$$

First term shows us a switching component of power, where f_{clk} is clock frequency; C_L is the loading capacitance and the probability that a power consuming transition occurs also known as activity factor (α) [2]. Mostly voltage swing V is same as supply voltage V_{dd} and the second term is due to direct path short circuit current, I_{sc} which occurs when both NMOS and PMOS transistors are simultaneously active. The third term, represents leakage current $I_{leakage}$ which originates from substrate injection and subthreshold effects.

One of the major factors to reduce power consumption is supply voltage V_{dd} upto a certain level. It cannot be reduced below the threshold values of transistors. Before scaling of supply voltage, circuit behaviour must be

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reviewed in terms of delay and energy characterstics because there will be effect on delay and power delay product (PDP_{DQ}) as energy per transition is directly proportional to V^2 as equation shows $P = C_L \cdot V_{dd}^2 \cdot f_{clk}$, Hence, power consumption reduces as quadratic function of supply voltage reduction [3].

Further, Multithreshold technique can also be introduced to decrease power consumption as well as leakage current, while maintaining the speed. Multi-threshold CMOS is a technique mainly used for leakage current. The important and different feature of multithreshold CMOS is that it uses both low and high threshold voltage transistors on a single chip. In this paper, a Low power dual edge triggered flip-flop with multithreshold technique is proposed.

II. EXISTING DESIGN OF DUAL EDGE TRIGGERED FLIP-FLOP

2.1. Conventional Dual Edge Triggered Flip-flop (CDE-FF)

Figure 2.1(a) is a dual edge triggered static pulsed flip-flop (DSPFF), It consists of clock signal generator [4] [5]. In clock pulse generator, four inverters are used to delay the clock signal. These delayed clock signals are used to generate sampled signals at both rising and falling edge of the clock pulse by using two pass transistors M1 and M2. In latch, data is applied to RB (Reset bit) and SB (Set bit) nodes through another two pass transistors M5 and M6 are controlled with clock pulse. In circuit there are two PMOS and two weak NMOS transistors are used to prevent from floating signals at RB and SB nodes. Because of static nature of latch, it circumvents the unessential transitions which reduce power consumption but there is drawback of the circuit that it mostly consumes power because of its leakage current [6]. For the same delays at the output, W/L ratio must be adjusted and hence distortion occurs in the output at Q and QB if less voltage is applied to the circuit because of RB and SB nodes which cannot be charged more than the gate drive voltage (V_{dd}-V_{th}).

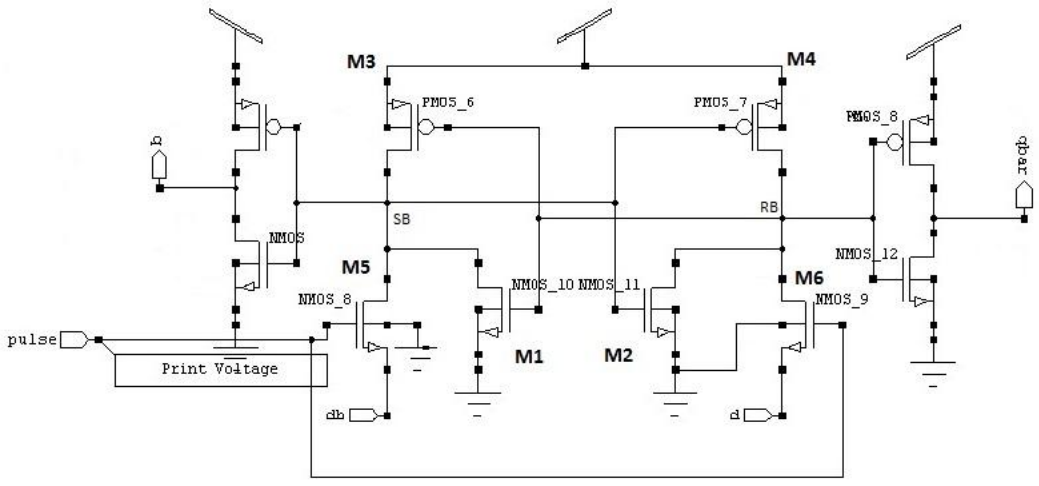

Fig 2.1(a) Circuit diagram of CDE-FF

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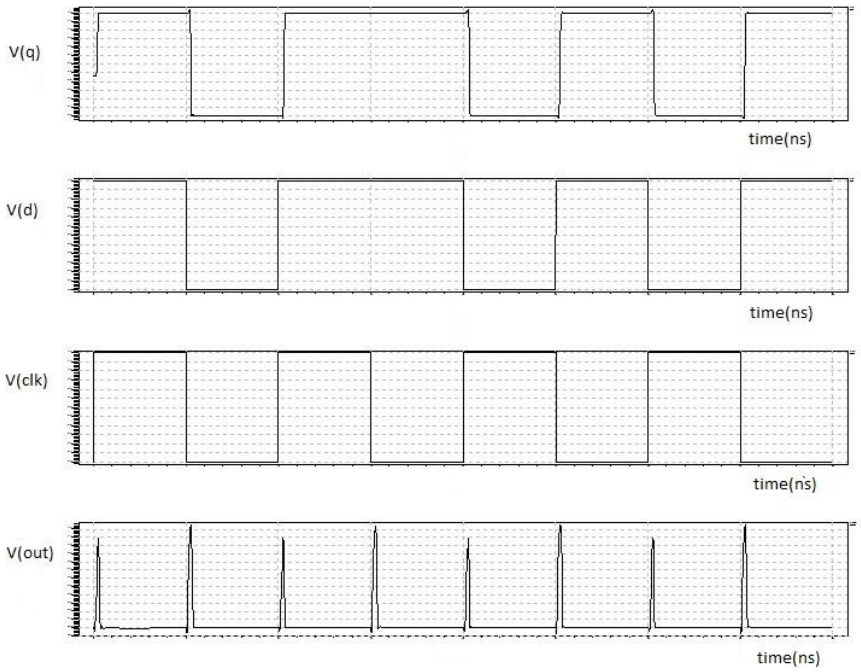

Fig. 2.1(b) Output waveform for CDE-FF

The figure 2.1(b) shows the output waveform of conventional dual edge triggered flip-flop (CDE-FF). There are four waveforms of clock pulse generator output V(out), clock pulse input signal V(clk), Data V(d) input bit pattern and V(q) output waveform of flip-flop. Some fixed delays are present in output V(q).

2.2. Asynchronous Set-Reset D Flip-flop (ASRD-FF)

The master slave D flip-flop is easily realized by cascading two latches that are clocked on opposite phases. If the master latch needs HIGH clock signal then slave gives output as LOW clock Signal. One example of this is shown in figure 2.2(a), where the latch based on cross coupled NOR gates is used [7]. The flip flop also has asynchronous set-reset inputs added in which only one of these asynchronous inputs is required. The unnecessary transistors used for the other asynchronous input can be left off. During operation, when the state of the master is changing state, it is necessary to pull one side low before the other side can go high. For this to be possible it is necessary to size the transistors correctly, similar to what is necessary for the clocked latches. Two additional inverters are added to buffer the output. These are sometimes needed because of the large capacitive loads that flip-flops often have to drive. To simplify the circuit, set reset asynchronous signals can be removed but when required these can be easily added. Also, note that the load transistors of the master latch had to be taken somewhat smaller to still allow the n-channel drive networks, which now consist of three series transistors, to dominate when changing the state of the latch [8].

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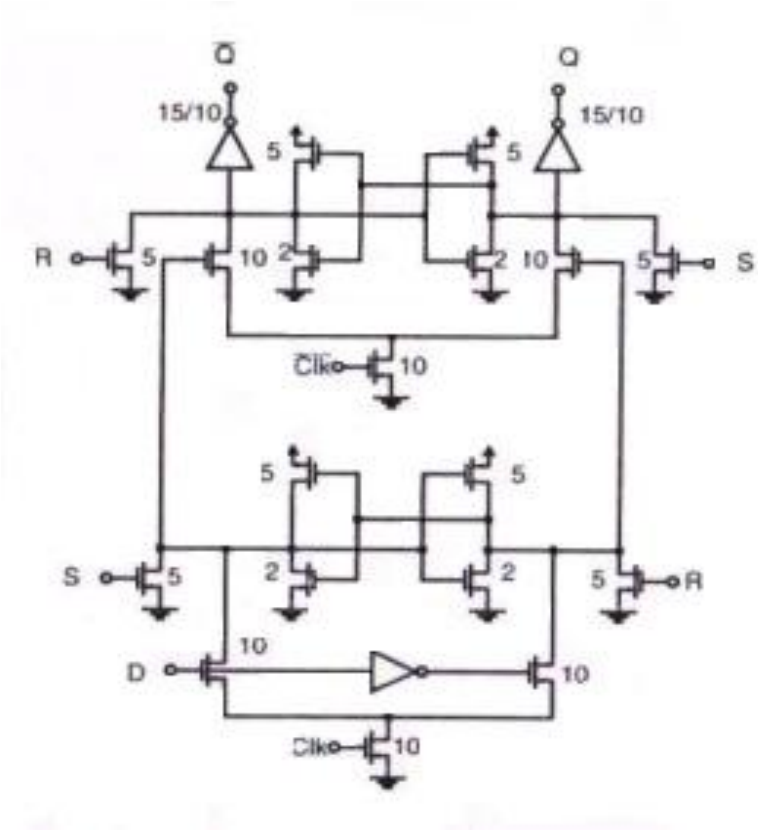

Fig. 2.2(a) circuit diagram for ASRD-FF [7]

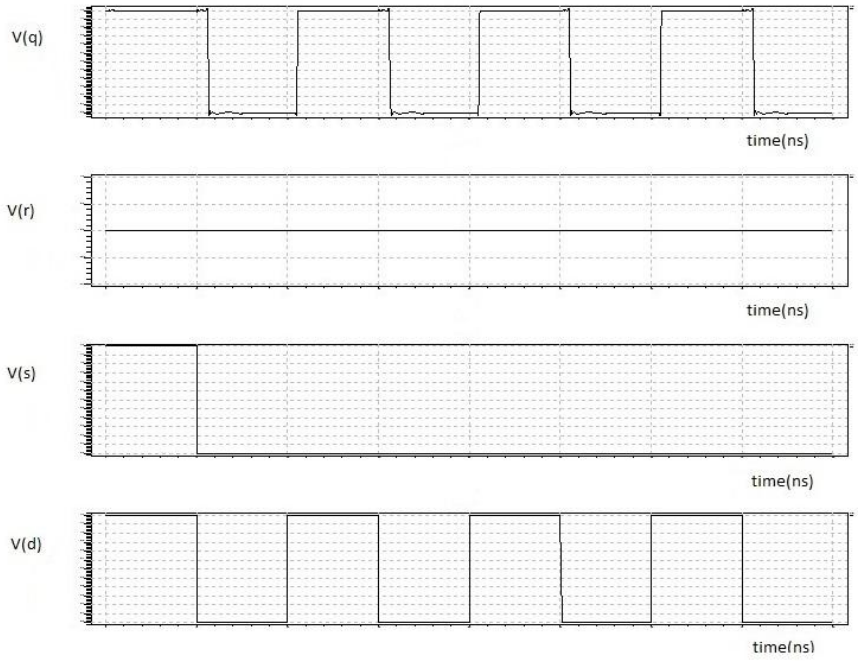

Fig. 2.2(b) Output waveform for ASRD-FF

The output waveform is shown in figure 2.2(b) as Data input signal V(d), Set signal V(s), Reset signal V(r) and V(q) output of the flip-flop. As the data (10101010) is applied to the D input, same V(q) output shows with some fixed delay. In the asynchronous set reset flip-flop here only set signal becomes high during first clock

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period and output gets a start signal. If the data (01010101) has to be displayed at the output then first or starting HIGH bit will be applied to reset input node and set input node will be at LOW state.

2.3. Proposed Transmission Gate Based D Flip-Flop (T-DETFF)

In previous circuits, there are number of transistors used for pulse generation circuit to achieve the proper functionality. Most of them are associated to clock signal, which increases activity factor α, and hence is the reason for high power consumption. Hence, dual data path technique is introduced to reduce number of transistors [9]. To reduce the unwanted voltage threshold effects, transmission gates are used which prevents to lead weak logic signals in pass transistors.

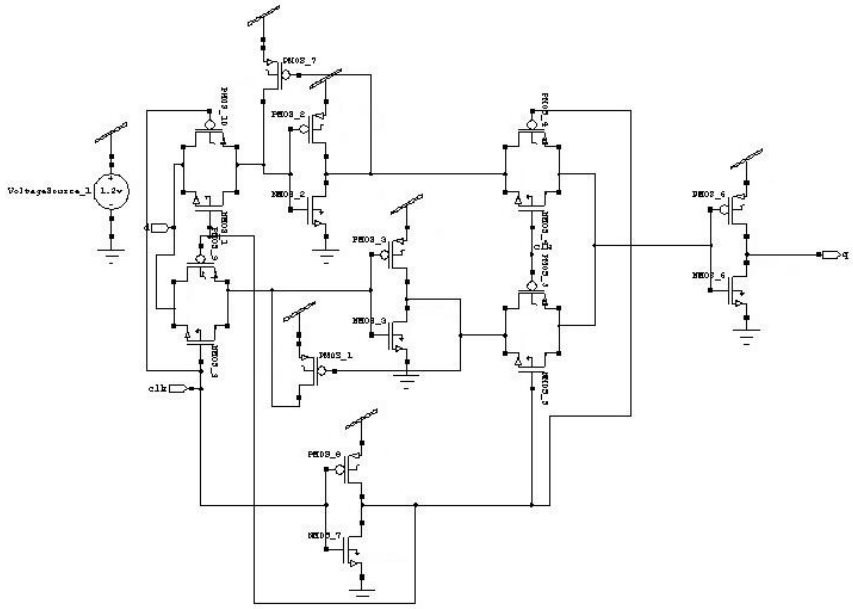

Fig. 2.3(a) circuit diagram for T-DETFF

As shown in figure 2.3(a), there are two data paths, upper data path triggers at positive edge and lower data path triggers at negative edge of clock pulse. Function of combined PMOS and an inverter circuit is to hold the logic when forepart transmission gate is closed. As the logic at data is high, the NOT gate inverts it to low hence PMOS transistor becomes ON which pulls up data to high. As data value is low, NOT gate inverts it to high logic level. Hence, PMOS transistors remains OFF because of that data value remain low as data isolates from V_{dd} power supply. Due to less number of transistors, less area is required to implement it. Output power is calculated at 1.2V V_{dd} power supply and eight bit data is applied to input.

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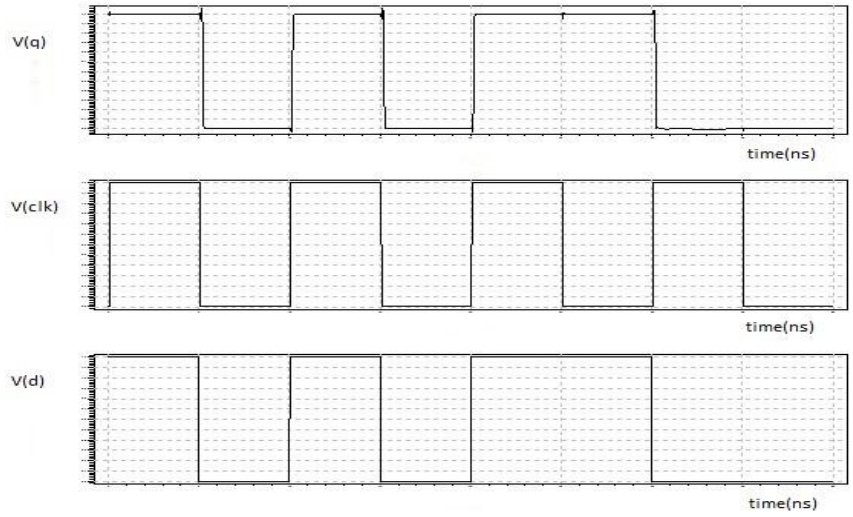

Fig. 2.3(b) Output waveform for T_DETFF

In Fig 2.3(b) waveform shows that applied input bits to D is same as at Q output while the clock pulse applied to clk input. The flip-flop triggers at both edges (rising edge as well as falling edge) hence called as double edge trigger flip-flop. There must be some delay is always present at the Q output with respect to input D signal [10].

III. RESULTS AND DISCUSSIONS

The performance of the proposed flip-flop design is analyzed and compared with conventional flip-flop designs. Table 1 present's comparison of result for conventional dual edge triggered flip-flop, an asynchronous Set-Reset D flip-flop and the proposed transmission gate based D flip-flop. A Conventional Dual Edge Triggered flip-flop (CDE-FF) uses clock generator design with a four-stage inverter chain whereas the proposed transmission gate based D flip-flop design does not need extra number of transistors. Hence, it requires less number of transistors because of which it saves power, which was consumed by unnecessary transistors. This becomes an advantage over other flip-flop circuits.

The proposed flip-flop can be used in 16 bit counter for future testing in integrated circuit. The circuit designs are simulated using tool EDA Tanner 13.0 simulation tool with 1.2 V supply voltage at room temperature 300 K. A fixed value of capacitor at 100fF is used as load capacitance. Clock frequency used in the proposed flip-flop design is 100MHz and this frequency is same as 200MHz clock frequency in Single Edge Triggered flip-flop (SET-FF). The simulation are carried at T-spice 130nm CMOS process. Six different bit patterns (α=0% for both all 1's and all 0's, α=25%, α=50%, α=100%) each representing a different switching probability, are applied in simulations.

Table 1 Comparison of Various Flip-Flop Designs

Various flip flop designs	Conventional Dual Edge Triggered Flip-Flop (CDE-FF)	Asynchronous Set Reset D Flip- Flop (ASRD-FF)	Proposed Transmission Gate Based DETFF (T_DETFF)
Number Of Transistors	22	38	18
D TO Q delay (ps)	153.32	1062.3	372.87
Power Consumption(µw)	38.13	29.074	28.23

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α=100% (10101010)			
Power Consumption(µw) α=50% (11110000)	22.40	12.291	9.69
Power Consumption(µw) α=25% (11000000)	24.33	12.286	9.723
Power Consumption(µw) α=0% (when all 0's)	20.03	10.57	6.30
Power Consumption(µw) α=0% (when all 1's)	20.036	9.52	6.01
Area (μm^2)	6.875	13.987	6.80

Table 1 summarizes that there are less number of transistors used in T-DETFF as compared to CDE-FF and ASRD-FF, Hence require less area in CMOS integrated circuit to implement. Comparing the Proposed design with CDE-FF, power saving by T_DETFF is 25.96%, 56.74%, 60.03%, 68.54%,70.00% when the activity factor α=100%, α=50%, α=25%, α=0%(for all 0's), α=0%(for all 1's), respectively.

Comparing Proposed design T_DETFF with ASRD-FF, Power saving of T_DETFF is 2.90%, 21.16%, 20.86%, 36.86%, 40.39% when the activity factor α=100%, α=50%, α=25%, α=0%(for all 1's), α=0%(for all 0's) respectively. When the switching activity factor α is 0%, then proposed design is more power economical against both flip-flops (CDE-FF and ASRD-FF). The D to Q delay of ASRD-FF flip-flop is very large when compared with both CDE-FF and T-DETFF [11][12].

The CDE-FF consumes more power as compared to both ASR-FF and T-DETFF. Proposed design will be cheaper as compared to ASRD-FF and CDE-FF because of its less area, VLSI chip can be designed with more number of flip-flops due to compact sizing.

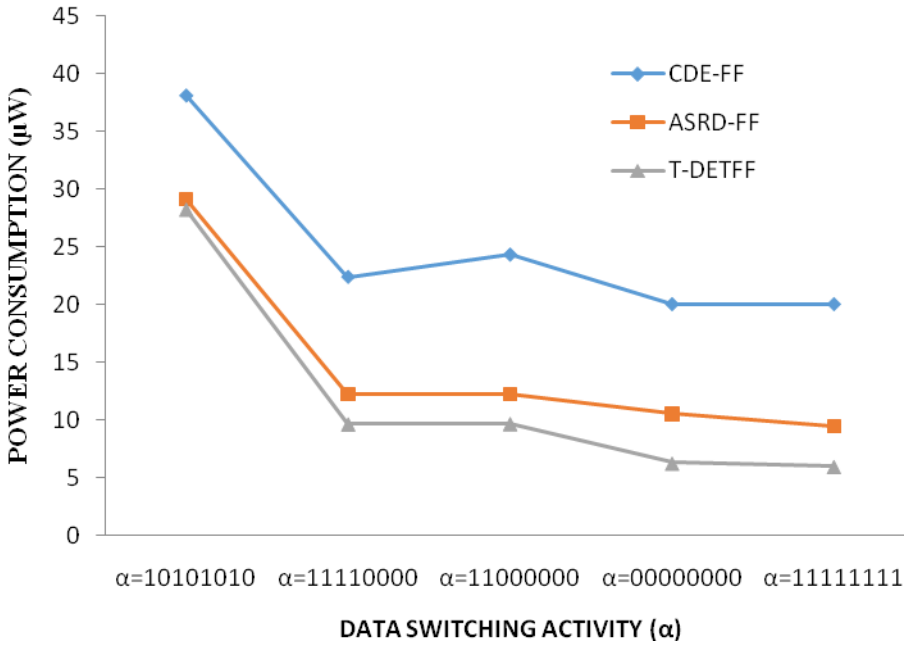

Fig-3(a) Power vs Data switching activity factor (α)

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Fig 3(a) shows graph of power Vs activity factor (α) for all three designs studied in this paper. Minimum power consumption occurs when there is no switching of data bits or we can say zero switching activity factor (α=0% for all 1's and for all 0's).

3.1. Power Delay Product

PDP_{DQ} is correlated with energy efficiency of the logic gate. It has dimensions of energy and measures energy consumed per switching event. After analysis of performance, Compromise in power delay product (PDP_{DQ}) is always required for the low power applications and high performance factors as both are equally valuable.

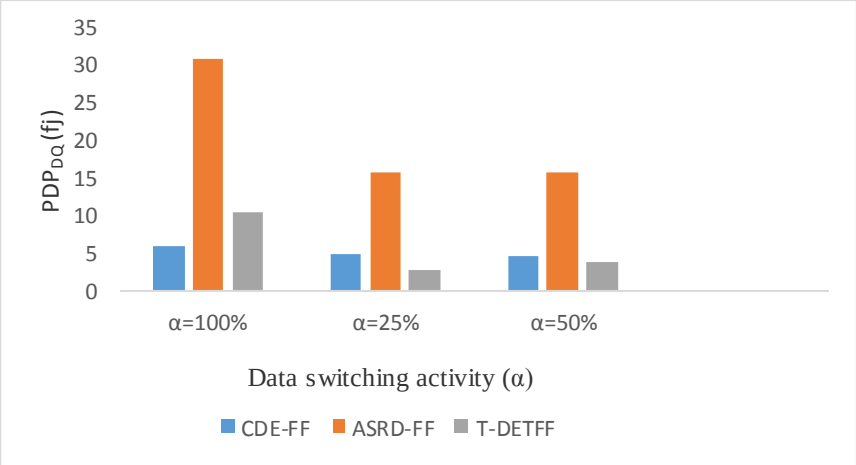

Fig 3(b) PDP_{DQ} vs Data switch activity

Figure 3(b) Shows the simulation results of PDP_{DQ} vs data switch activity. The PDP values of proposed design are smaller than the other designs for all data switching activity (α), except for α=100%, where PDP_{DQ} is higher a compared to CDE-FF because of its more time delay as compared to CDE-FF.

3.2. Multi-threshold T_DETFF

Due to technology advancement in digital electronics, we need to reduce threshold voltage as reduction in supply voltage to decrease the power consumption and multithreshold CMOS technique is used to decrease leakage current. The circuit consists of two different set of transistors, first which conducts on High threshold voltage also renamed as "sleep transistors" and another Low threshold transistors are the part of logical circuit [13]. To reduce leakage current, sleep transistors disconnect the logic circuit from power supply.

Table 2 Power and Delay of Multi-Threshold T_DETFF

Proposed Transmission gate Based Dual Edge Triggered Flip-flop (T_DETFF)	threshold voltage of NMOS= +0.08V and PMOS= -0.21V	threshold voltage of NMOS= +0.18V and PMOS= -0.36V
Power (µw) @α=100% (10101010)	29.25	28.25
Power (µw) @α=50% (11000000)	14.64	10.654
Power (µw) @α=25% (11110000)	13.71	11.55
Power (µw) @α=0% (for all 0's)	6.28	6.25
Power (µw) @α=0%(for all 1's)	6.133	6.11
D to Q delay (ps) (for α=50%)	226.43	331.66

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Table 2 Shows the power comparison of Multi-threshold T_DETFF after changing threshold voltages from NMOS (+0.08V) and PMOS (-0.21V) to NMOS (+0.18V) and PMOS (-0.36V). The increase in threshold voltage results in decrease in power consumption but there is small increase in D to Q delay [14] [15].Therefore Low threshold voltage transistors are mostly preferable which requires less supply voltage.

Multithreshold voltage changes are included in model files of NMOS and PMOS transistors. Circuit is simulated by include two library files (one is for Low threshold transistors and other is for High) simultaneously in EDA Tanner. NMOS1 and PMOS1 names are used for HIGH threshold NMOS and PMOS transistors respectively in a modified model file for simulation. Power saving by High threshold T_DETFF is 3.41%, 27.22%, 15.75%, 0.47%, 0.37% when activity factor α=100%, α=50%, α=25%, α=0% (for all 0's), α=0% (for all 1's) respectively in comparison to the earlier design summarized in Table 1. Hence the maximum power saving occurs when the activity factor is α=50%.

IV. CONCLUSION

In this paper, the power is reduced by using multithreshold voltage transistors. Firstly, the Power, D to Q delay of existing designs is calculated having same threshold voltage of all NMOS transistors and same in case of PMOS transistors. Then, By changing threshold voltage of particular transistors that are named as NMOS1 and PMOS1, We analyze that there is 27.22% decrease in power consumption for 50% switching activity factor (α) but delay increases upto 46.47%. The result has shown that the multithreshold technique can be used for low power application having compromise with speed. Better Speed can also be achieved by reducing threshold voltage of transistors using this technique.

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