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A High Step-Down Transformerless Single-Stage Single-Switch AC/DC Converter

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ABSTRACT

This paper presents a high step-down tranformerless single-stage single-switch ac/dc converter suitable for universal line applications (90–270 Vr m s). The topology integrates a buck-type power-factor correction (PFC) cell with a buck–boost dc/dc cell and part of the input power is coupled to the output directly after the first power processing. With this direct power transfer feature and sharing capacitor voltages, the converter is able to achieve efficient power conversion, high power factor, low voltage stress on intermediate bus (less than 130 V) and low output voltage without a high step-down transformer. The absence of transformer reduces the component counts and cost of the converter. Unlike most of the boost-type PFC cell, the main switch of the proposed converter only handles the peak inductor current of dc/dc cell rather than the superposition of both inductor currents. Detailed analysis and design procedures of the proposed circuit are given and verified by experimental results.

Index Terms—Direct power transfer (DPT), integrated buck– buck–boost converter (IBuBuBo), power-factor correction (PFC), single-stage (SS), transformerless.

I. INTRODUCTION

INGLE-STAGE (SS) ac/dc converters have received much Sattention in the past decades because of its cost effective-ness, compact size, and simple control mechanism. Among ex-isting SS converters, most of them are comprised of a boost power-factor correction (PFC) cell followed by a dc/dc cell for output voltage regulation [1]–[7]. Their intermediate bus voltage is usually greater than the line input voltage and easily goes be-yond 450 V at high-line application [8]. Although there are a lot of efforts to limit this bus voltage, it is still near or above the peak of the line voltage due to the nature of boost-type PFC cell. For application with low output voltage (e.g., ≤48V), this high inter-mediate bus voltage increases components stresses on the dc/dc cell. With a simple step-down dc/dc cell (i.e. buck or buck–boost converter), extremely narrow duty cycle is needed for the con-version. This leads to poor circuit efficiency and limits the input voltage range for getting better performance [9], [10]. Therefore, a high step-down transformer is usually employed even when galvanic isolation is not mandatory. For example, LED drivers without isolation may satisfy safety requirement [11]. Also, in some multistage power electronics system (e.g., in data center, electrochemical and petrochemical industries, and subway ap-plications [12]), the isolation has been done in the PFC stage, the second transformer in the dc/dc cell for the sake of isolation is considered as redundant. Hence, nonisolated ac/dc converter can be employed to reduce unnecessary or redundant isolation and enhance efficiency of the overall system. Besides, leakage inductance of the transformer causes high spike on the active switch and lower conversion efficiency. To protect the switch, snubber circuit is usually added resulting in more component counts [13]. In addition, the other

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drawbacks of the boost-type PFC cell are that it cannot limit the input inrush current and provide output short-circuit protection [14]. To tackle the aforementioned problems, an effective way is to reduce the bus voltage much below the line input voltage. Several topologies have been reported [9], [10], [13], [15]–[18]. Although the recently reported IBoBuBo converter [13] is able to limit the bus voltage under 400 V, it cannot be applied to the low-voltage application directly due to the boost PFC cell. On the other hand, the converters [9], [10], [15]–[18] employ dif-ferent PFC cells to reduce the intermediate bus voltage. Among those converters, [9] and [15] use a transformer to achieve low output voltage either in PFC cell or dc/dc cell. Therefore, the leakage inductance is unavoidable. In [10], [17], and [18], the converters employ a buck–boost PFC cell resulting in negative polarity at the output terminal. In addition, the topologies in [18] and [10] process power at least twice resulting in low power ef-ficiency. Moreover, the reported converters, in [16], and [17], consist of two active switches leading to more complicated gate control. Apart from reducing the intermediate bus voltage, the con-verter in [19] employs resonant technique to further increase the step-down ratio based on a buck converter to eliminate the use of intermediate storage capacitor. The converter features with zero-current switching to reduce the switching loss. However, without the intermediate storage, the converter cannot provide hold-up time and presents substantial low-frequency ripples on its output voltage. Besides, the duty cycle of the converter for high-line input application is very narrow, i.e., < 10%. This greatly increases the difficulty in its implementation due to the minimum on-time of pulse-width-modulation (PWM) IC and rise/fall time of MOSFET. More details on comparing different approaches will be given in the Section V.

In this paper, an intergrated buck–buck–boost (IBuBuBo) converter with low output voltage is proposed. The converter utilizes a buck converter as a PFC cell. It is able to reduce the bus voltage below the line input voltage effectively. In addition, by sharing voltages between the intermediate bus and output capacitors, further reduction of the bus voltage can be achieved.

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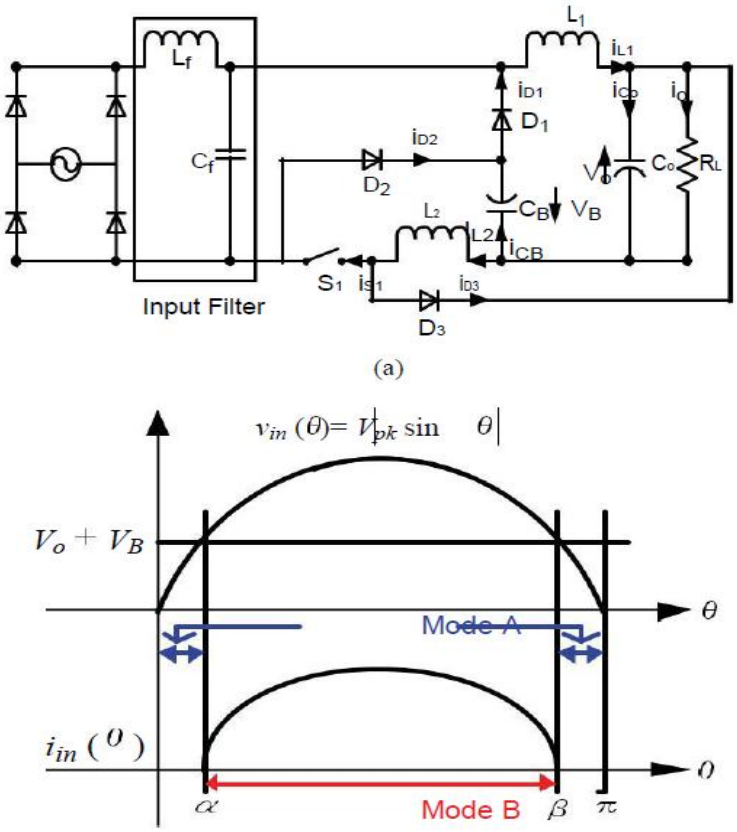

Fig. 1. (a) Proposed IBuBuBo SS ac/dc converter. (b) Input voltage and current waveforms.

Therefore, a transformer is not needed to obtain the low output voltage. To sum up, the converter is able to achieve:

1) low intermediate bus and output voltages in the absence of transformer;

2) simple control structure with a single-switch;

3) positive output voltage;

4) high conversion efficiency due to part of input power is processed once and

5) input surge current protection because of series connection of input source and switch.

The paper is organized as follows: operation principle of the proposed IBuBuBo converter is depicted in Section II and fol-lowed by design consideration with key equations in Section III. Experimental result and discussion of the converter are given in Section IV and V, respectively. Finally, conclusion is stated in Section VI.

II. PROPOSED CIRCUIT AND ITS OPERATING PRINCIPLE

The proposed IBuBuBo converter, which consists of the merging of a buck PFC cell (L_1 , S_1 , D_1 , C_o , and C_B) and

a buck–boost dc/dc cell (L_2, S_1 , D_2 , D_3, Co, and C_B) is il-lustrated in Fig. 1(a). Although L_2 is on the return path of the buck PFC cell, it will be shown later in Section III-A that it does not contribute to the cell electrically. Thus, L_2 is not con-sidered as in the PFC cell. Moreover, both cells are operated in discontinuous conduction mode (DCM) so there are no currents in both inductors L_1 and L_2 at the beginning of each switching cycle t0 . Due to the characteristic of buck PFC cell, there are two operating modes in the circuit.

Mode A (v_{in} (θ) ≤ V_B + V_o): When the input voltage v_{in} (θ) is smaller than the sum of intermediate bus voltage V_B , and output voltage V_o , the buck PFC cell becomes inactive and does not shape the line current around

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zero-crossing line voltage [20], owing to the reverse biased of the bridge rectifier. Only the buck–boost dc/dc cell sustains all the output power to the load. Therefore, two dead-angle zones are present in a half-line period and no input current is drawn as shown in Fig. 1(b). The circuit operation within a switching period can be divided into three stages and the corresponding sequence is Fig. 2(a),(b), and (f). Fig. 3(a) shows its key current waveforms.

1) Stage 1 (period d_1 Ts in Fig. 3) [see Fig. 2(a)]: When switch S_1 is turned ON, inductor L_2 is charged linearly by the bus voltage V_B while diode D_2 is conducting. Output capacitor Co delivers power to the load.

2) Stage 2 (period d_2 Ts in Fig. 3) [see Fig. 2(b)]: When switch S_1 is switched OFF, diode D_3 becomes forward biased and energy stored in L_2 is released to C_o and the load.

3) Stage 3 (period d_3 T_s - d_4 T_s in Fig. 3) [see Fig. 2(f)]: The inductor current $i_{L\ 2}$ is totally discharged and only C_o sustains the load current.

Mode B (v_{in} (θ) > V_B + V_o): This mode occurs when the input voltage is greater than the sum of the bus voltage and output voltage. The circuit operation over a switching period can be divided into four stages and the corresponding sequence is Fig. 2(c), (d), (e), and (f). The key waveforms are shown in Fig. 3(b).

1) Stage 1 (period d_1 T_s in Fig. 3) [see Fig. 2(c)]: When switch S_1 is turned ON, both inductors L_1 and L_2 are charged linearly by the input voltage minus the sum of the bus voltage and output voltage (v_{in} (θ) − V_B − V_o), while diode D_2 is conducting.

2) Stage 2 (period d_2 T_s in Fig. 3) [see Fig. 2(d)]: When switch S_1 is switched OFF, inductor current $i_{L\ 1}$ decreases linearly to charge C_B and C_o through diode D_1 as well as transferring part of the input power to the load directly. Meanwhile, the energy stored in L_2 is released to C_o and the current is supplied to the load through diode D_3 . This stage ends once inductor L_2 is fully discharged.

3) Stage 3 (period d_3 T_s in Fig. 3) [see Fig. 2(e)]: Inductor L_1 continues to deliver current to C_o and the load until its current reaches zero.

4) Stage 4 (period d_4 T_s in Fig. 3) [see Fig. 2(f)]: Only C_o delivers all the output power.

III. DESIGN CONSIDERATIONS

To simplify the circuit analysis, some assumptions are made as follows:

1) all components are ideal;

2) line input source is pure sinusoidal, i.e. v_{in} (θ) = $V_{p\ k}$ sin(θ) where $V_{p\ k}$ and θ are denoted as its peak voltage and phase angle, respectively;

3) both capacitors C_B and C_o are sufficiently large such that they can be treated as constant DC voltage sources without any ripples;

4) the switching frequency f_s is much higher than the line frequency such that the rectified line input voltage |v_{in} (θ)| is constant within a switching period.

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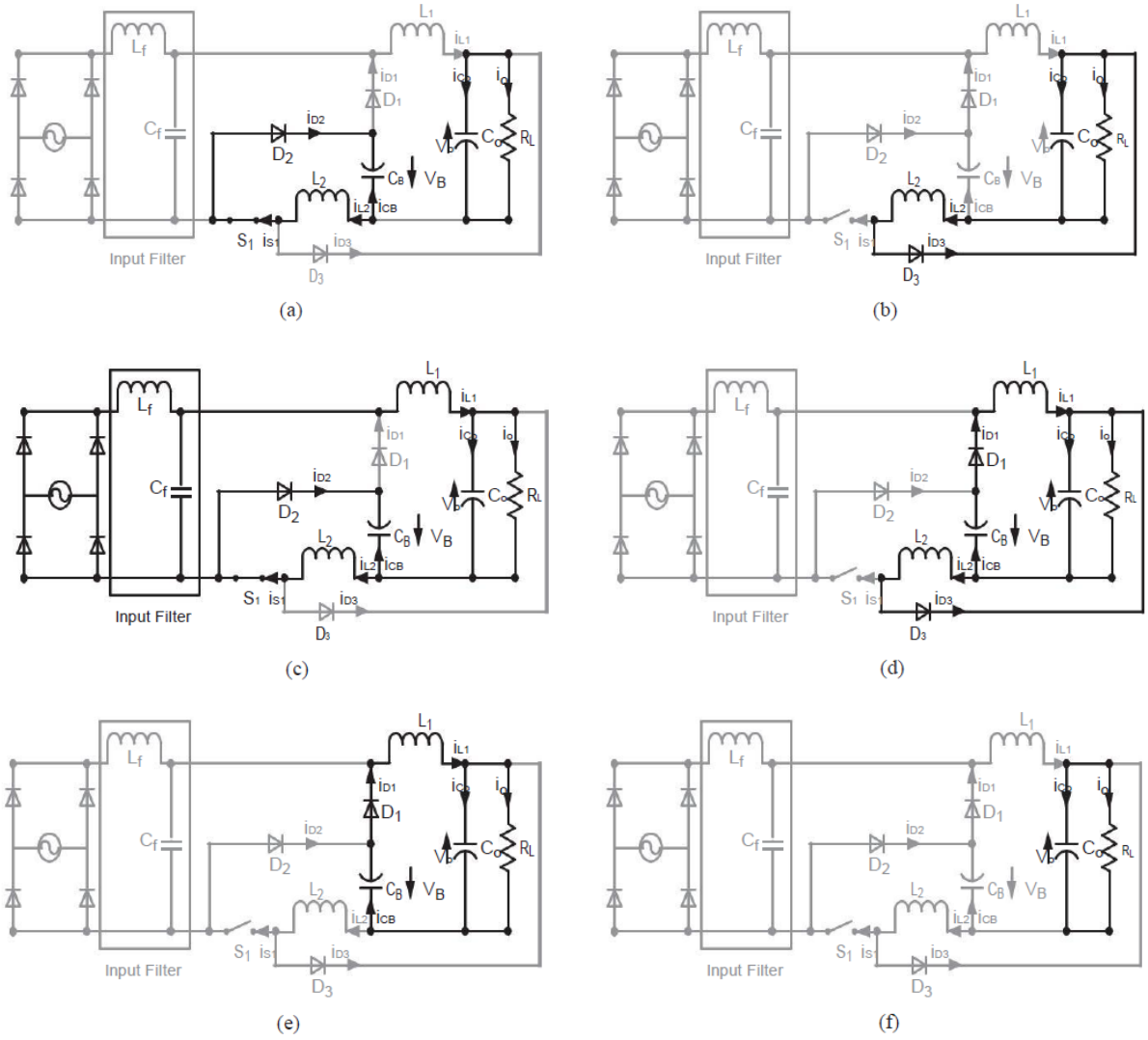

Fig. 2. Circuit operation stages of the proposed ac/dc converter.

A. Circuit Characteristics

According to Fig. 1(b), there is no input current drawn from the source in Mode A, and the phase angles of the dead-time α and β can be expressed as

$$\alpha = \arcsin \frac{V_T}{V_{pk}}$$

$$\beta = \pi - \alpha = \pi - \arcsin \frac{V_T}{V_{pk}} \quad (1)$$

where V_T is the sum of V_B and V_o . Thus, the conduction angle of the converter is

$$\gamma = \beta - \alpha = \pi - 2\arcsin \frac{V_T}{V_{pk}} . \quad (2)$$

From the key waveforms (see Fig. 3), the peak currents of the two inductors are

$$i_{L1pk} = \begin{cases} \frac{V_{in}(\theta) - V_T}{L_1} d_1 T_S, & \alpha < \theta < \beta \\ 0, & \text{otherwise} \end{cases} \quad (3)$$

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and

$$I_{L2\_pk} = \frac{V_B}{L_2} d_1 T_s \qquad (4)$$

where T_s ($1/f_s$) is a switching period of the converter. In (3) and (4), the dependency of i_{L1} pk on θ has been omitted for clarity. It is noted that L_2 does not contribute in (3) even though it is on the current return path of the PFC cell.

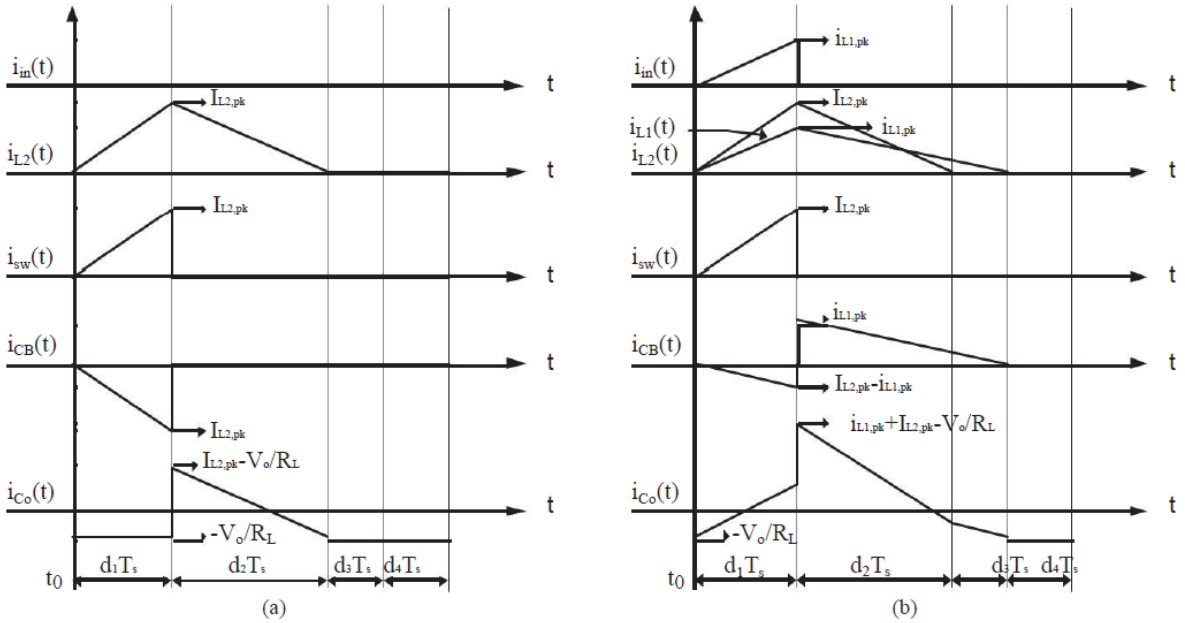

Fig. 3. Key waveforms of the proposed circuit

In addition, by considering volt–second balance of the L_1 and L_2, respectively, the important duty ratio relationships can be expressed as follows:

$$d_2 + d_3 = \begin{cases} \frac{V_{in}(\theta) - V_T}{V_T} d_1, & \alpha < \theta < \beta \\ 0, & \text{otherwise} \end{cases} \qquad (5)$$

By applying charge balance of C_B over a half-line period, the bus voltage V_B can be determined. From Fig. 3, the average current of C_B over a switching and half-line periods are expressed

$$\langle i_{CB} \rangle_{sw} = \frac{1}{2}(i_{L1\_pk}(d_1 + d_2 + d_3) - I_{L2\_pk} d_1) = \frac{d_1^2 T_s}{2} \frac{(V_{in}(\theta) - V_T)V_{in}(\theta)}{L_1 V_T} \frac{V_B}{L_2} \qquad (7)$$

and

$$\langle i_{CB} \rangle_{\pi} = \frac{1}{\pi} \int_0^{\pi} \langle i_{CB} \rangle_{sw} d\theta = \frac{d_1^2 T_s}{2\pi} \frac{V_{pk}}{L_1} V_T \left(\frac{\gamma}{2} + \frac{A}{4}\right) - B - \frac{\pi V_B}{L_2} \qquad (8)$$

where the constants A and B are

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$$A = \sin(2\alpha) - \sin(2\beta) \quad (9)$$

$$B = \cos(\alpha) - \cos(\beta). \quad (10)$$

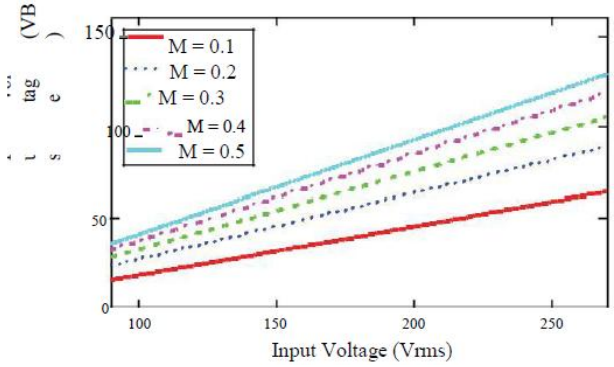

Fig. 4. Calculated intermediate bus voltage under different inductance ratios.

Putting (8) to zero due to the steady-state operation, this leads to

$$V_B = \frac{M V_{pk}^2}{2\pi(V_B + V_O)} \times \pi - 2\arcsin\left(\frac{V_B + V_O}{V_{pk}}\right) - \frac{2(V_B + V_O)}{V_{pk}^2}\sqrt{(V_{pk} + V_B + V_O)(V_{pk} - V_B - V_O)} \quad (11)$$

where M is the inductance ratio L_2 /L_1.

As observed from (11), the bus voltage V_B can be obtained easily by numerical method. It is noted that V_B is independent on the load, but dependent on the inductance ratio M. Fig. 4 depicts the relationship among V_B , rms value of the line voltage, and inductance ratio M. It is noted that the bus voltage is kept below 150 *V* at high-line input condition.

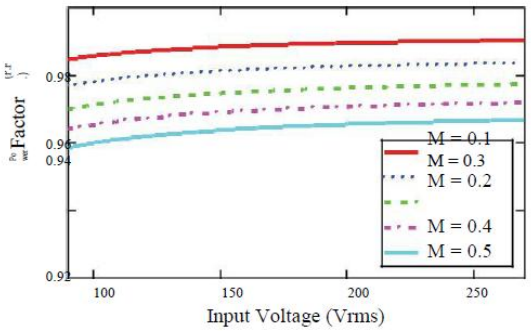

Fig. 5. Estimated Power Factor under variation of inductance ratios.

Similarly, the instantaneous and average input currents of the proposed circuit are

$$\langle i_{in} \rangle_{sw} = \frac{I_{L1pk}}{2} = \begin{cases} \frac{V_{in}(\theta) - V_T}{2L_1} d_1^2 T_s, & \alpha < \theta < \beta \\ 0, & \text{otherwise} \end{cases} \quad (12)$$

and

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$$I_{in} = \frac{1}{\pi}\int_{\alpha}^{\beta} \langle i_{in} \rangle_{SW}\, d\theta$$

$$= \frac{d_1^2 T_S}{2\pi L}\left[V_{pk} B - \gamma V_T\right]. \qquad (13)$$

Using (12) and (13), the rms value of the input current, average input power and power factor are given by

$$I_{in\,rms} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\beta} (\langle i_{in} \rangle_{SW})^2\, d\theta}$$

$$= \frac{d_1^2 T_S}{2\pi L_1}\sqrt{V_{pk}^2\left(\frac{\gamma}{2}+\frac{A}{4}\right) - 2V_{pk} V_T B + \gamma V_T^2}. \qquad (14)$$

$$P_{in} = \frac{1}{\pi}\int_{\alpha}^{\beta} v_{in}(\theta) \langle i_{in} \rangle_{SW}\, d\theta$$

$$= \frac{d_1^2 T_S V_{pk}}{2\pi L_1}\left[V_{pk}\left(\frac{\gamma}{2}+\frac{A}{4}\right) - V_T B\right] \qquad (15)$$

$$PF = \frac{\frac{1}{\pi}\int_{\alpha}^{\beta} v_{in}(\theta) \langle i_{in} \rangle_{SW}\, d\theta}{\frac{V_{pk}}{\sqrt{2}} I_{in\,rms}}$$

$$= \frac{\sqrt{2}}{\pi}\cdot\frac{V_{pk}\left(\frac{\gamma}{2}+\frac{A}{4}\right) - V_T B}{\sqrt{V_{pk}^2\left(\frac{\gamma}{2}+\frac{A}{4}\right) - 2V_{pk} V_T B + \gamma V_T^2}}. \qquad (16)$$

Fig. 5 exhibits the variation of power factor as a function of line input voltage and the inductance ratio M of the converter.

B. Condition for DCM

To ensure both cells working in DCM mode throughout the ac line period, we must determine their critical inductance first. To allow L_1 working in DCM and from (5), we have the following inequalities:

$$d_2 + d_3 \le 1 - d_{1\_PFC} \qquad (17)$$

and

$$d_{1\_PFC} \le \begin{cases} \dfrac{V_T}{v_{in}(\theta)}, & \alpha < \theta < \beta \\ 0, & \text{otherwise} \end{cases} \qquad (18)$$

where d_1 PFC is the maximum d_1 of the PFC cell. For the buck–boost dc/dc cell working in DCM mode, the following inequality must be held:

$$d_2 \le 1 - d_{1\_DC/DC} \qquad (19)$$

From (6) and (19), the maximum d_1 of the dc/dc cell is

$$d_{1\_DC/DC} \le \frac{V_O}{V_O + V_B} = \frac{V_O}{V_T}. \qquad (20)$$

Due to sharing switch in both cells of the converter, the maximum duty cycle $d_{1\text{-}max}$ of the proposed converter is

$$d_{1\_max} = \begin{cases} \min(d_{1\_PFC}, d_{1\_DC/DC}), & \alpha < \theta < \beta \\ d_{1\_DC/DC}, & \text{otherwise.} \end{cases} \qquad (21)$$

By applying input–output power balance of the PFC cell and substituting (21) into (15), the critical inductance $L_{1\,crit}$ is given by

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$$L_{1\_\min} = \frac{R_{L\_\min}}{V_{pk}^2} + \frac{}{}$$

$$+ V_T(\cos(\beta) - \cos(\alpha))\ d_1^2{}_{-\max} \qquad (22)$$

where RL min is denoted as the minimum load resistance of the converter.

For the dc/dc cell sustaining all the power to the load under the smallest. Under the input–output power balance of the dc/dc cell, the critical inductance $L2$ crit can be determined. The input power of the dc/dc cell in Mode A is given by

$$P_{in-DC/DC} = \frac{V_B}{\pi} \int_0^{\pi} \langle i_{DC/DC} \rangle_{SW}\, d\theta = \frac{V_B T_s}{2L_2} d_1 \qquad (23)$$

where < id c / d c >s w is the instantaneous input current of dc/dc cell.

Hence, by substituting (21) into (23), the critical inductance $L_{2\text{-crit}}$ is given by

$$L_{2\_crit} = \frac{R_{L\_\min} V_B^2 T_s}{2V_O^2} d_{1-\max}^2 \qquad (24)$$

C. Components Stresses

Before embarking on calculating stresses on the devices, there are two characteristics of the circuit to be clarified. Interestingly, the current passing through the diode $D2$ is the difference of current between iL 2 and iL 1 at the time interval $d1$ Ts . Both inductor currents flows into the diode at the interval, but in op-posite direction. In addition, unlike the boost-type single-stage ac/dc converter, the current of the switch $S1$ is iL 2 , but not the

TABLE I
VOLTAGE STRESSES ON THE SEMICONDUCTOR DEVICES

Semiconductor devices	Peak Voltage
Diode D_1	V_{pk}
Diode D_2	V_{pk}
Diode D_3	V_T
Switch S_1	$V_{pk} + V_T$

superposition current of both inductors. Thus, the simultaneous currents of the diode D_2 and switch S_1 at interval d_1 T_s are

$$i_{D_2} = i_{L2} - i_{L1} \qquad (25)$$

$$I_{S_1} = i_{L2}. \qquad (26)$$

The rms current stresses on the diodes and switch are deter-mined by averaging their rms current in a switching cycle over a half-line period. The rms current stress on the diode D_1 over a switching cycle is

$$I_{D1,sw\ rms} = \frac{T_s}{L_1}\sqrt{\frac{d_1^3 (v_{in}(\theta) - 2V_T)^3}{3V_T}}. \qquad (27)$$

$$I_{D_1,hf\,rms} = \frac{T_s}{\pi} d_1^3 \gamma V_T (8V_T^2 + 3V_{pk}^2) + 3V_{pk} B \frac{V_{pk}^2}{} + 4V_T^2 \frac{3V_T V_{pk}^2 A}{} \frac{V_{pk}^3 C}{} \qquad (28)$$

Then, by taking the average of (27) over a half-line period, its rms current stress is obtained as (28), shown at the bottom of the page, where $C = \cos(3\alpha) - \cos(3\beta)$.

Similarly, the current stresses on the other semiconductor devices can be calculated easily as

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$$I_{D_2,\text{hf rms}} = \frac{}{} [2\alpha V_B^2 + E] \qquad (29)$$

$$I_{D_3,\text{hf rms}} = \frac{V_B T_s}{L_2} \sqrt{\frac{3\pi}{d_1^3 (V_B - V_o)^3}} \qquad (30)$$

$$I_{S_1,\text{hf rms}} = \frac{V_B T_s}{L_2} \frac{d_1^3}{3} \qquad (31)$$

where

$$E = \frac{1}{L^2} \gamma (V_B L_T + L_2 V_o)^2$$

$$\frac{1}{A} - 2L_2 V_{pk} B (V_B (L_1 + L_2) + L_2 V_o) + \frac{L^2 V^2}{\gamma + 2}.$$

In addition, the voltage stresses on the semiconductor devices are stated in Table I.

D. Capacitors Optimization

To determine the size of the intermediate bus capacitor C_B, we can consider the hold-up time ($t_{hold up}$) of the circuit.

The bus capacitor C will sustain all the output power within when the ac$B$input source is removed. In normal prac- *th old u p* tice, the hold-up time is one of the ac line cycle. In addition, the maximum capacitance of CB to meet this hold-up time re-quirement is determined under the low-line and full output load conditions. Thus, the size of CB is expressed as follows:

$$C_B = \frac{2P_o t_{hold up}}{(V_B @ 90V_{rms})^2}. \qquad (32)$$

Apart from the size of C_B , it is noted that the line frequency ripple on the output capacitor C_o is inevitable since a portion of the input power is coupled to the load directly. However, this ripple can be reduced by increasing its capacitance.

E. Distribution of Direct Power Transfer

The interaction of power processing between both PFC and dc/dc cells under low and high-line conditions is described as

$$p_o(\theta) = p_{o\,\text{PFC}}(\theta) + p_{o\,\text{DC/DC}}(\theta) \qquad (33)$$

where po (θ), po PFC(θ), and po DC/DC(θ) are denoted as in- stantaneous output power of the converter, output power of PFC cell and output power of dc/dc cell, respectively. Both instantaneous output powers of PFC and dc/dc cells can be calculated as

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$$p_{o\,PFC}(\theta) = v_{o\,i_{L1}}(\theta)_{sw} = \begin{cases} \frac{(d_1(\theta))^2 V_o I_s}{2} v_{in}(\theta)(v_{in}(\theta) - V_T), & \alpha < \theta < \beta \\ 0, & \text{otherwise} \end{cases} \quad (34)$$

$$p_{o\,DC/DC}(\theta) = p_{in\,DC/DC}(\theta) = V_{B\,DC/DC} < I_{sw} > = \frac{V_B^2 T_s}{2L_2} (d_1(\theta))^2 \quad (35)$$

where $p_{in\,dc/dc}(\theta)$ and $d_1(\theta)$ are defined as the instantaneous value of input power of the dc/dc cell and duty cycle d*1* .

cial role in this analysis. $d1(\theta)$ can be obtained easily once the average output current of the converter is determined. By concycle, the average output current of the converter is given by

$$I_o = \begin{cases} i_{L1}(\theta)_{sw} + i_{d3}(\theta)_{sw}, & d3_{sw} \text{ otherwise} \\ \frac{(d_1(\theta))^2 T_s}{2} v_{in}(\theta)(v_{in}(\theta) - V_T) + \frac{V_B^2}{L_1 V_T}, & \alpha < \theta < \beta \\ \frac{(d_1(\theta))^2 T_s}{2} \frac{V_B^2}{L_2 V_o}, & \text{otherwise.} \end{cases} \quad (36)$$

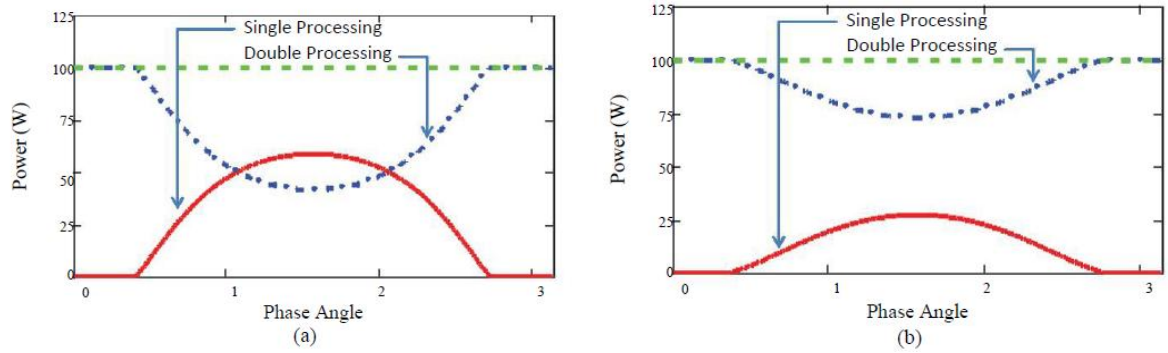

Fig. 6. Calculated power processing by PFC cell (red trace) and dc/dc cell (blue trace). Condition: P_o = 100 *W* (green trace), V_o = 19 *V* and *M* = 0.4.

Hence, $d1(\theta)$ in a half-line period is expressed as

$$d_1(\theta) = \begin{cases} \frac{2P_o}{v_{in}(\theta)(v_{in}(\theta) - V_T) - \frac{V_o}{L_1 V_T}}, & \alpha < \theta < \beta \\ \frac{2L_2 P_o}{V_B^2 T_s}, & \text{otherwise.} \end{cases} \quad (37)$$

By substituting (37) into (34) and (35), the simultaneous output power of the converter and power distribution of the PFC and dc/dc cells are plotted as in Fig. 6. The traces of single and double power processing represent the

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power proceed by PFC cell *po* PFC$^{(\theta)}$ and dc/dc cell po dc/dc$^{(\theta)}$, respectively. Besides, the green dash trace is the output power (*po* total*(θ))* of the converter. It is noted that the power handled by both cells is changed oppositely to maintain the load power under different input voltages. At low-line condition, there is more input power coupled to the output directly. In contrast, more power is deliv-ered to the output by the dc/dc cell at high-line condition. More discussion of the direct power transfer is given in Section V.

IV. EXPERIMENTAL RESULTS

The performance of the proposed circuit is verified by the prototype. To ensure the converter working properly with con-stant output voltage, a simple voltage mode control is employed. To achieve high performance of the converter for universal line operation in terms of low bus voltage (< 150V) and high power factor (> 96%), the inductance ratio has to be optimized ac-cording to Figs. 4 and 5. The lower the bus voltage of the con-verter, the lower voltage rating capacitor (150 V) can be used.

TABLE II
CIRCUIT COMPONENTS

Parameters	Values
IC Controller	TL594
Input filter inductor L_f	2 mH
Input filter capacitor C_f	2 ∝F
Inductor L_1	106 ∝H
Inductor L_2	46 ∝H
Inductance Ratio (M = L_2/L_1)	0.434
MOSFET S_1	SPW47N60CFD
D_1	MUR3040PT
D_2	MUR3040PT
D_3	MUR3040PT
C_B	5 mF
C_o	5 mF

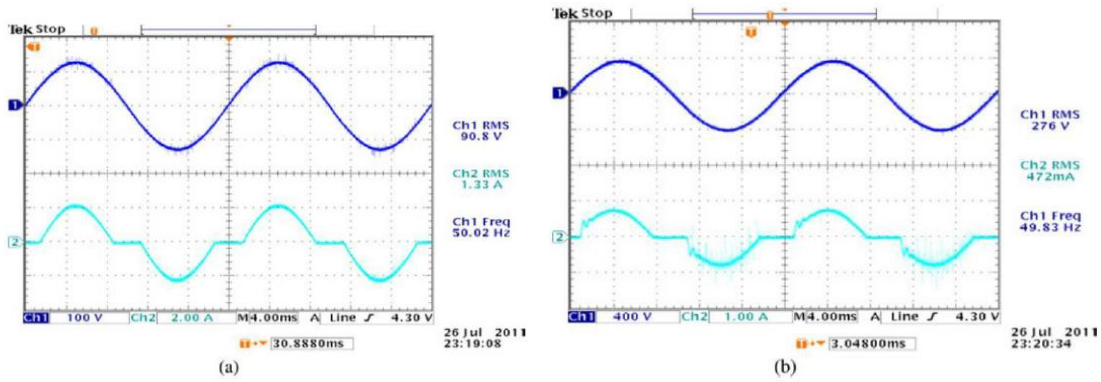

Fig. 7. Measured input characteristic of the converter at (a) 90 Vr m s and (b) 270 Vr m s under 100-W condition

In addition, the inductance ratio will affect the efficiency of the converter. More detail will be given in Section V. Taking the performance of the converter on bus voltage, power factor, and efficiency into account, the inductance ratio around M = 0.4 is selected. Table II depicts all the components used in the circuit, and its specification is stated as follows:

1) output power: 100 W;

2) output voltage: 19 Vd c ;

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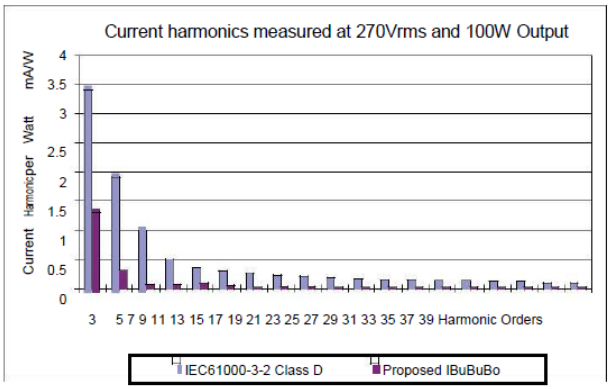

Fig. 8. Comparison of IEC61000-3-2 Class D standard with measured input current harmonics at 270 Vr m s .

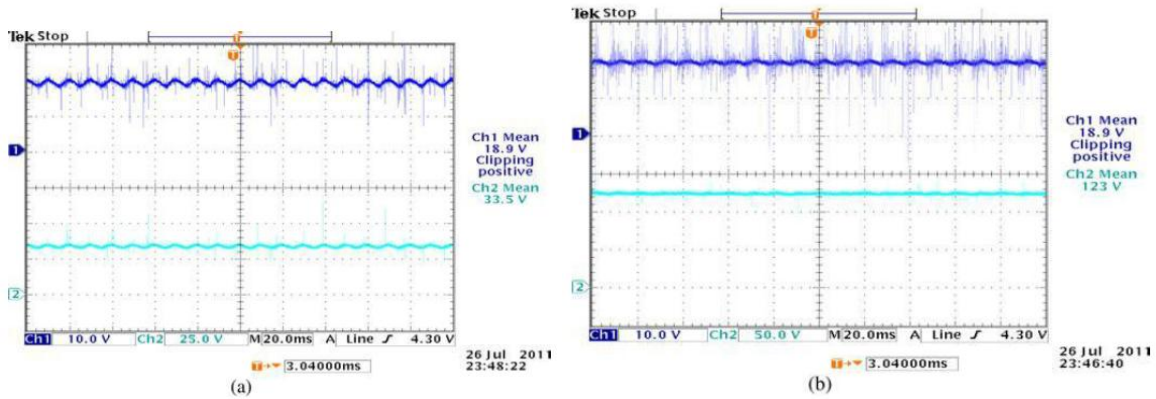

Fig. 9. Measured output voltage (upper trace −10 V/div) and intermediate bus voltage (bottom trace −40 V/div) at (a) 90 Vr m s and (b) 270 Vr m s under full load condition.

3) power factor: > 96%;

4) intermediate bus voltage: < 150V;

5) line input voltage: 90–270 Vrm s /50 Hz;

6) switching frequency (*fs*): 20 kHz.

Fig. 7 shows the waveforms of the line-input voltage along with its current under full load condition at 90 Vrm s and 270 Vrm s , respectively. The measured current harmonics met the IEC61000-3-2 class D standard as shown in Fig. 8. In ad-dition, the measured output and bus voltages under both low and high line conditions are shown as in Fig. 9. It can be seen that the bus voltage was kept at 123 V and well below 150 V at high-line condition. Fig. 10 illustrates the conversion efficiency of the proposed converter under different line input and out-put power conditions. The maximum efficiency of the circuit is around 89% at low line application. Furthermore, Fig. 11 shows the predicted intermediate bus voltage is in good agreement with the measured value.

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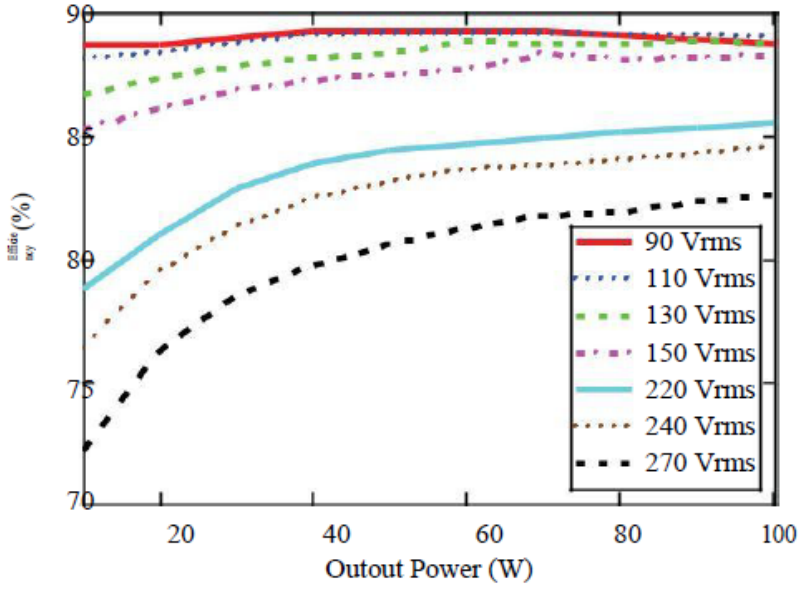

Fig. 10. Measured circuit efficiency under load variation.

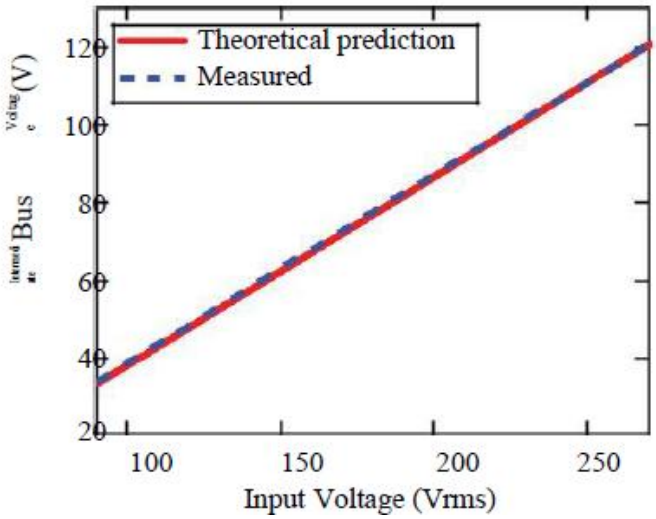

Fig. 11. Comparison of measured intermediate bus voltage with its predicted value.

V. DISCUSSION

According to [13] and [21], the direct power transfer ratio

n under this type of capacitive coupling is Vo/VT. It can be seen that the portion of direct power transfer from input to output decreases when VB becomes larger resulting in increase of VT. In other words, the direct power transfer decreases when the line input voltage increases. It matches with the discussion in Section III-E. In addition, the increase of VB will lower the conversion efficiency of dc/dc cell due to larger voltage conversion around ten times at high-line condition, from VB = 123 V down to Vo = 19 V. As a result, it further impairs the efficiency of the converter at high-line operation. On the other hand, from (2), decrease of VB extends the conduction angle of the converter leading to higher power factor. However, lower VB requires decrease of inductance ratio resulting in higher peak inductor currents and causing higher conduction loss. Thus, tradeoff has to be made for selecting the inductance ratio

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among the peak current of both inductors, bus voltage, and power factor. Nevertheless, the converter is capable to be used under high-line condition with the full load efficiency around 84% at 240 Vrm s .

TABLE III
COMPARISON OF RECENTLY REPORTED TOPOLOGIES

	Diode	Control Switch	Magnetic Components	Capacitors	Intermediate Bus Voltage V_B	Input Voltage V_{rms}	Output Condition	Maximum Efficiency
[13]	3	1	2 Ind.	2	≤ 400 V	90 ~ 270 Vrms	100 V/100 W	89.5%
[15]	4	1	1 Ind. and 1 Trans.	2	≤ 220 V	90 ~ 270 Vrms	48 V/100 W	82%
[9]	2	2	1 Ind. and 1 Trans.	2	≤ 36 V	187 ~ 265 Vrms	56 V/100 W	85.5%
[10]	4	1	2 Ind.	2	≤ 86 V	110 Vrms	-20 V/50 W	77%
[17]	3	2	3 Ind.	2	≤ 209 V	85 ~ 265 Vrms	-48 V/111.52 W	83.1%
[18]	6	1	3 Ind.	3	V_{B1} = 70 V V_{B2} = 30 V	85 Vrms	-5 V/20 W	80.5%
[19]	2	1	2 Ind.	2	N/A	90 ~ 240 Vrms	19 V/13.72 W	90.56%
Proposed	3	1	2 Ind.	2	≤ 130 V	90 ~ 270 Vrms	19 V/100 W	88.9%

Here Ind. and Trans. are denoted as number of inductors and number of transformers.

To continue with the comparison from Section I, Table III shows the performances of recent topologies and the proposed converter in more detail. In order to achieve low output voltage and low intermediate bus voltage with high efficiency for univer-sal line operation, the topologies employ different approaches. Furthermore, every converter has their best performance when working at particular input and output conditions. Although the input and output conditions for the converters in the table are not the same, we have two criteria to compare their performances. First, for a given power level, the lower the output voltage of the converter, the lower the efficiency it gets due to more current flowing in the circuit. Second, for PWM converters, the fewer semiconductor devices used in the converter, the lesser the con-duction and switching loss of the converter will be. However, the operational parameters, selection of switching frequency, and semiconductor will also impact on the circuit efficiency. Therefore, it is hard to have a fair efficiency comparison and, hence, circuit efficiencies shown are just for the information pur-pose. Nevertheless, apart from the efficiency, the performances on reducing the bus voltage, the step-down ratio and circuit complexity are less dependent on the input and output condi-tions, and operational parameters, but the topology itself and the inductance ratio. From the table and excluding all the isolated converters, it can be seen that the proposed converter is able to achieve the lowest bus voltage at high-line condition with low output voltage and probably higher efficiency among all trans-formerless topologies and its structure is simpler. In addition, comparing with [10], [18] at low-line condition, the proposed converter is also able to achieve the lowest bus voltage at around 33.5 V with positive output voltage and probably higher effi-ciency. Thus, the proposed converter has better performance for lower output voltage operation.

VI. CONCLUSION

The proposed IBuBuBo single-stage ac/dc converter has been experimentally verified, and the results have shown good agree-ments with the predicted values. The intermediate bus voltage of the circuit is able to keep below 150 V at all input and output con-ditions, and is lower than that of the most reported converters. Thus, the lower voltage rating of capacitor can be used. More-over, the topology is able to obtain low output voltage without high step-down transformer. Owing to the absence of trans-former, the demagnetizing circuit, the associated circuit dealing with leakage inductance, and the cost of the proposed circuit are reduced compared with the isolated counterparts. In addition, the proposed converter can meet IEC 61000-3-2 standard, and provide both input surge current and output short-circuit protec-tion. Thanks to the direct power transfer path in the proposed converter, it is able to achieve high efficiency around 89%.

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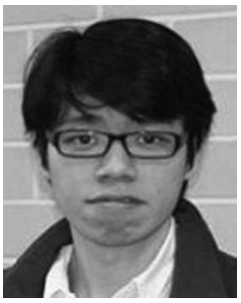

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