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A NEW HYBRID ACTIVE NEUTRAL POINT CLAMPED FLYING CAPACITOR MULTILEVEL INVERTER FED INDUCTION MOTOR

Sonam Gehlot[1], J.S. Shakya[2]

[1,2]*Electrical Engineering, Samrat Ashok Technological Institute, (India)*

ABSTRACT

The paper proposes a new five-level hybrid Topology combination feature of natural point clamped and flying capacitor inverters. The future topology provides good loss distribution; avoid direct series connection of semiconductor devices. The five level Flying capacitor(FC) based on active neutral point clamped (ANPC) Inverter .The voltage across the FC's and dc link capacitors be simultaneously controlled at their reference Voltage levels. NPC and FC inverters are the Most widely used topology of multilevel inverters In high power application. This paper present Basic operation and most used modulation and Control techniques developed to date. The discuses the main field of application and presents some technological Problems such as capacitor balance and losses. The features of this topology are investigated and Compared to other available topology and implement the induction motor of this paper.

Keywords: Multilevel Inverter, Flying Capacitor, Active Neutral Point Clamped Modulation Techniques.

I. INTRODUCTION

Over the past three decades, multilevel inverter have made revolutionary change in utilization of power electronics in medium to high voltage and high power application multilevel inverter provide significant advantages over the typical 5 level inverter, including but not limited to lower harmonic distortion. For medium voltage inverter, cascade H Bridge (CHB), neutral point clamped (NPC) and flying capacitor (FC) are the primary topology. Among them NPC & FC to control the voltage across the dc link which reefed in this paper has 5level FC based ANPC inverter.

FC inverter uses capacitor to generate output voltage level. Instead of using clamping diode it use capacitor to hold voltage to the desired value. The topology can provide both capacitor voltage comparison and power loss distribution among switches. They are connected to the mid-point of two valve pairs on same position on each side of the midpoint between the valves. Flying capacitor at higher levels that increase the initially cost and maintenance charge and decreases the reliability of the inverter along with capacitor pre charge in same application.

NPC inverter use diodes to clamp voltage level generated at the dc link capacitor to o/p voltage. It was a first widely popular NPC multilevel topology. It is use in the industrial application. No. Of diodes, unbalanced

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operation of dc link voltage divider capacitor, and distribution of loss among switches are major problem of this topology. Active NPC (ANPC) improves the loss distribution NPC by replacing diode with active switches.Providing alternative neutral point path. [9]

Hybrid topologies are possible solutions where higher number of levels is required. Combining the advantages of CHB, FC, and NPC, hybrid inverters can give loss and voltage balancing while keeping the number of components low. Examples of hybrid topologies combine FC and NPC can be found in [10]–[12], some of which has already creates industrial applications. The 5-level Flying Capacitor active neutral point capacitor is an example of hybrid topologies that complete its way to the industry. The ACS2000. family of medium voltage drives, commercialized by ABB, uses this topology with both active and passive features end configurations. The most important advantage of this topology is the use of a single flying capacitor to create the output five levels. compare to other topologies that provide a common dc-link, FC-ANPC has provided a suitable trade off between the cost, performance, and reliability for 5-level applications. The disadvantages of FC-ANPC is high number of switches, series connection of high voltage switches, and poor loss distribution [13].

This paper projected a new five-level hybrid topology base on FC and ANPC inverter. The target of the proposed topology is to defeat the shortcoming of the traditional FC-ANPC. Thus, comparatively, the proposed topology provides better loss distribution, avoids direct series connection of high voltage switches, and eliminates 2 switches per phase leg. These advantages come at the charge of an additional capacitor and 6 diodes. Never the less, the lifetime of each capacitor is expected to delay due to the half cycle operation and lower rms current..

In this paper, the configuration and operation associated carrier-based and non carrier- f the proposed topology is described in section II. In section III, based modulation techniques are presented and modified to suit to the proposed topology. IV implements the induction motor for FC and ANPC inverter. In section V, the simulation result of a case study is presented to verify the operation of the proposed topology for medium voltage application.

II. THE PROPOSED TOPOLOGY AND OPRETION

The proposed to topology include dc-link that is between the three phases. The DC-link provide 3-voltage levels +2E, 0, -2E for the phase legs. Since all the phases have the similar configuration, only one phase leg of this topology has been shown in fig.1. The entire component shown in the fig. Have been shown in fig have equal operating voltage E i.e. one fourth of the dc-link voltage Vac. The Fc capacitor CA1 and CA2 are controlled to stay charged at the target voltage E..

The presented states of singal phase leg are shown in table I. To generate level 2E, all the top arm switches SA1, SA2, SA3, and SA4 have to turn on. For level E, two choices are available i.e. either through the dc-link positive point (EP) or through dc-link's neutral point (E0). This redundancy can be used to the balance voltage of CA1. Level 0 is generated through clamping the dc-link's neutral point to the output v/g (00). Negative states can be generated similarly due to the symmetric of the topology.

The operation of this topology is similar to topologies such as stacked multicell (SMC) converter [11], [12], [7], where the positive or negative stacked operate separately. Hence, the positive stacked capacitor CA1 is used and balanced through the positive cycle and rest during the negative cycle, where as the negative stack capacitor

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CA2 is used and balanced for the duration of the negative cycle and rest during the positive cycle. So, the flying capacitors will see switching frequency rather than line frequency and therefore the capacitor extent is not too large. Similar to the 3-level NPC inverter, if the three phases of the load are balanced, the neutral point voltage will be constant inside theory. However, the voltage might slightly drift away due to the imbalance in the elements' leakage current. In addition, all though small, there is always a little imbalance among the phases. A constant voltage drift, level though small, can cause higher voltage across part of the devices which can be lethal. Nevertheless, this drift can be rewarded by injecting a small common mode to the three phases.

An important feature of this topology is the even distribution of transitions among switching devices. Therefore, switching loss which is the major limiting factor of inverter's thermal performance is distributed among the switches. As the main result, the trade off between switching frequency and current date is improved. This provides the opportunity to either increase the rated current and power of the inverter is increase the switching frequency resulting in lower capacitor size and improved voltage wave form quality.

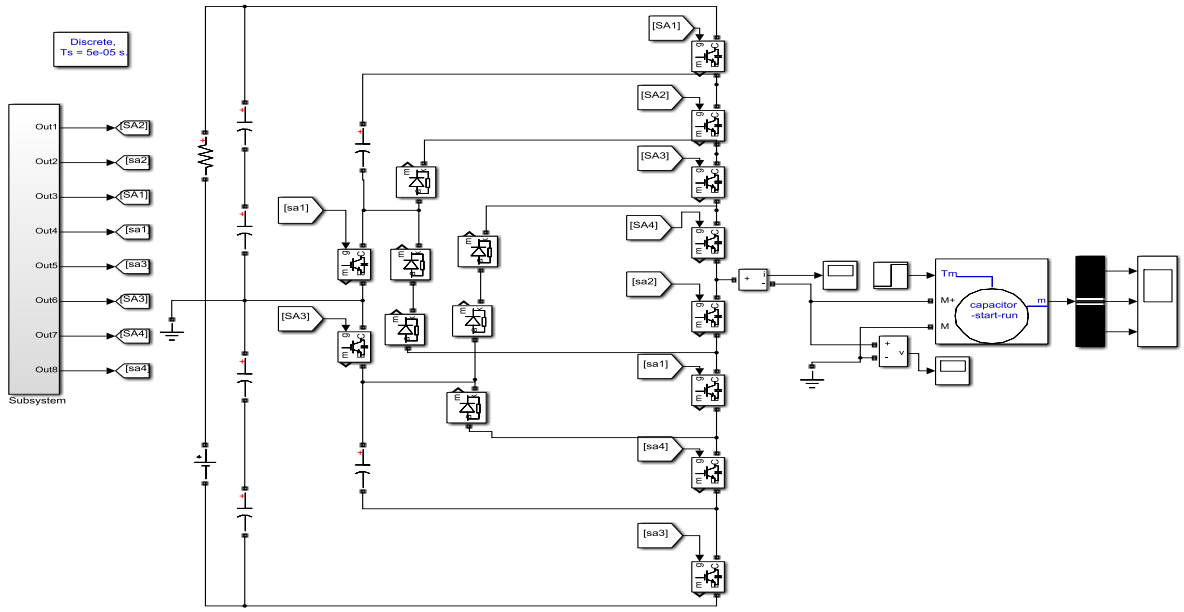

Fig 1.A phase leg of the proposed 5-level hybrid topology.

TABLE I switching states of the proposed inverter

Level	State	S1 S2 S3 S4	C1 C2
+2E	+2E	1 1 1 1	N.A. N.A.
+E	+EP	1 0 1 1	i>0charge N.A. i<0 Discharge
	+E0	0 1 1 1	i>0Discharge N.A.

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						i<0 charge	
0	0	0	0	1	1	N.A.	N.A.
-E	-E0	0	0	1	0	N.A.	i>0 charge i<0 Discharge
	-EN	0	0	0	1	N.A.	i>0 Discharge i<0 charge
-2E	-2E	0	0	0	0	N.A.	N.A.

S'1, S'2, S'3, S'4 are switched complementary to S1, S2, S3, S4, respectively i>0 represents outbound current and i<0 represents inbound current .N.A. stands for not affected.

III. MODULATION TECHNIQUES

A choice of modulation techniques may be adapted for the proposed topology. Carrier-based modulation with sinusoidal and modified reference as well as non-carrier-based techniques such as space vector modulation and selectively harmonic elimination may be used to generate the gate signals. The choice of a modulation technique is mostly a trade off among the requirements of the application, complexity of the software, and cost of the control hardware.

3.1Carrier-Based Modulation

This paper used only carrier-based modulation, non carrier-based modulation are not used Carrier set's arrangement and reference waveform's shape are the main sources of varieties in carrier-based modulation techniques for multilevel inverters. As for carrier set's arrangement, level shifted carriers LSC and phase shifted carriers PSC are the two main category that are respectively suitable for diode-clamped and multi-cell structure. Two members in this LSC family, alternative phase opposition disposition APOD and phase disposition PD are known to generate the best results for single phase and three phase application, respectively.

Multilevel Carrier - Based PWM :- Multilevel carrier-based PWM uses several triangular carrier signals, which can be modified in phase and/or straight down position in order to reduce the output voltage harmonic content. There are two common carrier modifications applied to these multilevel inverter phase-shifted PWM is widely used in NPC inverters and can also be used in cascaded inverters. In [46], it is shown that this modulation technique is applied to a five-level inverter. This modulation technique produces even distribution of power among cells, such as that in Fig. , which produces a high harmonic content in the input current. In this drawback is avoid using rotating carrier, which balances the power of each cell. In [12], the phase-shifted modulation is used in each NPC inverter and synchronized with the other cells to produce the multilevel output voltage. This modulation shifts the phase of each carrier in a proper angle to reduce the harmonic satisfied the output voltage, as shown in fig2. Moreover, it is possible to work in the over modulation region when a common-mode term is added to the reference wave . This flexibility has been used to serve different purpose such as increase dc-link's utilization, or lower THD, lower loss, and neutral point voltage control. For the proposed inverter, a hybrid modulation technique is need due to the hybrid structure of the topology. Figure 2 illustrates the modulation technique for single-phase case. It is intuitive to separate the operation to positive and negative cycles, since the

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each cycle is generated with a 3-level FC stack. The gate signals for each FC is then generated using PSC to present natural voltage balancing for the flying capacitors. The generated output PWM wave for matches the APOD scheme.

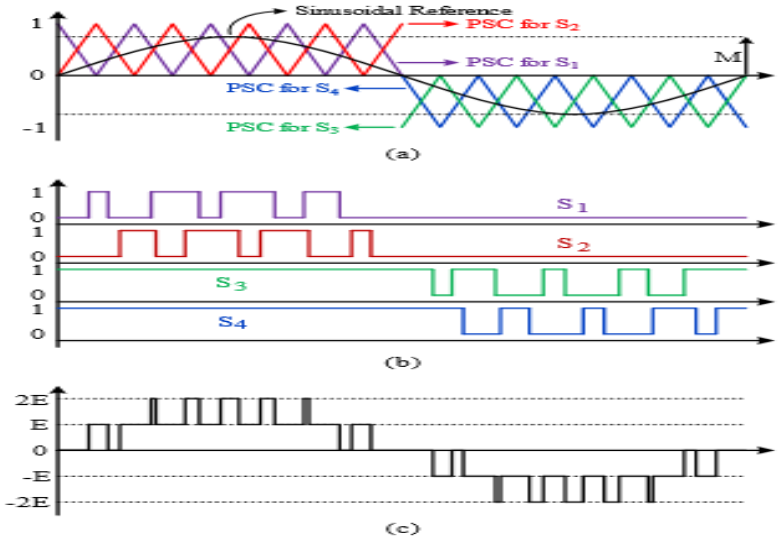

Fig 2 carrier-based modulation using PSC with sinusoidal reference for single phase application.(a) reference and carrier arrangement.(b) gate signal . (c) output waveform.

It is important procedure is independent of the adopted modulation technique. Therefore, it can be used the carrier-based modulation techniques as well as non-carrier-based. This might be there a good alternative when the complexity of the carrier-based technique is relatively high e.g. for PD scheme.

IV. IMPLEMENTS THE INDUCTION MOTOR FOR FC AND ANPC INVERTER

The single phase induction motor is the work mare of modern industry shown on fig 1. Single phase induction motor of wound rotor type is commonly used in adjustable speed drives. According to the type of winding on rotor, there are two common types of induction machines namely squirrel cage induction motor and wound-rotor induction motor. Squirrel-cage induction are mostly used in industrial drives which have cylindrical rotor with short-circuited rotor with short-circuited rotor windings with the voltage supplied to stator winding thus rotor does not have a brushes and commentator but consists of conducting bars that are placed into the rotor slots. These bars are short circuited by the shorting rings .Whereas wound rotor induction motor have connected rotor winding. In addition to the voltages that are applied to the stator windings the phase voltage can be supplied to the rotor winding using brushes and slip ring. However, wound-rotor induction motor has not been widely used because their efficiency and maximum angular velocity are lower compared to squirrel-cage. On the other hand, squirrel-cage, motor have been tremendously used in high performance electric drives and electromechanical systems [7]

V. SIMULATION RESULTS

To verify the operation of the proposed topology and the performance of the modulation techniques provided in section III, using MATLAB. The technique is used to improve the level of the inverter to extend the design

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flexibility and reduces the harmonics. The performance of the natural balancing technique for single-phase 4kV inverter supply, carrier frequency 500Hz. the dc-link voltage is set at 400V and flying capacitor are 10µF.

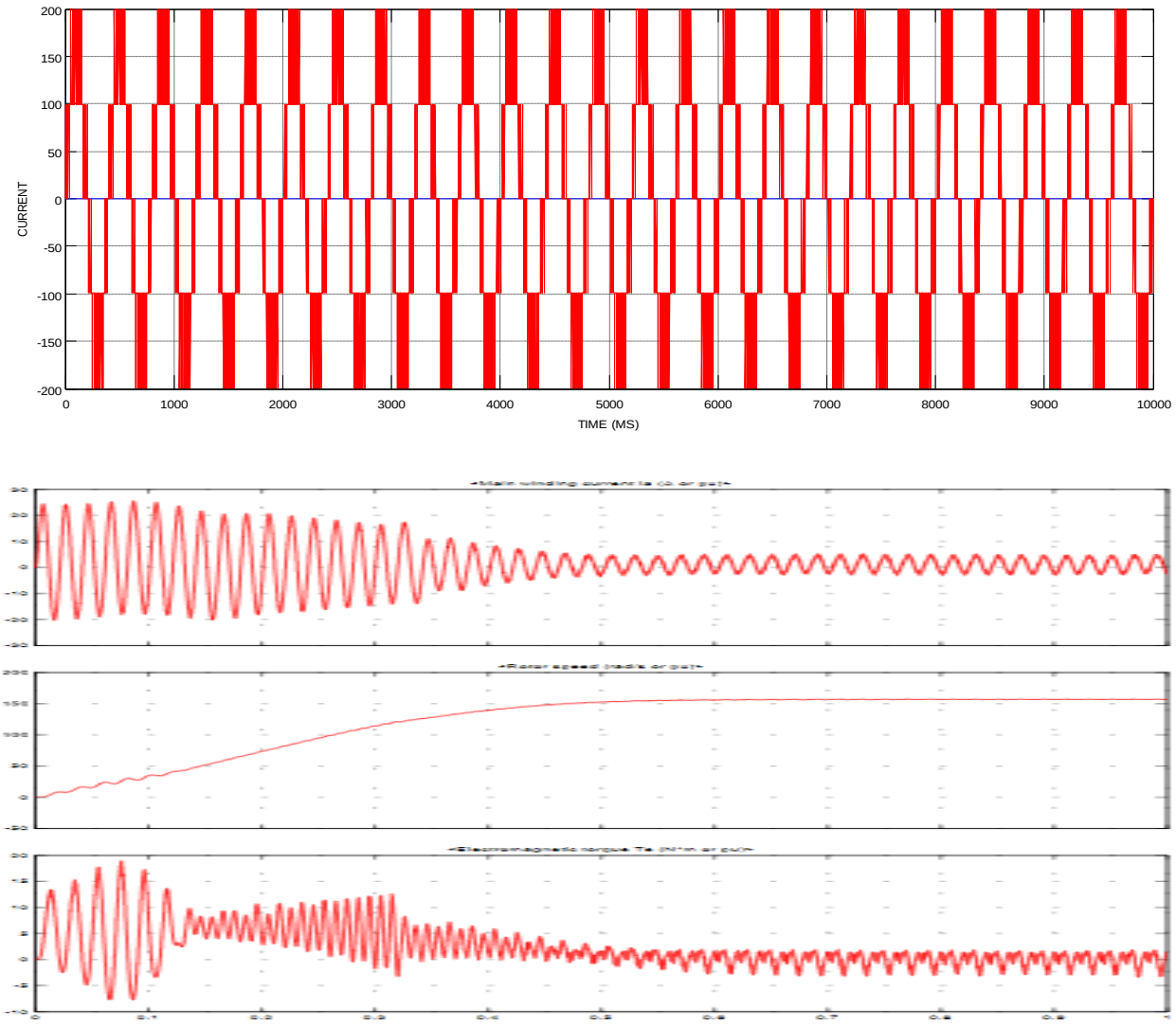

Fig 4. Simulation results (a) phase voltage (b) induction motor voltage

V. CONCLUSION

A new hybrid five-level inverter topology and modulation technique is future. this new topology requires two less switches at the charge of an additional capacitor and six diodes. However, since the capacitors still see the switching frequency and their range remain the same, it is expected to reduce the inverter's total cost. Also, unlike 5-level ANPC, all switches must hold up the same voltage which eliminates the need for series connection of switches and associated synchronized turn on and off problem. Good loss distribution between switches can increase the inverters rated power or provide higher switch frequency and smaller capacitor size. The simulation of multilevel inverter is carried out in MATLAB/ Simulation, to identify the suitable level inverter which has comparatively less total harmonic distortion in its output. A relative study is done for better

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configuration of multilevel inverter. The simulation results are existing and analyzed. From this part of work, the sinusoidal PWM based simulation give better results. Hence, it is taken for further studies in the proposed inverter.

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