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ANALYTICAL MODELING AND CHARACTERIZATION OF CYLINDRICAL GATE ALL AROUND MOSFET

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ABSTRACT

In this paper, an analytical study of the threshold voltage with respect to various physical parameters of cylindrical Gate All Around MOSFET has been found solving two dimensional Poisson equation. This paper claims calculation of threshold voltage using centre potential and calculation of the effect of device parameters on threshold voltage.

Keywords: Cylindrical Gate All Around, Threshold Voltage, Short Channel Effect

I INTRODUCTION

In recent years, CMOS has encountered its limitations due to scaling of device size to improve circuit performance. Moore era has seen evolution of most promising solution as well as most improved piece of nanoscale technology called Gate All Around nanowire MOS that has attracted great attention instead of planar structure MOS by researcher due to efficient control on channel. We have considered cylindrical one in our research as it is better than rectangular because of reduction of the fringing(corner) effect. This device has also also helped in achieving higher packing density due to shorter dimensions and higher drive current. In this paper along with the introduction we come across detailed knowledge of CGAA thereby following it with analysis of physics of CGAA model followed by simulated result.

II DEVICE STRUCTURE

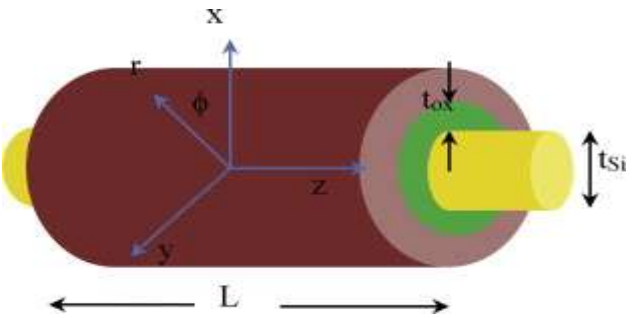

Fig. 1 Structure of Cylindrical Gate All Around MOSFET

We have introduced the 30nm Gate All Around MOSFET for analysis and after depth study of multigate devices finally found the results using 2D simulation for the device with change in threshold voltage with various oxide thickness, silicon thickness and drain to source voltage to explore short channel effects. In the device above radial direction is assumed along the radius and lateral directions are assumed along z axis of the figure. It has uniform doping concentration of drain-source keeping channel doping less. The value of silicon film thickness is taken twice the radius of the cylinder (diameter of cylinder). All the structure junctions are taken as abrupt and biasing condition at room temperature. This device is the one in which gate oxide is wrapped around channel region and above it gate electrodes with excellent transconductance and short channel behaviour are embedded. Mobility factor played an important role in the simulation of the model. In this inversion layer formation effect on threshold voltage and impact ionization effects are ignored.

Table 1: Parameters used for the simulation

Parameter Symbol	Parameter	Value
N_a	Impurity concentration doped in the channel	$10^{16}cm^{-3}$
N_d	Impurity concentration doped in the source and drain	$10^{20}cm^{-3}$
t_{si}	Thickness of silicon film	10nm
t_{ox}	Oxide thickness	2nm
L	Channel length	30nm
ε_0	Vacuum Permittivity	$8.8*10^{-12}F/m$
ε_{si}	Silicon Permittivity	$11.85*\varepsilon_0$
ε_{ox}	Oxide Permittivity	$3.9*\varepsilon_0$
K	Boltzmann constant	$1.38*10^{-23}J/K$
T	Absolute temperature in Kelvin	300K
χ_{si}	Silicon Susceptibility	20.75
ϕ_m	Work Function of metal	$4.6*1.6*10^{-19}V$

III CALCULATIONS

The potential distribution in the channel region $\phi(r,z)$ and is obtained by solving the Poisson equation in a cylindrical coordinate system:

$$\frac{1}{r}\frac{\partial}{\partial}\left(r\frac{\partial}{\partial r}(\phi(r,z))\right)+\frac{\partial}{\partial z}(\phi(r,z))=\frac{qNa}{\epsilon_{Si}}$$

The built-in potential between the source/drain and Si channel junction and is given by:

$$V_{bi}=\frac{KT}{q}\ln\left(\frac{N_aN_d}{n^2{}_i}\right)$$

The flat band voltage of the MOSFET is :

$$V_{fb} = \phi_m - \phi_s$$

$$\phi_s = \frac{\chi_{Si}}{q} + \frac{E_{g,Si}}{2q} + \frac{KT}{q}\ln\left(\frac{N_a}{n_i}\right)$$

Considering channel Length (L) very large, we get the following threshold voltage equation and substituting the value of flatband voltage we get:

$$V_{th-L} = \phi_{smin-th} + V_{fb} + \frac{\lambda q N_a}{4\epsilon_{si}}\left(1 - \frac{t^2_{si}}{\lambda}\right)$$

If the equation is replaced by equation of A and B and $V_{gs}$by V_{th}

$$V_{th} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

Where a,b and c are constants and their values are calculated below:-

$$a = 1 - N_2 N_4 N_5$$

$$b = N_1 N_4 N_5 + N_2 N_3 N_5 - 2V_{th-L}$$

$$c = V^2_{th-L} - N_2 N_4 N_5$$

$$N_1 = \frac{\left[\left(V_{bi} + V_{fb} + \frac{\lambda q N_a}{4\epsilon_{si}}\right)\left(1 - e^{\left(-\sqrt{\frac{4}{\lambda}}L\right)}\right) + V_{ds}\right]}{e^{\left(\sqrt{\frac{4}{\lambda}}L\right)} - e^{\left(-\sqrt{\frac{4}{\lambda}}L\right)}}$$

$$N_2 = \left[\frac{\left(1 - e^{\left(-\sqrt{\frac{4}{\lambda}}L\right)}\right)}{e^{\left(\sqrt{\frac{4}{\lambda}}L\right)} - e^{\left(-\sqrt{\frac{4}{\lambda}}L\right)}}\right]$$

$$N_3 = -\left[\frac{\left(V_{bi} + V_{fb} + \frac{\lambda q N_a}{4\epsilon_{si}}\right)\left(1 - e^{\left(\sqrt{\frac{4}{\lambda}}L\right)}\right) + V_{ds}}{e^{\left(\sqrt{\frac{4}{\lambda}}L\right)} - e^{\left(-\sqrt{\frac{4}{\lambda}}L\right)}}\right]$$

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$$N_4 = -\left[\frac{\left(1 - e^{\left(\sqrt{\frac{4}{\lambda}}L\right)}\right)}{e^{\left(\sqrt{\frac{4}{\lambda}}L\right)} - e^{\left(\sqrt{\frac{4}{\lambda}}L\right)}}\right]$$

$$N_5 = 4\left(1 - \frac{{t_{si}}^2}{\lambda}\right)$$

IV DEVICE SIMULATION

In this section, results are obtained from the theoretical models of the center potential compared with numerical simulation results. In our results inversion layer formation is not very prominent so neglected.

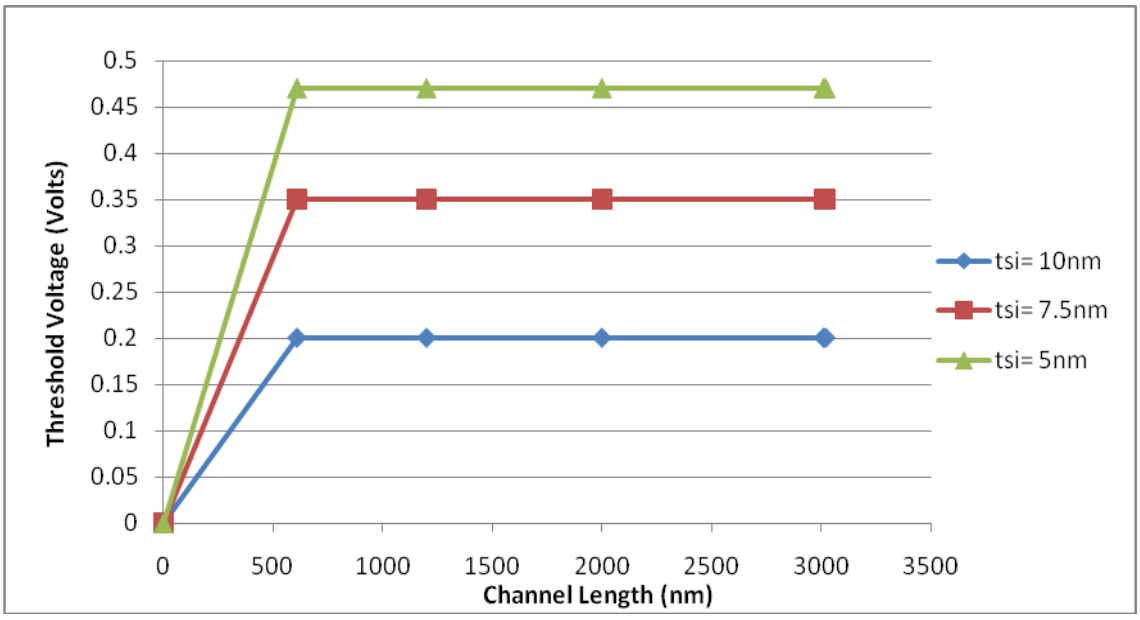

Fig.2: Threshold voltage with change in channel length at various values of t_{si}

Fig.2 shows variation of threshold voltage along the increasing channel length for different silicon film thickness. It can be seen that V_{th} increases with decrease in Si film thickness. V_{th} increases initially but after a certain value becomes constant with increase in channel length. We have considered standard value upto10nm for silicon film thickness in the channel.

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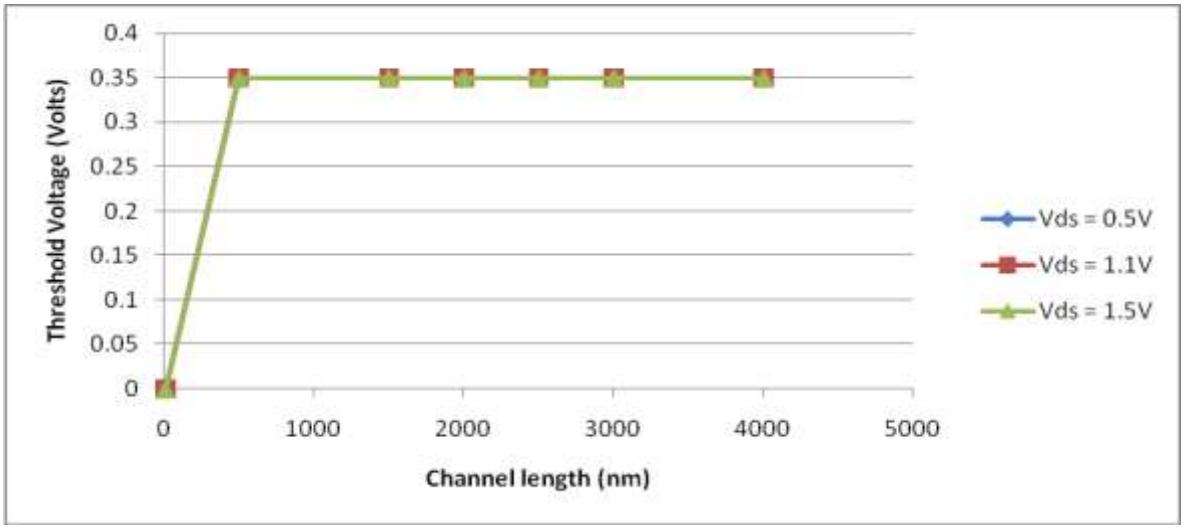

Fig.3: Threshold voltage with change in channel length at various values of V_{ds}

Fig.3 shows the variation of threshold voltage along the increasing channel length for different drain bias voltage. The plot shows that the threshold voltage is independent of variation in drain to bias voltage during the turning on of the device. So no matter how channel length varies, the threshold voltage variation remain same across for all drain to source voltages.

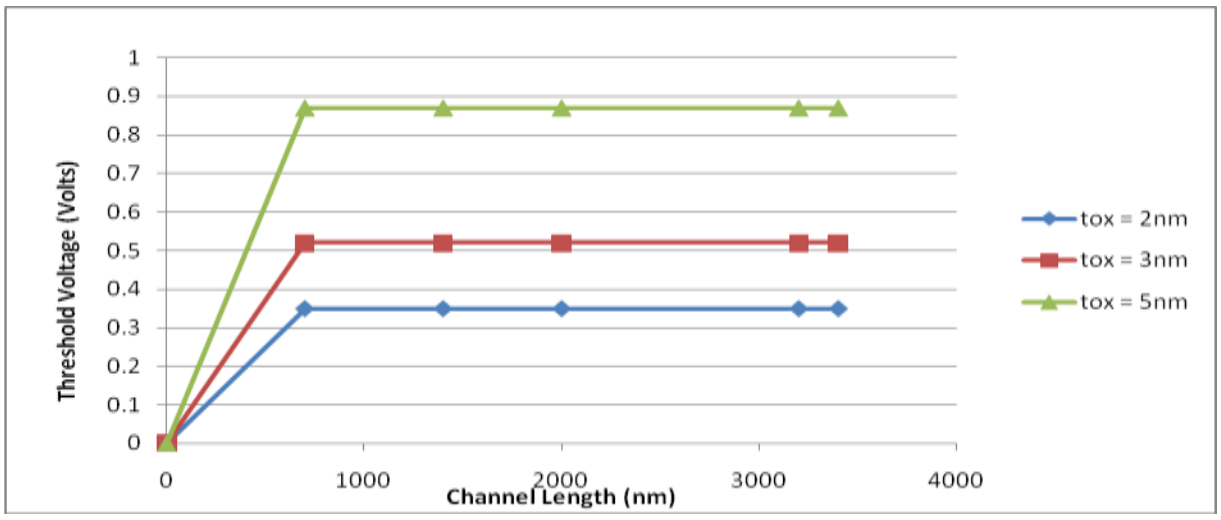

Fig.4: Threshold voltage with change in channel length at various values of t_{ox}

Fig.4 shows the variation of the threshold voltage along the increasing channel length for different gate oxide thicknesses. The graph indicates that larger the gate oxide thickness greater the threshold voltage roll off and loss of

control on channel by gate is gradual with increase in gate thickness. In above graph we have assumed standard values of gate oxide thickness upto 5nm. So we need to scale the thickness in order to remove the shortcomings in the device thereby increasing the device efficiency.

V CONCLUSION

The 2D simulations were carried out for various parameters for the centre potential model of CGAA MOSFET. The graphical values by MATHCAD15 are well matched with the values obtained from SILVACO in the device simulation of cylindrical Gate All Around MOSFET. The developed model will be useful to advance the device parameters for the desired performance and for device parameters to be well scaled for use in the circuit.

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