International Journal of Advance Research in Science and Engineering
Vol. No.5, Issue No. 04, April 2016
www.ijarse.com
IJARSE
ISSN 2319 - 8354

ANALYTICAL MODELING AND CHARACTERIZATION OF FINFET

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ABSTRACT

FinFET transistors use standard drain and source contacts which takes less power and is exposed to less heat which helps in improving the processor performance and this performance won't fall similar to the traditional chip. On the other hand, the results delivered by the processor are of superior returns. Therefore, all the chip makers preferFinFET technology. Another important reason is, the stand-by time power consumption of FinFET transistors is very less. These two key reasons are finally pushing almost all the chipset makers toward this newFinFET technology. We have calculated the value of Vth by summing up the values of Vth for two different cross-sections of the bulk FinFET. We have divided the FET into two sections. First one is the side-channel view (cross-sectional view)and the second one is the narrow-channel view (top view). Thus by summing up these both the voltages, we get Vth.

Keywords: Bulk FinFET, Gate length, Gate height, Threshold Voltage

I INTRODUCTION

The traditional transistor or normal MOSFET require significant amount of power so the entire circuit present on the chip will also require a larger amount of power due to the presence of many transistors in the circuit on the chip. And due to this high consumption of power, theprocessor's sustainability will be reduced along with the increase in the amount ofdissipation of heat energy, which is never preferred by the chipset developers. As ofFinFET transistors, they use standard drain and source contacts so they consume less power and dissipate less heat so the processor's performance would not be similar to that of the traditional chip. FinFETs have negligible short channel effects (SCEs) for almost all types of technologies used (this is 40-nm technology node) and beyond. Development in the production and research ofbulk tri-gate FinFET devices is also rapidly increasing in complexity in generation as it is a nano-scale device. Some production devices have incorporated rounded corners, work-function engineering, channel-strain engineering, and also fin-body doping. In addition to this, research devices also possessmultithreshold voltage (*V*th) techniques through work function engineering and gate–source/drain (G–S/D) overlapping and by fin doping. Planar transistor scaling found in deep-sub micrometer

CMOS technology has almost attained its limits at sub-40-nm nodes and it isdue to very poor electrostatic integrity. This electrostatic integrity is manifested as degraded short-channel effect and also high leakage current. Multigate field-effect transistors (FETs) can overcome these issues because of higher control attained by channel potential over multiple gates wrapped around the FETs body. Amongst multigate FETs, FinFETs have majorly emerged as the best structures from a fabrication perspective.

As the planar MOSFETs shows a significant SCE (Short Channel Effect) and the devices are highly affected by this problem, the designers are paying more attention to FinFETs, because FinFETs have negligible SCE for the same channel length.This difference is obtained due to higher grip of gate over the channel in case of FinFETs as compared to that of planar MOSFETs. The channel in planar MOSFET is horizontal whereas inFinFETs channel is vertical as well as horizontal (also known as the fin). So, the channel height (Hg) determines the fin-width (W) of the FinFET. This is known as width quantization. According to width quantization the width of the FinFET must be more than twice of Hg. Thus, random Fin-widths are not possible. As smaller fin heights can offer more flexibility, thereby multiple fins, leading to more silicon area. But, taller fins shares less silicon footprint, and may also result in the instability of the FinFET structure.

II DEVICE STRUCTURE

From the time of fabrication of MOSFETs, the minimum length of the FET channel has been continuously shrinking.One of the main reasonsbehind this reduction has been an increasing rate of interest in high-speed devices in very large-scale integrated circuits (VLSI circuits). In order to sustain the scaling of conventional bulk devices, there is a requirement of innovations to circumvent the main barriers of fundamental physics that are responsible for constraining the conventional MOSFET device structure. The limits which are very often cited to control the density and position of dopants which provide high current (On and Off) ratio. It also provides finite sub threshold slope and quantum-mechanical tunneling of majority charge carriers through thin gate, from drain to source and also from drain to body.

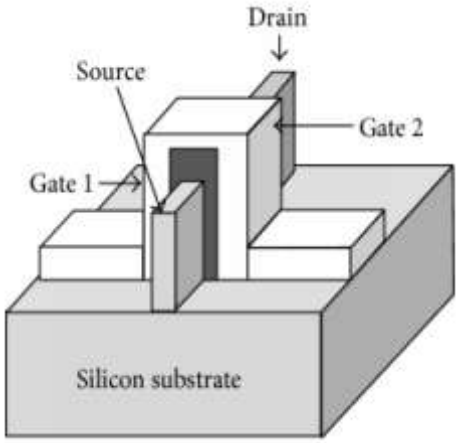

Fig.1: Structure of FinFET

Though the most often type of FinFETs are implemented on SOI, they are also being implemented on conventional bulk wafers vastly. FinFETscan be easily implemented on SOI and Bulk wafers. In bulk FinFETs, all fins have a common Silicon substrate (known as bulk).FinFETs can be implemented or fabricatedin different directions with their channel along,in a single die itself.Here are the parameters taken into consideration for our research, the gate length (Lg) of FinFET is 10 nm, the fin height (Hg) is 40 nm, and the fin width (Wg) is 20 nm. As the drain current flows on the top as well as on the sidewalls of the fin and the devices under observation consists of a single fingers (N = 1), the total effective width is calculated as $W = N \times (2Hg + Wg) = 100$ nm.

III THEORITICAL CALCULATIONS

We have calculated the value of Vth by summing up the values of Vth for two different cross-sections of the bulk FinFET. We have divided the FET into two sections. First one is the side-channel view (cross-sectional view)and the second one is the narrow-channel view (top view).

The threshold voltage for the side-channel view is calculated as the threshold voltage for the DG MOSFET. The side-channel is analyzed as a DG MOSFET as the center portion is either source or drain(as per the side chosen for analysis) and is surrounded by gate on both sides.

So,

The depletion width of this region is calculated as,

$$x_{dep} = 0.5W_f$$

This depletion width is used for the calculation of voltage in the source too drain channel region. In order to calculate the value of final threshold voltage we also need the flat-band voltage (V_{fb})

Hence, threshold voltage can be calculated by,

$$V_{th,SCE} = V_{fb} + \varphi_b + \left(q.N_b.\frac{x_{dep}}{C_{ox}}\right) + (1 - x_h/L).$$

Then we calculate threshold value for the narrow-width i.e., the top view. When we observe the FET from the top it is analyzed as simple MOSFET. The gate lies between the source and drain.

As we know that this NWE region (Narrow width region) or the top-view region is observed in the planar MOSFETs, therefore the threshold voltage is calculated in a similar manner as that of simple planar MOSFETs.

So,

We firstly calculate the depletion width for the MOSFET,

$$x_{df} = V_{ths}.\left(\frac{8\varepsilon_{ox}}{\pi^2}.x_{dep}.q.N_b\right).\ln\left(1 + \frac{T_{gate}}{T_{ox}}\right)$$

And then we calculate the threshold voltage,

$$V_{ths} = V_{fb} + 2\varphi_b + \sqrt{2\varepsilon_s.q.N_a.\left(\frac{2\varphi_b}{C_{ox}}\right)}$$

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Finally, we add the threshold voltages of both the portions in order to achieve the final the FinFET.

$$V_{th} = V_{fb} + 2\varphi_b + \delta_w + \frac{q.N_b.x_{dep}}{C_{ox}}.\left[1 - \left\lfloor\frac{x_h}{(L-2x_m)}\right\rfloor\frac{\pi.x_{df}}{4H_g}\right]$$

The other variables which are to be calculated for the final calculation of Vth are

the feedback voltage is calculated as,

$$V_{fb} = \emptyset_{ms}$$

and

$$\emptyset_{ms} = -\left(\frac{E_g}{2e} + \varphi_b\right)$$

IV DEVICE SIMULATION

The mathematical simulation of this device is conducted on the tool called MathCAD15.

There is a list of constants that are used in the calculation of different variable for the final calculation of Vth.

Table 1: Constant parameters used for calculations

Constants Used	Constant Values
εs	11.7*εo
εox	8.8*εo
Na	$2*10^{18}$
Nb	$3*10^{18}$
Ni	$2.14*10^{18}$
q	$1.6*10^{-19}$
Δw	0.47
χ_{Si}	20.75
Π	3.14
e	$1.6*10^{-19}$
K	$1.13*10^{-23}$
Eg	1.6eV
Xm	0.16nm
Xh	20nm
Tgate	30nm
Tox	1.5nm

In this section, results are obtained from the theoretical models of the threshold voltage compared with numerical simulation results. The voltage is calculated on the basis changes occurring in the height and length of the FinFET gate channel.

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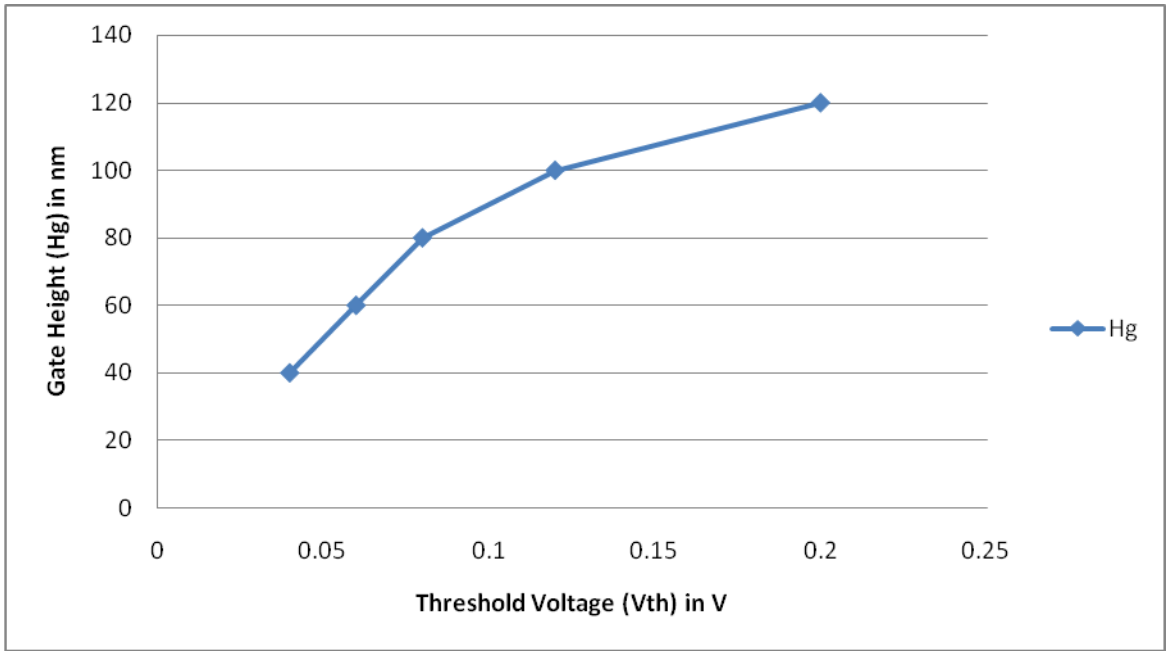

Fig.2 shows variation of threshold voltage along with the variations in the height of the FET gate.

The changes occurring in threshold voltage are gradual with respect to gate height. As the gate height increases the value of Vth also increases but this variation becomes almost constant after a certain (in this case 120nm approx.)

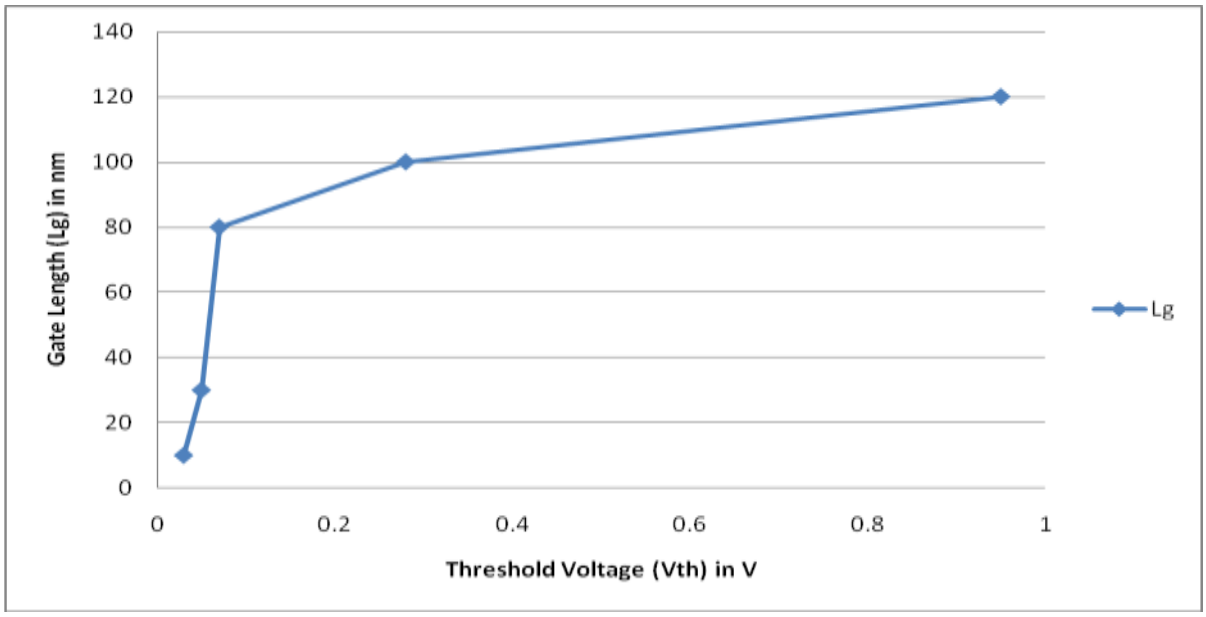

Fig.3 shows variation of threshold voltage along with the variations in the length of the FET gate.

The threshold voltage (Vth) varies for different gate-lengths (Lg) firstly in an exponential way and then in a very slow manner. As we increase the gate-length (Lg), up to a particular value of Lg the threshold voltage increases exponentially but after that value of Lg , the graph of Vth varies very slowly.

V CONCLUSION

Circuit designers can look forward to enjoying a relatively seamless transition and significant benefits from FinFET technology. There are many companies or industries which are responsible for the further research work in this field like Synopsys is trying to create IP, tools, flows and also expertise in FinFETs that will help in guiding the designing community towards the appropriate and successful adoption of this radical change in technology of semiconductors.

Earlier, design teams use to transition their IP from older planar MOSFET technologies to the process nodes with the help of their in-house design capabilities and also the re-use of IPs. But now,FinFET technology has started creating new challenges for different the design teams, as their current tools and techniques of these teams may not help them in optimally designing the IPs for FinFET processes, thereby delaying time to marketthe product. FinFETs require a new generation of design experience, expertise and tools in order to get the most from the technology.

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