RELIABILITY ASSESSMENT OF LOW POWER AND PARAMETRIC INTERRUPTION BREAK REDUCTION IN TSV (THROUGH-SILICON-VIA) BASED 3D-ICS

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ABSTRACT

Power consumption and Reducing the parametric interruption has become an important concern in 3D IC technologies. This paper deals with both low power and parametric interruption analysis for Through-Silicon-Via (TSV) based on 3D ICs. Initially considering about TSV count, wire length, and the parameter interruption break could occur in a TSV. The wire length reduction based on tree generation Method of Mean and Medians (3D MMM) algorithm. It can be establish possible number of TSV count to minimize the overall power consumption. Parametric interruption break could occur in a TSV of a 3D-ICs due to manufacturing imperfection. Finding of such a break is must for imperfectness diagnosing, yield learning, and /or reliability viewing. To test those defect, paper is about an innovative plan-for-testability technique titled as Inconsistent Output Threshold (IOT). Disclosing that by dynamically shifting output of a TSV from a normal inverter to a Schmitt-Trigger inverter, the parametric interruption break on the TSV can be characterized and detected. Utilizing IOT analysis technique for further derive the propagation delay of each TSV participating in an oscillation ring through extract process. In this process, have consider bother the strength of the two TSV drivers, and then measure their effects in terms of change in the oscillation ring's period. By some following analysis, the propagation delay of each TSV can be revealed so the parametric delay fault on TSV can be characterized and perceive. SPICE simulation reveals that this model remains good change when there is significant process variation. A scalable test infrastructure indicates that the test time is modest at only 0.126 ms and 0.0527 ms for 2 TSVs, when the test clock is running at 10 MHz.

Keywords: 3-D ICs, Inconsistent Output Threshold, Oscillation ring, Parametric interruption, Through-silicon-via.

I. INTRODUCTION

A 3D integrated circuits, the idea behind 3D IC's is to mount two or more dice on top of each other. An individual die is now so thin it would be possible to mount 100 on top of each other to form a cube. Another technique is to take a group of dice that all perform an identical function (for example like memory chips) to build them into a 3D stack. In a modern framework, it will involve at least one die being mounted on the top of

another die, with the lower die employing TSVs to allow the upper die to communicate with the lower die and the SiP substrate. It can have a memory die attached to a logic die (or vice versa), or an analog/RF die attached to a digital logic die. [10] and so on.

A through-silicon-via (TSV) is a vertical electrical connection passing completely through a silicon wafer or die. TSVs are a high performance technique used to create 3D packages and 3D integrated circuits, compared to alternatives such as package-on-package, because the density of the VIAs(Vertical Interconnect Access). It is substantially higher because the length of the connections is shorter [15]. A 3D integrated circuit (3D IC) is a single integrated circuit built by stacking silicon wafers and/or dies interconnecting them vertically, so that they behave as a single device. By using TSV technology 3D ICs can pack a great deal of functionality into a small "footprint." The different devices in the stack may be heterogeneous, e.g. combining CMOS logic, DRAM and other materials into a single IC [13].

A catastrophic fault is a sudden and total failure of some system where recovery is impossible. Catastrophic failures often lead to cascading system failures. The term is most commonly used for structural failures but has often extended for many other disciplines where total and irrecoverable loss occurs [14]. The stages of the ring oscillator are often differential stages that are more immune to external disturbances. This renders are also available in non inverting stages. A ring oscillator can be made with a mix of inverting and non inverting stages by providing the total number of odd inverting stages. The oscillator period in all cases is equal to twice the sum of the individual delay in all the stages [12]. In unspecialized, a TSV is a inaccurate interconnecting conductor, with very petite resistance but extensive condenser. An in-depth investigating of the interlink inactivity supporter can be institute in [17].

A design for outspoken break menstruation was planned, in which the oscillation strip construct was applied to remember the inactivity of a cadre in a closed-loop sort [5]. Moreover, the RO can be used to essay stuck-at faults and retard faults related with the connect wires in a 2-D IC, as demonstrated in [13], [14], and [18]. These schemes, though potent, may not be pronto practical to the TSVs in a 3-D IC. Very lately, a method was planned in to notice parametric detain faults. It incorporates a transistor connecting at each TSV to make a voltage mortal with the faulty resistivity of the TSV, and uses an similarity comparator to observe the resulting voltage to execute a pass/fail try. The method requires an analog reference voltage scattered to all TSVs low effort. In this theme, we give a two-step characterization-based judge method [8]. Prototypic, we resemble the propagation break crossways a TSV with a resistive unsettled charge. Wares, passing a tryout resolution either based on a test threshold or finished outlier reasoning.

At the intuition of this method is a new technique called *Inconsistent Output Threshold* (IOT) [21]. The IOT group is implemented with an RO structure consisting of two TSVs and a enumerate of logic entrepreneur. The great dimension that differentiates it from all previous RO-based schemes is that each TSV's turnout inverter is outfitted with a shifting threshold, significant that it can be obsessed to bear equal a natural CMOS logic inverter or a Schmitt-Trigger inverter (with unbalanced 0 → 1 and 1→ 0 thresholds) [22][23]. The most eminent conception of this theme can be explicit are given by dynamical the TSV's output inverter from a normal one to an Schmitt Trigger, the undulation period of the RO will change, with the disagreement reflecting the propagation delay crossways the TSV. The rest of this paper is corporate in next portion II provides aspect aggregation, including essential electrical model of a TSV, and a short review of IOT analysis [21]. Portion III

proposes the new architecture supporting the IOT scheme and its operations. Portion IV presents the experimental results, and Portion V concludes this paper.

II. TSV STRUCTURE

The TSVs that are fabricated after all the transistors and metal layers are formed. Fig. 1. shows the cross-sectional view that a die with TSVs. Circuits in a die use the top-level metal (front metal) to connect a TSV with other circuit elements in the design and the bottom of a TSV is connected with some back metal which is utilized to link to another die's front metal when two dies are bonded.

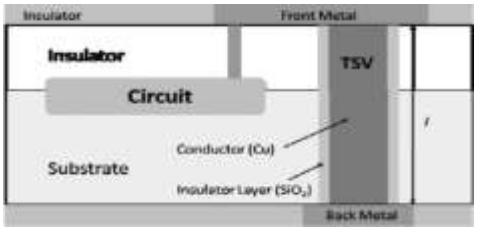


Fig 1: Cross Section View of TSV

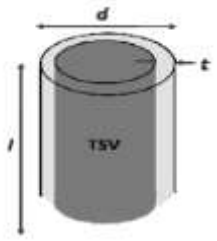


Fig 2: Cylindrical Structure of TSV

The conductor of TSVs could be copper or other metal material. It is isolated from Si substrate with insulator layer (e.g., SiO). Fig. 2. Shows the 3-D structure of a TSV as in a cylinder shape [9].

2.1 RC MODEL

Analytically, model of resistance and capacitance of TSV by the following equations, where *l* and *d* are the length and diameter of the TSV, *t* is the thickness of the insulator (SiO_2) between the silicon substrate and the Copper material inside the TSV ρCu is the Copper resistivity and ϵSiO_2[6].

$$R = \rho \times l/A \quad (1)$$

Providing parasitic RC characteristics of TSV and Micro-bumps, the capacitance changes according to voltage Vg, depends on Vfb & Vth the dielectric constant of SiO_2.

Accumulation : (Vg < Vfb)

$$C = Cox \quad (2)$$

Depletion : (Vfb < Vg < Vth)

$$C = Cox\ Cdep / (Cox + Cdep) \quad (3)$$

Inversion : (Vg > Vth)

$$C = Cox\ Cdep / (Cox + Cdep) \quad (4)$$

TABLE 1: Values of resistance and capacitance

	Normal	Best	Worst
Resistance (mΩ)	46	39	56
Capacitance (fF)	122	105	141

The values of resistance and capacitance are calculated according to voltage Vg depends on three regions from that three cases values normal, best and worst are obtained. We can use the normal or best values to do the RC modeling for TSV.

III. TSV INTERRUPTION MODEL

3.1 TSV Modeling

For a TSV with physical parameters resistance (RTSV) and capacitance (CTSV) are to be deliberate using length, surrounding oxide wideness, and length. Supported on an analytical TSV RC models presented, the significant term invariable of this wire. This is an extremely small valuate compared to the essential gate delay (which is in the extent of tens to hundreds of picoseconds in a exemplary 0.25μm impact). Nevertheless, the condenser of a TSV is much larger than that of an on-chip interconnect [17]. As a prove, the detain caused by a TSV is not in the wire itself, but in its dynamic gate. Supported on this observation, have defined the TSV delay as the overall propagation delay crosswise the TSV structure and its driver gate [13].

3.2 Delay Model in Transmission Line of A TSV

A TSV can be viewed as a transmission conductor, which takes its effect of its inductance and its conductance to surface, as shown in Fig. 3. This image also shows the connections of the R, L, C, and G as celebrity that the effects of the inductance L and the conductance G may not be negligible when the TSV is utilized for transmitting a high frequency analog signal. To verify the above statement, perform of the RLCG model, with the inductance increased 1000× from its typical value to 2.8 nH. The waveforms will occurs to applied input as 0→1 of the TSV inverting driver. In Fig. 4. A 1→0 transition is observed at the endpoint of the TSV B [9] [19]. The output transition at node B exhibits low-amplitude ripples due to the increased inductance but overall, the propagation delay of the signal remains almost unchanged. The CTSV will dominate the delay of a fault-free TSV. However, RTSV could have a significant impact on a faulty TSV if its value is large enough to be comparable to the effective on-resistance of the driver.

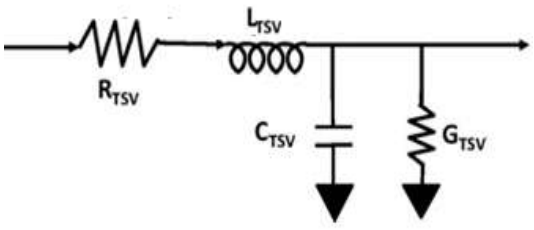


Fig 3: Transmission line-based circuit model for a TSV

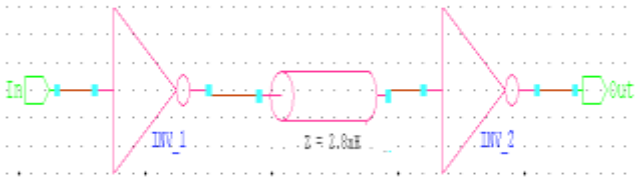


Fig 4: Simulation of a Signal propagating through a TSV

3.3 INPUT SENSITIVE ANALYSIS

In this section, review the most related previous work proposed in referred to as input-sensitivity (IS) analysis, which aimed to predict the capacitance of each TSV under test. As shown in Fig 5 two TSVs are paired to form

a RO. The resulting period of the RO is twice the propagation delay around the ring. Observing the oscillation period of this RO can reveal certain delay information. The RO can be dynamically set to one of three different configurations by tuning the strengths of the input drivers of the two TSVs, namely:

1) Normal configuration.
2) TSV1−driver−reduced configuration
3) TSV2−driver−reduced configuration

During test mode, the three RO configurations are turned on in sequence and the oscillation period of each configuration is measured. A procedure is then followed to map the measurement results to the capacitance and propagation delay across each of the two TSVs [20]. The main idea of the IS analysis is that the capacitance of a TSV can be reflected in the change of the oscillation period of the RO, while perturb the driving strength of the input buffer of that TSV, regardless of the periphery circuit in the oscillation ring. Although the IS analysis can capture the effect of the TSV capacitance, it has a limitation of not being able to factor in the effect of the TSV resistance (which affects the wire part of the TSV delay) when the TSV is highly resistive [19] [20]. This is a drawback that might not be very detrimental if one only attempts to use it to gauge the TSV's capacitance or to profile the delays across mostly fault-free TSVs. But it is a problem if one attempts to measure the delay across a faulty TSV with a resistive open fault.

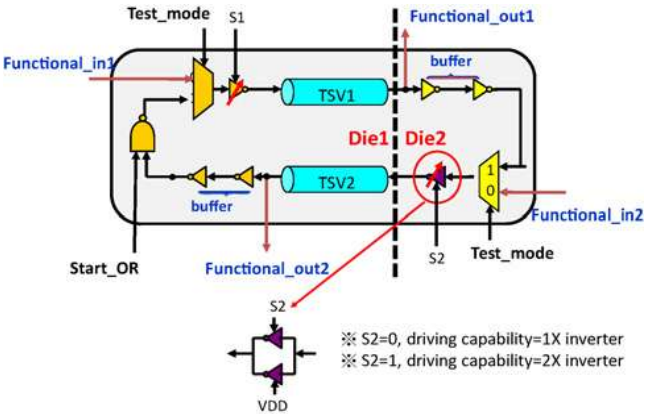


Fig 5: Architecture for a TSV pair

IV. INCONSISTENT OUTPUT THRESHOLD TECHNIQUE

4.1 Operating of Schmitt Trigger Inverter

The having investigated the behavior of high-gain amplifier with no feedback, now turn to amplifier with positive feedback, also known as Schmitt Triggers. Schmitt Trigger is a wave shaping circuit, used for generating of square wave. It is a bi-stable circuit in which two transistor switches are connected re-generatively [22]. It has a hysteresis property, The hysteresis in Schmitt trigger is valuable when conditioning noisy signals for using digital circuit. The noise does not causes false triggering and so the output will be free from noise. The input import that a larger-than practice input voltage drop is required to change the output logic level. In opposite line, impoverishment a higher voltage to locomote the output of a Schmitt Trigger inverter from "1" to "0," and lower voltage to alter the output from "0" to "1" as shown in Fig. 6.

The hysteresis property requires two different thresholds:

1) A high-to-low threshold, is given as HL

2) A low-to-high threshold, is given as LH , as can be seen in the voltage transfer curve obtained by SPICE simulation using a 0.25 µm CMOS process. The high-to-low threshold, HL, is the input voltage beyond which one can change the output state from "1" to "0," while low-to-high threshold, LH, is the input voltage below which one can change the output state from "0" to "1." In detail, the drive-up path and the drive-down path of an Schmitt Trigger inverter are each composed of two transistors in cascade. The hysteresis property is created by slightly dragging the voltage of the mid points of the drive-up and drive-down paths, to take advantage of the body effect of MOS transistors.

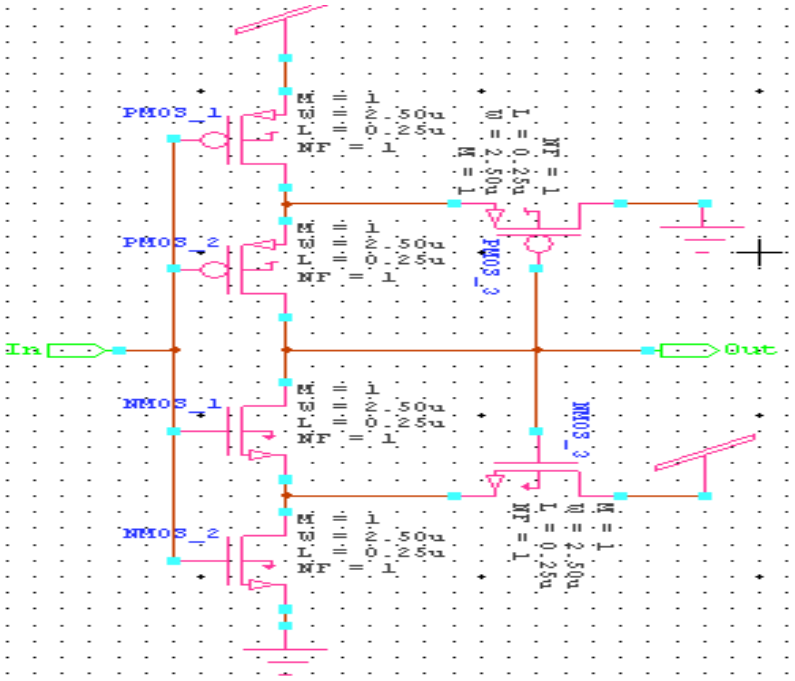


Fig 6: Schmitt – Trigger Inverter

4.2 Structure of IOT Analysis

As illustrated in Fig. 7. a pair of TSVs is configured into an RO, similar to the IS analysis. To support the IOT analysis, there is a change in the output inverter of each TSV with variable threshold, as defined. A IOT inverter is the combination of a normal CMOS inverter and an ST inverter, with the function depending on the value of a control signal 'X'.

In other words, a IOT inverter operates in two different modes:

1) Common approach
2) Schmitt Trigger approach

When X = 0, IOT inverter = Common CMOS inverter. While X = 1, IOT inverter = Schmitt Trigger inverter.

There are two IOT inverters in a test unit composed of two TSVs as shown in Fig. 7, one for each TSV. Their controlling signals are denoted as X_1 (for the IOT inverter of the TSV_1) and X_2 (for the IOT inverter of the TSV_2).

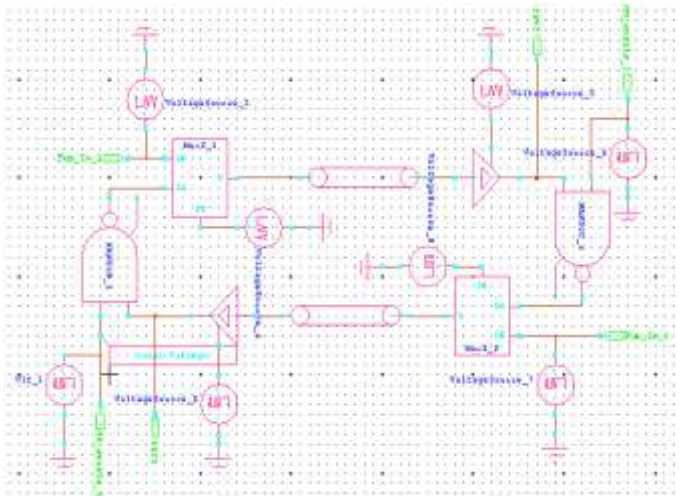


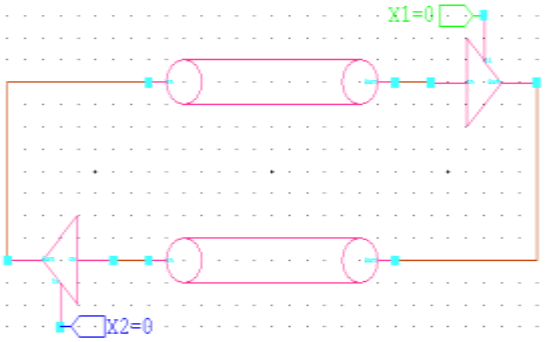
Fig 7: Schmitt of a TSV Supporting IOT

Based on the value combination of <X_1, X_2>, three configurations in IOT analysis are as summarized in (Fig. 8., Fig. 9., Fig. 10.)

1) Normal Design: (X_1, X_2) = (0, 0), i.e., both IOT inverters are in their Common approach. The oscillation period of the RO is denoted as T_{REF}

2) TSV_1-in-ST Design: (X_1, X_2)= (1, 0), i.e., the IOT inverter associated with TSV_1 is in the Schmitt Trigger approach, while that of TSV_2 is in its common approach. The oscillation period of the resulting RO is denoted as $T_{ST1.}$

3) TSV_2-in-ST Design: X_1, X_2 = (0, 1), i.e., the IOT inverter associated with TSV_2 is in the Schmitt Trigger approach, while that of TSV_1 is in its common approach. The oscillation period of the resulting RO is denoted as T_{ST2}.



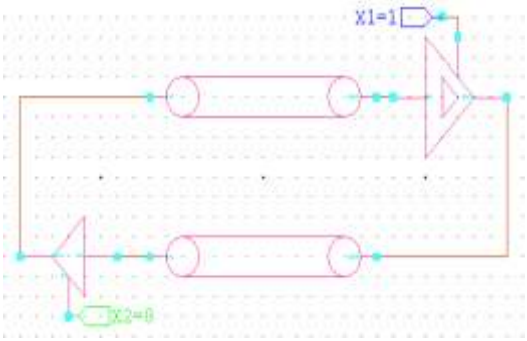


Fig 8: Common Configuration **Fig 9: TSV1 in Schmitt Trigger**

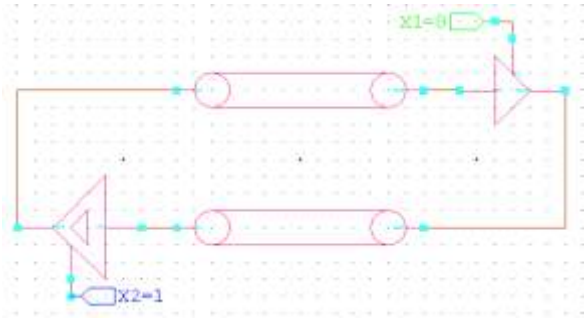


Fig 10: TSV2 in Schmitt Trigger

A IOT inverter can be realized by a schematic as shown in Fig. 11. Its equivalent circuit is depicted when the control signal X is "0" (in which case it becomes to a common inverter). When the control signal X is "1" (in which case it becomes to an Schmitt Trigger inverter).

4.3 Overall Flow

There are three major steps in the measurement phase for each test unit (composed of a TSV pair) shown in Fig. 12.

In step 1, activating the RO in its normal configuration and measuring the result oscillation period, denoted as T_{REF}.

In step 2, activating the RO in its TSV1-in-ST configuration and measuring the resulting oscillation period, denoted as T_{ST1}.

In step 3, activating the RO in its TSV2-in-ST configuration and measuring the resulting oscillation period, denoted as TST2. In the prediction phase, following computations are to be done.

$$\Delta T_{ST1} = T_{ST1} - T_{REF} \qquad \Delta T_{ST2} = T_{ST2} - T_{REF}$$

The two derived timing parameters ΔT_{ST1} and ΔT_{ST2} can be regarded as the timing signatures of the two TSVs (ΔT_{ST1} for TSV1 and ΔT_{ST2} for TSV2). They are correlated with the TSV delays, with the following rationale.

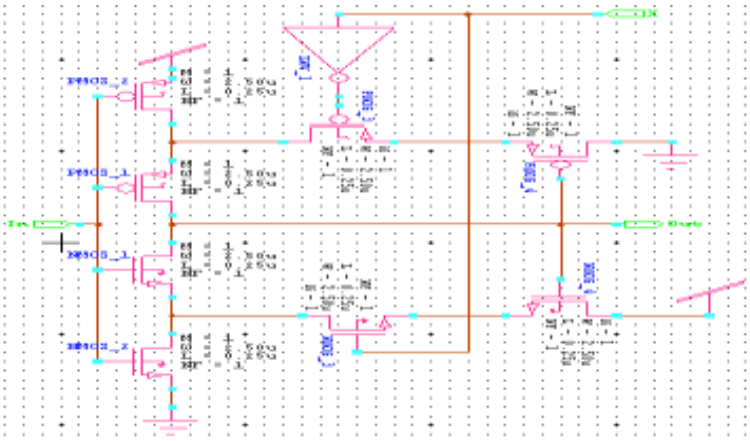


Fig 11: Operation Between a common and ST inverter

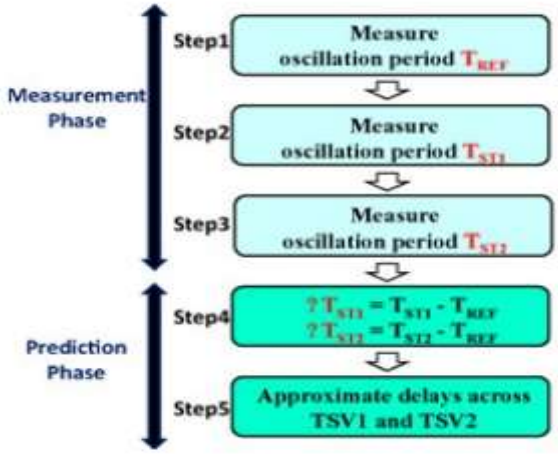


Fig 12: Overall Flow for TSV delay observation

A larger TSV delay (due to excessive R) induces a larger rise/fall time in the signal waveform at the endpoint of the TSV. At the output of the IOT inverter, the rise/fall time will translate into a measurable period difference between the normal configuration and the TSV-in-ST configuration. It is notable [9],[19],[20] that the delays due to the peripheral circuitry in the RO (such as the multiplexers and the triggering XOR gates) have been canceled out, since to calculate $\Delta T_{ST} = (T_{ST} - T_{REF})$ and thus ΔT_{ST} will reflect only the delay across the associated T_{SV}. It is also notable that even though the traditional oscillation ring formed by a TSV pair without IOT inverters might be able to reflect the extra TSV delay for fault detection, it has one major drawback compared to this method, when observing a larger-than-normal oscillation period using the traditional oscillation ring, it cannot be concluded whether the extra delay is caused by a TSV or other circuitry in the oscillation ring. In contrast, IOT scheme provides a zoom-in view to each TSV delay and provides higher characterization resolution as well as diagnostic capability.

V. EXPERIMENT RESULT

The simulation results that take into account the process variation of our CMOS 0.25µm process.

5.1 IOT Analysis

When X = 0, IOT inverter = Common CMOS inverter.

While X =1, IOT inverter = Schmitt Trigger inverter. When X = 0 and X = 1, The delay measurement are calculated for voltage 0.5 V and frequency at 10 MHz. The maximum difference delay between both approaches 0.13nS.

5.2 Delay and Power Calculation

For Example: TSV Model: C_{TSV} = 50pF, L_{TSV} = 2.8pH, G_{TSV} = 0.1nΩ^{-1}, R_{TSV} = 30mΩ, 3KΩ.

Fig. 13. shows simulation results that takes into account the process variation of our CMOS 0.25 µm process for a TSV with C_{TSV} = 50 pF. In this analysis, a noise-free power supply voltage is given for each TSV faults. Based on the above results, one test flow for parametric delay fault detection can be proceeding as follows. For a test unit, it derives the ΔT_{ST1} and ΔT_{ST2} for the two TSVs by the IOT analysis, respectively. Which are shown in below graph.

At Measurable Phase Of ΔT_{ST1} and ΔT_{ST2} $\Delta T_{ST1} = T_{ST1} - T_{REF} = 0.1265 \times 10^{-6}$sec

$\Delta T_{ST2} = T_{ST2} - T_{REF} = 0.05273 \times 10^{-6}$sec

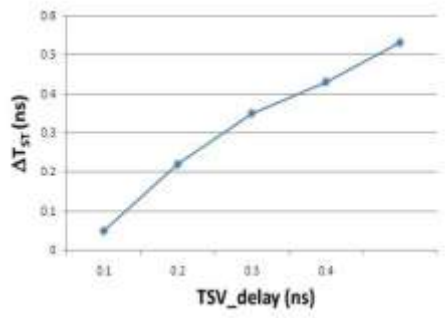


Fig 13: The measurement of Overall Flow for TSV delay Observation

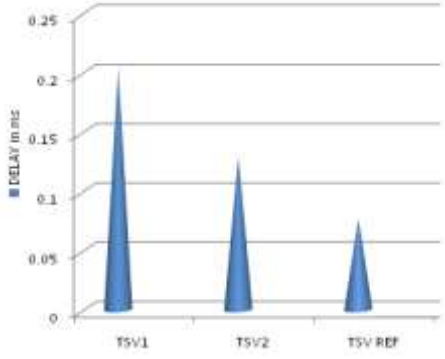


Fig 14: Comparison of T_{REF}, T_{SV1}, T_{SV2} delay Measurement

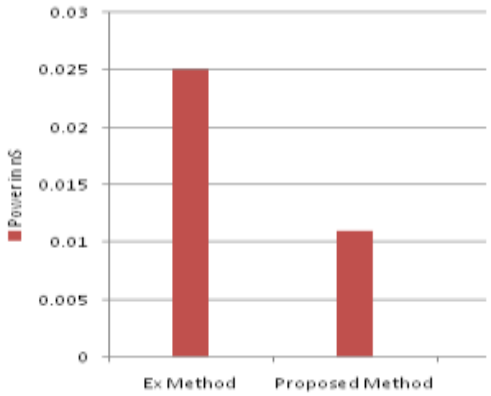


Fig 15: Comparison of Power Calculation

VI. CONCLUSION

The parametric delay reduction methods for TSVs are mostly for gross delay with the values exceeding a target system clock period. It is unique in its ability to characterize the extra delay across a TSV with a resistive open fault. A IOT scheme using only logic circuit was proposed. In this scheme, dynamically switching the inverter of a TSV from a normal inverter to an Schmitt Trigger, the propagation delay across the TSV can be approximated. SPICE simulation validates that there exists a linear relationship between the TSV delay to be quantified and the quantity that can be measured (denoted as ΔT_{ST} by the proposed scheme). The oscillating period of T_{REF}, T_1, T_2 are measured and ΔT_{ST1} and ΔT_{ST2} are calculated. By over flow TSV-delay prediction approximate delay across TSV_1 and TSV_2 are calculated and delay reduced using Schmitt-Trigger inverter. For future enhancement to analyze crosstalk behavior of TSVs in 3-D integrated system.

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