

## EVALUATION OF DELAY FOR MULTI-RATE SIGNAL BY USING FARROW FILTER

Mousumi De<sup>1</sup>, Biswajit Basak<sup>2</sup>

<sup>1</sup> M.Tech Scholar, Microwave & Communication Engineering,  
MCKV Institute of Engineering, Howrah, (India)

<sup>2</sup> Assistant Professor, Dept of ECE, Hooghly Engineering & Technology College,  
Hooghly, (India)

### ABSTRACT

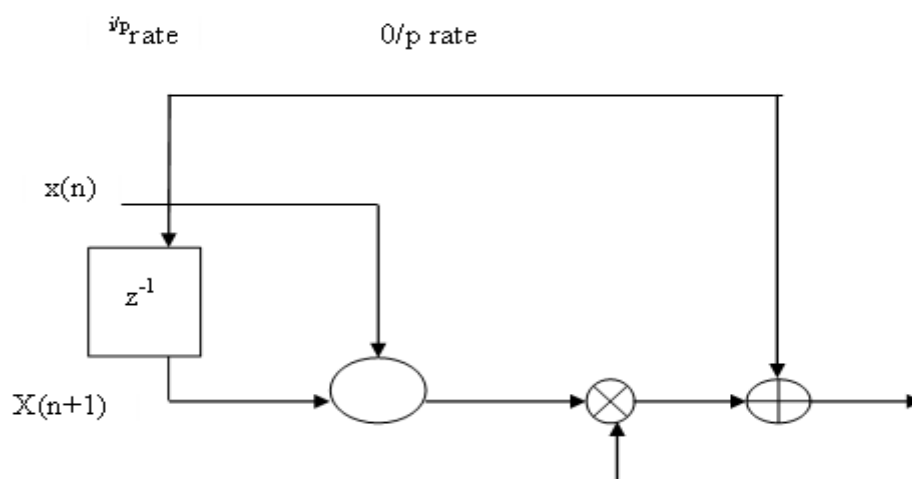
The discrete time systems process the data at more than one sampling rate is called multi-rate system. In this case the sampling rates of signals are unequal at various parts of the system. In all available communication channels achieving maximum signal transfer without any noise, the only frequency processor synchronized with the sampling rate. In this paper evaluate the differential delay of Farrow filters in different sampling frequencies.

### I. INTRODUCTION

Multi-rate systems are used extensively in all areas of digital signal processing (DSP). Their function is to alter the rate of the discrete-time signals, by adding or deleting a portion of the signal samples. They are essential in various standard signal processing techniques such as signal analysis, de-noising, compression and so forth. During the last decade, however, they have increasingly found applications in new and emerging areas of signal processing, as well as in several neighboring disciplines such as digital communications.

One example is sampling rate conversion by arbitrary conversion factors where the traditional interpolators and decimators used for integer and rational-factor conversion fail or imply very high interpolation and decimation factors. An efficient structure

for adjustable FD filtering is the so called Farrow structure which makes use of a number of fixed FIR sub-filters and only one variable parameter.

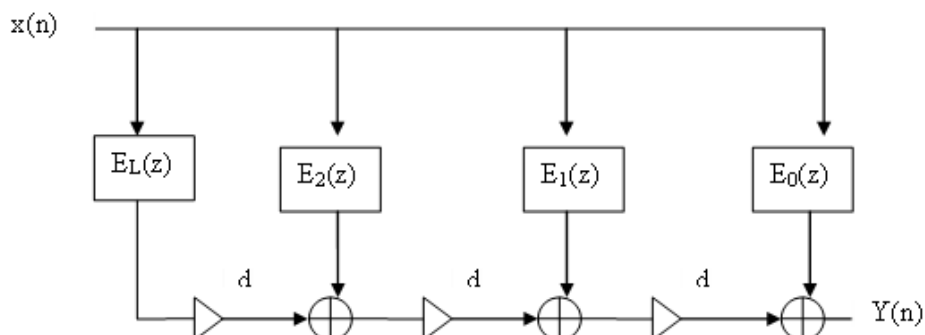


**Diagram: Farrow Structure**

The farrow filters is another class of digital filters which are used extensively in arbitrary sample rate conversions and fractionally delaying the samples. They have polyphase structure and are very efficient for digital filtering. Field-programmable gate array (FPGA) has become an extremely cost-effective means of off-loading computationally intensive digital signal processing algorithms to improve overall system performance. In this paper the farrow filters are implemented for fractional delay and arbitrary change in sample rate conversion. This filters gives a better performance than the common filter structures in terms of speed of operation, cost, and power consumption in real-time. The proposed filter structures have wide applications in the designing of sample rate converters, analog to digital converter, decimators and interpolators.

**II. FARROW FILTER AND DELAY**

When the decimation factor  $1/R$  or the interpolation factor  $R$  is an integral value, then the conversion of sampling rate can be performed conveniently with the aid of fixed digital filters (Farrow, 1998). In case of a scenario where the factors are irrational, it will be impossible to use fixed digital filters directly. Moreover, if  $R$  is considered as the ratio of two relatively large prime integers, then, in the case of the conventional poly-phase implementation, it is quiet essential that the orders of the required filter become very large (Oh et al., 1999). In nutshell, it means that a large number of coefficients need to be stored in coefficient memory. In sampling rate conversion by non-integer factor, it is required to determine the values between existing samples. In this case, it is very convenient to use interpolation filters. Among them, polynomial based filters are generally assumed to provide an efficient implementation form directly in digital domain. Such filters witness an effective implementation through Farrow structure or its higher version (Farrow, 1998; Hentschel and Fettweis, 2000). The main advantage of the Farrow structure is based on the presence of fixed finite-impulse response (FIR) filters as one of its ingredients. Thus, there is only one changeable parameter being the so-called fractional interval  $\mu$ . Besides this, the control of  $\mu$  is easier during the operation than in the corresponding coefficient memory implementations, and the concept of arithmetic preciseness; not the memory size limits the resolution of  $\mu$ . These characteristics of the Farrow structure make it a very attractive structure to be implemented using a VLSI circuit or a signal processor (Vesma, 1999; Fettweis and Hentschel, 2000).



**Diagram: Farrow Filter**

The dashed line separates the filter into a section running at the input signal's sampling-rate and a section running at the output sampling-rate. Note that the output is re-labeled to be  $y[m]$  rather than  $y[n]$ . This is due to different input and output rates. Notably, the fractional delay denoted as  $\beta_m$  will now change at every instant an

output sample occurs. The first time an input is used,  $\beta_m$  will take on the value 0.3 and the output will be computed as

$$Y[m] = 0.5 (x [n-1] - x [n] ) + x[n] = 0.5 x [n-1] + 0.5 x [n] \quad \dots(1)$$

Before the input sample changes, one more output sample will be computed.  $\beta_m$  will take the value 0 and the output will simply be

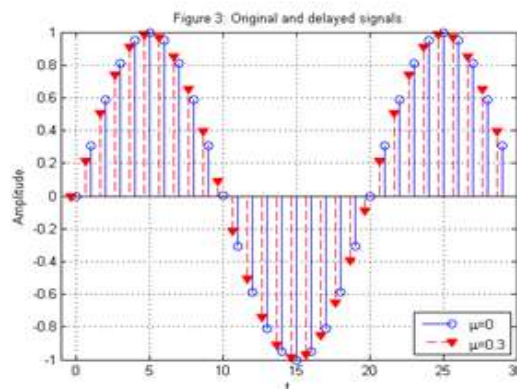
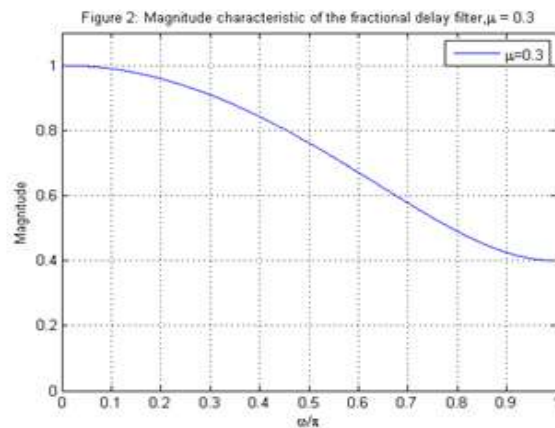
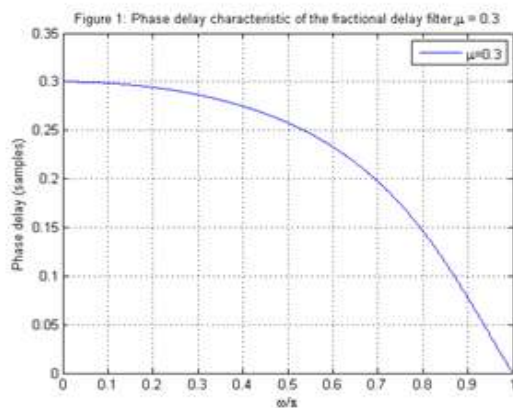
$$Y(m + 1) = x [n] \quad \dots(2)$$

Subsequently, the input sample will change;  $\beta_m$  will be once again set to 0.5 and so forth. In summary, when increasing the sampling rate by a factor of two,  $\beta_m$  will cycle between the values {0.5, 0} twice as fast as the input, producing an output each time it changes. In the general case, it is simply a matter of determining which values  $\beta$  must take. The formula is simply

$$\beta_m = ( m f_s / f'_s ) \bmod 1 \quad \dots(3)$$

Where  $f_s$  is the input sampling rate and  $f'_s$  is the output sampling rate. In order to perform a non integer SRC (sample rate conversion), Farrow structure or its modifications directly can be used. However, in many cases, it becomes more efficient to use cascaded structures engineered by the modification of the Farrow structure and fixed FIR, or multistage FIR filter (Babic et al., 2001, 2002, 2005; Meyer and Bease, 2007). The main advantage of using the cascaded structures instead of the direct modification of the Farrow structure lies in the fact that in case of joint optimization of the two building blocks the computational complexity to generate practically the same filtering performance is dramatically reduced. This is because of the following reasons. First, the implementation of a fixed linear phase FIR interpolator is not very costly, compared to the Farrow structure. Second, most importantly, the requirements for implementing the modification of the Farrow structure become significantly milder. This is mainly because the FIR filter takes care of pass-band and stop-band shaping, where the Farrow-based structure should only take care of attenuating images of FIR filter.

### III. SIMULATION RESULTS



#### IV. DISCUSSION

A farrow filter is a filter of digital type having as main function to delay the processed input signal a fractional of the sampling period time. There are several applications where such signal delay value is required, examples of such systems are: timing adjustment in all-digital receivers (symbol synchronization), conversion between arbitrary sampling frequencies, echo cancellation, speech coding and synthesis, musical instruments modeling etc. In order to achieve the fractional delay filter function, two main frequency-domain specifications must be met by the filter. The filter magnitude frequency response must have an all-pass behavior in a wide frequency range, as well as its phase frequency response must be linear with a fixed fractional slope through the bandwidth.

In this paper consider the input and the output rates in the case of a fractional filter are identical. Just generate the first 30 samples of the signal  $x[n] = \sin(0.1 \cdot \pi \cdot n)$  and perform the fractional delay filtering for the delay factor  $\mu = 0.3$ . Plot the input sequence  $\{x[n]\}$  and the delayed sequence  $\{y[n]\}$ . At first generate the delay signal from 0 to 0.3 and apply it over the sinc function with first 30 samples. Get the fig 1, fig2 and fig 3 respectively.

#### V. CONCLUSION

This paper has considered a multirate approach for fractional-delay filtering. According to the results one of the most challenging approaches for designing fractional delay filters is the use of frequency domain optimization methods. The use of MATLAB as a design and simulation platform is a very useful tool to achieve a fractional delay filter that meets best the required frequency specifications dictated by a particular application.

## REFERENCES

- [1] Diaz-Carmona, J.; Jovanovic-Dolecek, G. & Ramirez-Agundis, A. (2010). Frequency-based optimization design for fractional delay FIR filters. *International Journal of DigitalMultimedia Broadcasting*, Vol.2010, (January 2010), pp. 1-6, ISSN 1687-7578.
- [2] Erup, L.; Gardner, F. & Harris, F. (1993). Interpolation in digital modems-part II: implementation and performance. *IEEE Trans. on Communications*, Vol.41, (June 1993), pp. 998-1008.
- [3] Farrow, C. (1988). A continuously variable digital delay element, *Proceedings of IEEE Int.*
- [4] H. Johansson and P. Löwenborg, "Reconstruction of nonuniformly sampled bandlimited signals by means of digital fractional delay filters," *IEEE Trans. Signal Processing*, vol. 50, no. 11, pp. 2757–2767, Nov. 2002.
- [5] C. W. Farrow, "A continuously variable digital delay element," in *Proc. IEEE Int. Symp. Circuits Syst.*, Espoo, Finland, June 7–9, 1988, vol. 3, pp. 2641–2645.
- [6] J. Vesma and T. Saramäki, "Optimization and efficient implementation of FIR filters with adjustable fractional delay," in *Proc. IEEE Int. Symp. Circuits Syst.*, Hong Kong, June 9–12, 1997, vol. IV, pp. 2256–2259.
- [7] Delay calculation of farrow filter in multirate filter Evaluation of delay for multirate signal by using farrow filter.