A NEW APPROACH FOR DELAY AND LEAKAGE POWER REDUCTION IN CMOS VLSI CIRCUITS

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ABSTRACT

In the nanometer range design technologies dynamic power dissipation is very important issue in present peripheral devices. In the CMOS based VLSI circuits technology is scaling towards down in respect of size and achieving higher operating speeds. We have also considered these parameters such that we can control the leakage power. In the past, the dynamic power has dominated the total power dissipation of CMOS devices. However, with the continuous trend of technology scaling, leakage power is becoming a main contributor to power consumption. In this paper, a technique has been proposed which will reduce simultaneously both delay and leakage power. The results are simulated in Tanner Tool in 90nm and 70 nm CMOS Technologies at 5volt.

Keywords: ***Dynamic power, Leakage power, Multi-threshold, Delay***

I INTRODUCTION

Today leakage power has become an increasingly important issue in processor hardware and software design. With the main component of leakage, the sub-threshold current, exponentially increasing with decreasing device dimensions, leakage commands an ever increasing share in the processor power consumption. In 65 nm and below technologies leakage accounts for 30-40% of processor power.

According to the International Technology Roadmap for Semiconductors (ITRS), leakage power dissipation may eventually dominate total power consumption as technology feature sizes shrink. While there are several process technology and circuit-level solutions to reduce leakage in processors, in this paper a novel approaches for reducing both leakage and dynamic power with minimum possible area and delay tradeoff are proposed.

For the most recent CMOS feature sizes (e.g., 90nm and 65nm), leakage power dissipation has become an overriding concern for VLSI circuit designers. For deep-submicron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. This to an extent reduces the dynamic (switching) power dissipation. However, the sub-threshold leakage current increases exponentially thereby increasing static power dissipation [1].

Modern digital circuits consist of logic gates implemented in the complementary metal oxide semiconductor (CMOS) Technology. Power consumption has two components: Dynamic Power and Leakage power [2]. Dynamic and leakage power both are the main contributors to the total power consumption. Dynamic power

includes both switching power and short circuit power. Spurious transitions (also called glitches) in combinational CMOS logic are a well-known source of unnecessary power dissipation. Reducing glitch power is a highly desirable target [3]. The dynamic power cannot be eliminated completely, because it is caused by the computing activity. It can, however, be reduced by circuit design techniques.

Static power refers to the power dissipation which results from the current leakage produced by CMOS transistor parasitic. Traditionally static power has been overshadowed by dynamic power consumption, but as transistor sizes continue to shrink, static power may overtake dynamic power consumption To alleviate the rising significance of static power in digital systems, static power reduction technique shave been developed like transistor stacking, dual threshold voltage , MTCMOS etc. Some of these techniques are state saving and some are state destructive techniques. For example: Sleep transistor is a state destructive technique. Despite the rising significance of static power in CMOS circuits, the dynamic power is still the major contributor to power consumption.

II POWER DISSIPATION FACTORS

In CMOS, power consumption consists of leakage power and dynamic power Dynamic power includes both switching power and short circuit power. Switching power is consumed when the transistors are in active mode and short circuit power is consume when a pull-up and pull-down network are on turning on and off. For 0.18u and above leakage power is small compared to dynamic power but 0.13u and below leakage power is dominant. Dynamic power dissipation is proportional to the square of the supply voltage. In deep sub-micron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. This, to an extent, reduces the dynamic power dissipation [4].

The leakage current of a transistor is mainly the result of reverse biased PN junction leakage and Sub threshold leakage. Compared to the sub-threshold leakage, the reverse bias PN junction leakage can be ignored. The Sub-threshold conduction or the sub-threshold leakage or the sub-threshold drain current is the current that flows between the source and drain of a MOSFET when the transistor is in sub-threshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage [5].

It is given by:

$Is0=\mu 0 Cox\ (Weff/Leff)$ …… (1)

$P_{LEAK=}\ I_{LEAK}\ V_{DD}$…… (2)

where μ0 is the zero bias electron mobility, Cox is the oxide capacitance per unit area, and Weff and Leff are the effective channel width and length, respectively. V_{DD} is supply voltage and I_{LEAK} is the cumulative leakage current due to all the components of the leakage current.

2.1 Leakage Power Reduction

Leakage current is a primary concern for low-power, high-performance digital CMOS circuits. The exponential increase in the leakage component of the total chip power can be attributed to threshold voltage scaling, which is essential to maintain high performance in active mode, since supply voltages are scaled. Numerous design

techniques have been proposed to reduce standby leakage in digital circuits. Leakage power has become a serious concern in nanometer CMOS technologies, and power-gating has shown to offer a viable solution to the problem with a small penalty in performance [6]

Devices which are operated on battery are either idle (Standby) or Active mode. Leakage power can be divided in to two categories based on these two modes [7]:-

1) **Leakage Control in Standby Mode:** Most microelectronic systems spend considerable time in a standby state. The energy consumed by the logic and the DC-DC converter to enter or exit a low power mode must be considered carefully. If the cost of transitioning to and from a low standby power state is low enough then the greedy policy of entering the low power state as soon as the system is idle may be adopted. Otherwise, the expected duration of the standby state must be accurately calculated and taken into account when devising a power management policy.
2) **Leakage Control in Active Mode:** For circuits whose power consumption is dominated by the leakage power in STAND BY mode, the aforementioned techniques can be used to reduce the power consumption. On the other hand, if a circuit's power consumption is not dominated by the leakage in STAND BY mode, then it is necessary to consider the total power consumption (including switching power dissipation and active mode leakage) and optimize the circuit to reduce it as described next.

2.2 Proposed Method

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift, where power dissipation has become as important a consideration as performance and area. Two components determine the power consumption in a CMOS circuit: Static and Dynamic Power. Static (Leakage) power: includes sub-threshold leakage, drain junction leakage and gate leakage due to tunneling.

Among these, sub-threshold leakage is the most prominent one. Dynamic power: Includes charging and discharging (switching) power and short circuit power. In Dynamic power, power consumption due to switching activity is more prominent. It can be concluded from the above discussion so far that glitch and leakage power both are the main contributors to the power consumption.

A novel technique has been proposed in this section, which will reduce both delay and leakage power in CMOS VLSI circuits. The new technique is Sleep Variable body biasing with transmission gate. The circuit diagram of optimized circuit 1 and optimized circuit 2 is shown in the Fig.1-2.

This proposed design includes variable body biasing technique along with sleep insertion technique. Sleep transistors are crucial part in any low leakage power design. The source of one of the sleep transistor is connected to the body of other PMOS sleep transistor for having body biasing effect. So, leakage reduction in this technique occurs in two ways. Firstly, the sleep transistor effect and secondly, the variable body biasing effect. This technique uses aspect ratio W/L=3 for NMOS transistor and W/L=6 for PMOS transistor. Due to the minimum aspect ratio the sub-threshold current reduces.

Since the sources of the NMOS sleep transistor is connected to the body of PMOS transistor as shown in Fig. 1, the threshold voltage of the sleep transistors increases due to the body biasing effect during sleep mode. This increase of threshold voltage of the transistors reduces the leakage current. That's why the static power consumption also lowers.

The variable biasing will be useful in reducing leakage power. Sleep transistor method provides good reduction in leakage power in idle mode, but it is a state destructive techniques.

Stacking approach is also utilized here to some extent to retain the state in active mode. Variable body biasing will be useful in increasing threshold voltage to reduce leakage current

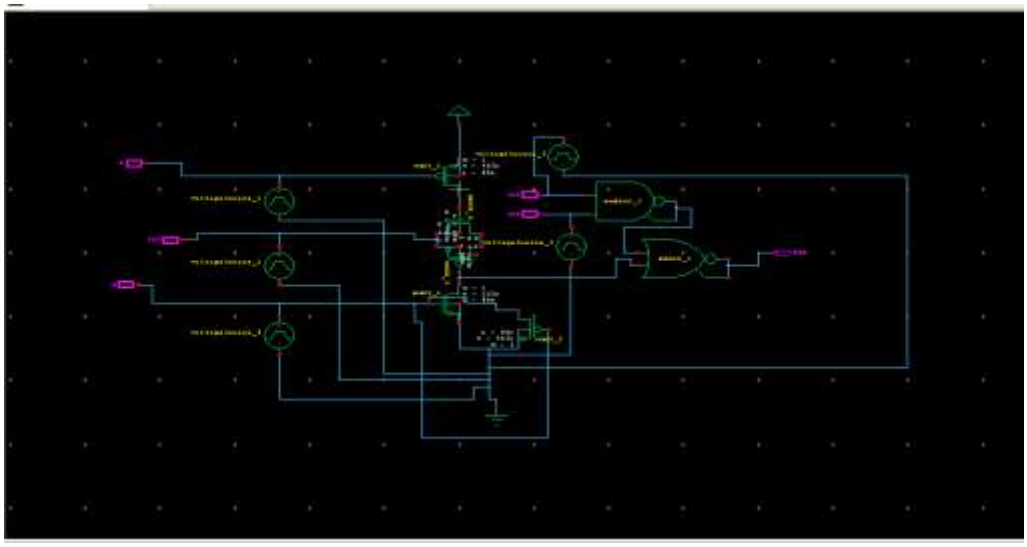

Figure 1: Optimized Circuit 1at 90nm

The transmission gate has a less area overhead as compared to other delay elements. The optimized circuit2 is shown in Fig. 2.Transmission gate used here in the proposed technique.

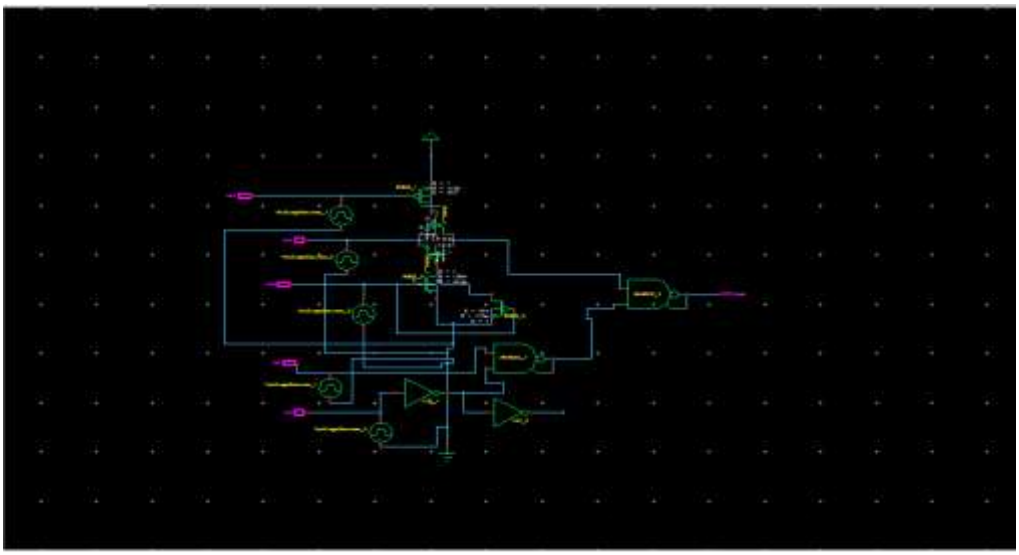

Figure 2: Optimized Circuit 2 At 90nm

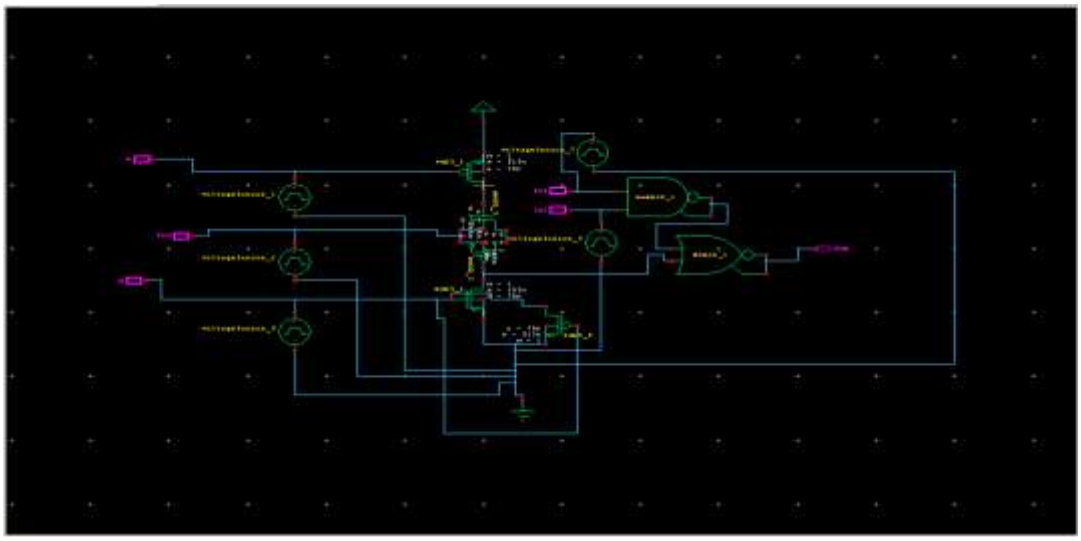

Figure 3: Optimized Circuit 1 At 70nm

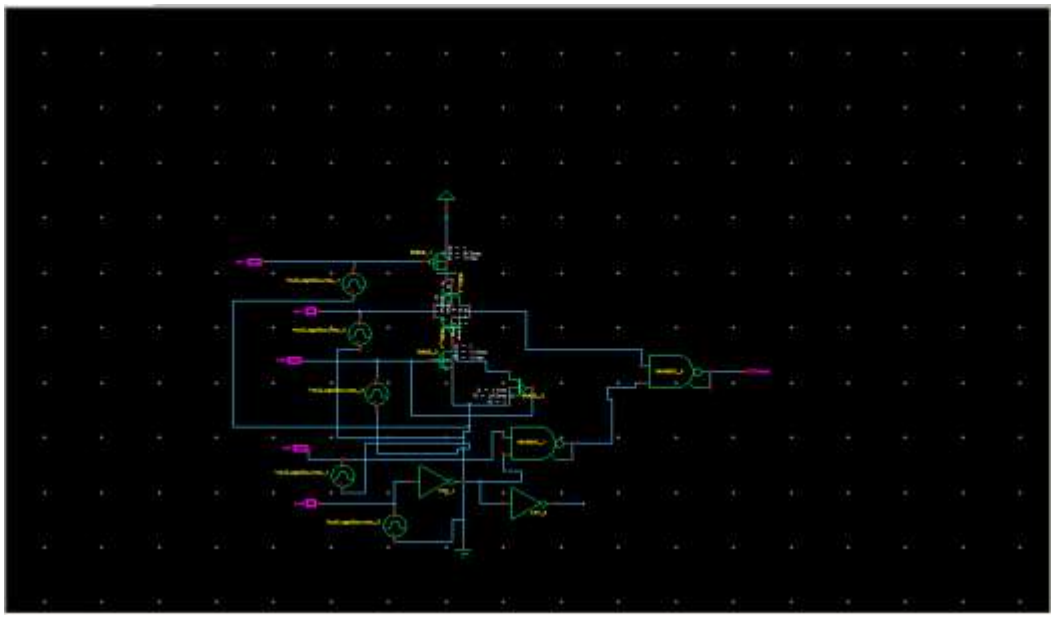

Figure 4: Optimized Circuit 2 At 70nm

III RESULT

The circuit design is carried out using 90 nm and 70nm optimized circuit1 and optimized circuit2 technology files. All the designs are done and simulation is performed in Tanner design environment. The total (average) power dissipation is measured using Tanner tools. The power and delay are measured.

The simulation of optimized circuit1 and optimized circuit2 is performed with 12 nanosecond period and variable pulse widths.

The average power dissipation during all operating modes is measured by using Tanner result browser and calculator. Table 1 and 2 compares the total power dissipation of all the optimized circuit1 and optimized circuit2 at 90 nm , 70nm technologies. In Table I Power of optimized circuit2 is reduced by comparison of

optimized circuit1.And its delay are reduce both comparison optimized circuit1 and optimized crcuit2 and in Table II Power of optimized circuit 2 is reduced by comparison of optimized circuit2 and its delay also reduce both comparison of optimized circuit1 and optimized circuit2.

Table I. Comparison Between Optimized Circuit 1 And Optimized Circuit2 (90nm)

Circuit/Parameter	Optimized Circuit1	Optimized Circuit2
Power	4.236934e+000watts	2.043141e+000watts
Delay	3.0102e-0009	1.0041e-007

Table II . Comparison Between Optimized Circuit 1 And Optimized Circuit2 (70nm)

Circuit/Parameter	Optimized Circuit1	Optimized Circuit2
Power	6.420379e+004watts	3.019895e+015watts
Delay	1.0339e-0007	0.0000e-0000

IV CONCLUSION

Scaling down of the technology has led to increase in leakage current. Nowadays, a leakage power has become more dominant as compared to Dynamic power.

Therefore, in this paper, the efficient technique has been proposed for reducing power and delay reduction in CMOS VLSI Circuits. The proposed method results in ultra low power consumption. Two optimized circuits are giving good results in terms of power and delay. The comparison is shown in Table I given below. The results are simulated using Tanner tool in 90nm technology at 5 volts in the circuits shown in Fig. 1-2.

Circuits shown in Fig.3-4 are simulated in Tanner tool for 70 nm. Comparison table given in Table II has shown above. The results are simulated using Tanner tool in 70nm technology at 5volts in the circuits shown in Fig. 3-4.

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