REDUCING PVT VARIATIONS USING ADAPTIVE BODY BIASING COMPENSATION TECHNIQUES

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ABSTRACT

Adaptive body bias is a valuable tool for overcoming systematic manufacturing variation, which is usually manifested in the product as leakage or timing variation between chips. FBB applied to a slow chip lowers the transistor threshold voltage and speeds up the chip. Conversely , RBB applied to a fast chip increases the transistor threshold voltage and reduces the excess leakage current of the chip. Here our design presented ensured to work under type process, temperature variation from 0^0C to 50^0C , core supply variation from 1.1to 1.2 & V_{DDE} variation from 3.0V to 3.6 V. other specifications are delay, frequency of operation,V_{1L}& V_{1H} levels.

Keywords: PVT Compensation, Adaptive Body Biasing.

I INTRODUCTION

With continued technology scaling, the sensitivity of circuits towards process ,voltage & temperature(PVT) variation is hampering circuit performance and yield. Process variations occur due to proximity effects in photolithography, non-uniform conditions during deposition etc. These cause fluctuations in parameters such as channel length, width and result in delay and leakage of the circuit. Also change in operating temperature occur due to power dissipation in the form of heat. An increase in operating temperature can cause on current to be decreased and hence as a result lowers the speed of the circuit. To reduce all these variations we can use Adaptive Body Biasing. ABB is a dynamically tool which is used to reduce leakage or timing variation between chips. ABB is of two type. Devices that are slow but do not leak too much can be forward body biased(FBB) to improve the speed, whereas devices that are fast and leaky can be reverse body biased(RBB) to meet the leakage budget.

II BODY EFFECT

Body effect refers to change in the transistor threshold voltage (V_T) resulting from a voltage difference between the transistor source & body. Because the voltage difference between the source & body affects the V_T,the body can be thought of as a second gate that helps to determine how the transistor turns on & off. The strength of the body

effect is usually quantified by the body efficient "gamma". Strong body effect enables a variety of effective body biasing techniques,& these techniques were used effectively in older process generations however , body effect has diminished with transistor scaling, & conventional deep-submicron transistors have very little body effect. For this reason body bias is not widely used for 65nm & smaller process technologies.

2.1 Body Biasing

Body bias involves connecting the transistor bodies to a bias network in the circuit layout rather than to power or ground. The body bias can be supplied from an external(off-chip) source or an internal(on-chip) source.

Reverse body bias, which involves applying a negative body-to-source voltage to an n-channel transistor,raises the threshold voltage and thereby makes the transistor both slower and less leaky. Forward body bias,on the other hand, lowers the threshold voltage by applying a positive body-to-source voltage to an n-channel transistor and thereby makes the transistor both faster and leakier. The polarities of the applied bias described above are the opposite for a P-channel transistor.

III BODY BIAS METHODOLOGIES

There are several body bias methodologies. A more advanced body bias methodology is to apply an Adaptive Body Bias.

3.1 Adaptive Body Biasing

Adaptive body bias is a valuable tool for overcoming systematic manufacturing variation, which is usually manifested in the product as leakage or timing variation between chips. For instance ,FBB applied to a slow chip lowers the transistor threshold voltage and speeds up the chip. Conversely , RBB applied to a fast chip increases the transistor threshold voltage and reduces the excess leakage current of the chip. The ability to tune as manufactured silicon back toward the electrical target with adaptive body biasing decreases the process technology's effective V_T variation and therefore improves the electrically-limited sort yield of the product.

IV DESIGN OPTIMIZATION

The designer has to ensure that the design is efficient as well as cost effective. The cost of production of a chip is much more expensive then to design. It is necessary to optimize area so that production in each batch increases thereby reduction in cost. Power consumption is also very important issue. There are some important parameters among which we have to compromise during the design: Area, power consumption, delay, speed, etc. Hence by taking care of all these parameters we have to provide an optimized design.

4.1 Decision of W/L Ratio

Area of a chip is basically determined by the (W/L) ratio of transistors. we have taken transistor model from the Linear Technology 130nm technology and then with suitable biasing simulated the ckt and plots are obtained. According to application specific, we will decide the lengths if there is the issue of leakage current then we have to choose the length according to the plot of leakage current wrt length.

4.2 Speeds versus Area Trade-Off

The speed of a circuitry is determined by the switching response of the circuit. The rise time and fall time of output determines how fast the circuit is operating. Faster the circuit lesser time it will take to settle. The basic cause of the rise time and fall time is the parasitic offered by the circuit.

4.3 Design and Optimization Techniques

The physical design is a design process which is an intermediate between circuit design and circuit on silicon. During the physical design we use different polygon layers which represent the different layers on the silicon. By using these layers a schematic is transformed into layout which is used later for mask preparation during fabrication process. So layout is a heart of all over the circuit design because it transfers the circuit into real world. After the layout design we check it for certain rules known as DRC (Design Rule Check) and LVS (Layout versus Schematic) check. When our layout passes both these checks then we extract net list from the layout. By simulating this post layout net list we verify our results, the dc results will remain same but there may be some changes in transient results due to the parasitic.

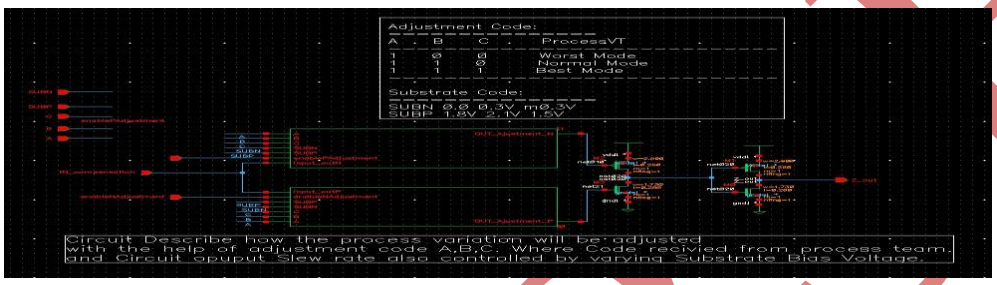
V RESULT AND ANALYSIS

Output Buffer output slope can be adjusted through compensation technique. Either by change in compensation codes or by adjusting proper substrate biasing voltage. Here in this project I am trying to adjust output slope which is affected by process variation through substrate biasing control mechanism. Adaptive biasing technique used to control the output slope of buffer. Using feedback signals from I/O PAD slew rate control is also achieved. LTSPICE simulation results are shown here.

Waveform	SUBP=1.8V	SUBP=2.1V	SUBP=1.5V
P Buffer-Rising Waveform	61.159ps	60.281ps	63.348ps
P Buffer-Falling Waveform	90.354ps	78.139ps	116.5ps

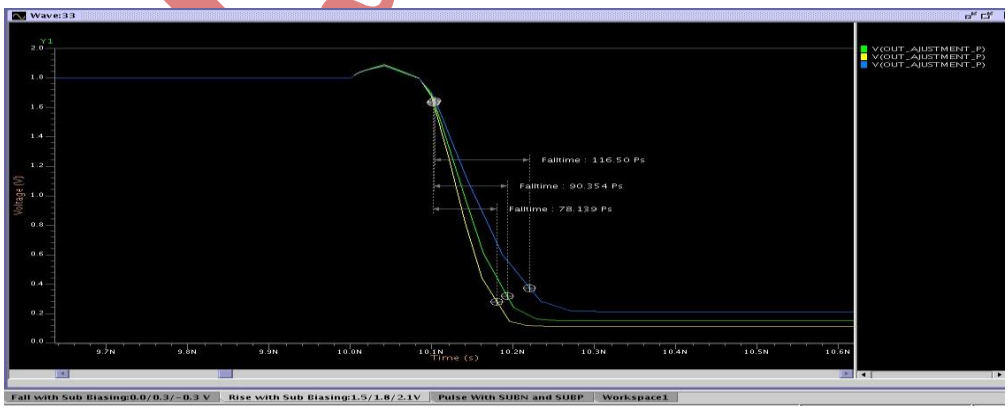
	SUBN=0.0	SUBN=0.3V	SUBN=-0.3V
N Buffer- Rising Waveform	406.7ps	388.06ps	416.79ps
N Buffer- Falling	34.236ps	32.779ps	39.042ps

5.1 Circuit Diagram of Pre-Buffer with Falling



5.2 Simulation Waveform of N Pre-buffer Fall

5.3 P Pre-buffer Fall



VI CONCLUSION

Due to change in Substrate Voltage Slope of the output Curve changes Increase in Substrate Bias Voltage Decrease in Rise (tr) and Fall (tf) time of output waveform

REFERENCES

[1] A.Amerasekeraand C.Durrury,ESD in Silicon Integrated Circuit ,John Wiley & Sons,1995.

[2] A.Amerasekeraet.,Al., "*ESD failure Modes : Characteristics Mechanism and Process Influences*" IEEE Trans. Electron Devices,Vol.39,No2,pp.430-436,feb1992.

[3] A.Amerasekera and C.Duvvury "*The Impact of technology scaling on ESD Robustness and Protection Circuit design,"* Proc.EOS/ESD Symp. 1994, pp 237-245.

[4] C.Duvvury and A.Amerasekera, "*ESD issued for advanced CMOS Technologies* ," Microelectronics Reliability,Vol36,No7,1996.

[5] Canh Q Tran,Hiroshi Kawaguchi and Takayasu Sakurai . "*Low Power High Speed Level Shifter design for Block-Level dynamic voltage scaling environment*," University of Tokyo.

[6] Craig Brunty and Laszlo Gal, "*Optimum Tapered Buffer*" IEEEJSSC Vol 27 Jan 1992.

[7] C.R. Parthasarthy, "*Investigation of Slew Rate Control in the buffersof HCMOSS I/O library,"* Library development group,Central R&D ,ST Microelectronics Gr.Noida.

[8] FeiYuan ,Ph.D,P.Engg, "*Simultaneous Switching Noise(SSN),"* Department of Electrical and computer Engg, RyersonUniversity,Toronto,Canada.

[9] Jose Rocha,MarcelinoSantos,J.MDores Costa and Floriberto Lima, "*High Voltage Tolerent Level Shifters and Logic Gates in standard low voltage CMOS Technology"* .

[10] J.S.Shor,Y.Afek and E.Engel, "*I/O buffer for high performance ,low power application* ," CICC,pp,595-598,May,1997.

[11] J.E.Vinson and J.J.Liou, "*Electrostatic discharge in semiconductor devices, protection technique*" Proceeding of IEEE,Vol 88,2000.