4th INTERNATIONAL CONFERENCE ON
Recent Trends in Engineering and Technology
Hirasugar Institute of Technology, Nidasoshi
ISBN: 978-93-48954-14-5
Date: 7th-8th March 2025

A Study, Analysis and Comparison of Gate Level Approximate Adders

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ABSTRACT

This paper presents study, analysis, and comparison of various Gate level AFAs reported in the state-of-the-art literature. The Gate-level AFAs (GAAs) are derived by approximating the gate-level schematic of EFA. To analyze and compare the efficacy of GAAs for image processing applications, the 'circuit design metrics' (CDMs), 'logic-gate complexity' (LGC), 'error metrics' (EMs), and 'image quality metrics' (IQMs), etc. have been extracted using a unique design methodology. All the design metrics under consideration have been extracted under common PVT conditions using Cadence EDA tools based on generic CMOS 180 nm technology.

Keywords— *Exact Full Adder, Approximate adder, Cost function, Circuit design metrics, Image quality metrics.*

I. INTRODUCTION

Most of the future generation electronic devices are essentially battery-operated "Internet-of-Things" (IoT) devices[1]. These IoT devices are computationally intensive and demands energy-efficient and high-speed Digital Signal Processing (DSP) architectures. The critical block in these architectures is Multiply-and-accumulate (MAC) unit. MAC operations are more expensive in terms of area, power, and cost. Hence it is very essential to trade-off among these design parameters while designing a DSP architecture for particular application[6-9]. Many low-power techniques have also been proposed in the state-of-the-art literature, to design energy-efficient DSP blocks. The approximate computing is one such technique that introduces the errors in the computation that are being approximated [17]. It can be considered as a most promising technique for various error-tolerant applications, such as multimedia signal processing, classification, pattern recognition, wireless communications, graphics, web search, machine learning algorithms etc. Due to limitations in human visual perception, the output quality of applications such as image, video, audio processing, etc. can tolerate some percentage of errors.[16,17,18].

Approximate computing can be applied to design approximate 1-bit full adders (FAs), derived based on the following design abstractions: gate level, logic equation level and transistor level. Gate-level(GL) approximation is one type of design abstraction used to approximate digital circuits for error-tolerant application, where the exact GL schematic is approximated to trade-off power, area, and speed[10-15].

II. EXISTING GATE LEVEL APPROXIMATE FULL ADDERS

In this section we present the study, analysis, and comparison of various existing GAAs in terms of design metrics. Gate-level(GL) approximation is one type of design abstraction used to approximate digital circuits for

error-tolerant application, where the exact GL schematic is approximated to trade-off power, area, and speed. Various GAAs that were reported in the literature are derived based on the approximation of GL schematic of an EFA shown in Fig. 1.a. The current literature survey reports various GAAs derived either by approximating EFA (Fig.1) or by proposing a novel GAAs using various combination of logic-gates. The schematics of GAAs that were reported in the literature [1-5] in the Fig.1b to f. And their corresponding truth-tables are shown in the Table I. In the Table I, the 'C' and 'S' stands for Cout and Sum outputs of an adder.

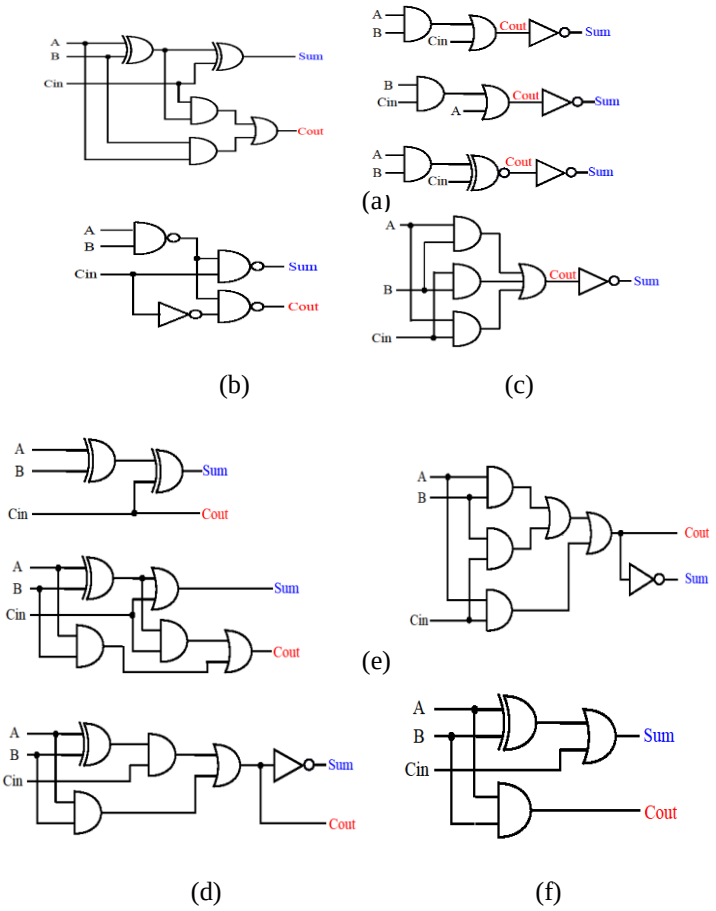


Fig 1: Logic diagram of Exact full adder and Approximate full adders

TABLE I: Truth Table Gate level Exact and AFAs

Inputs	EFA	NFAx	RAM1	RAM2	RAM3	RAM4	InXA1	InXA2	InXA3	JAA	SAA
ABCi	CS	CS	CS	CS	CS	CS	CS	CS	CS	CS	CS
000	00	01	01	01	01	01	00	01	01	01	00
001	01	10	10	01	10	01	11	01	01	01	01
010	01	01	01	01	01	01	01	01	01	01	01
011	10	10	10	10	10	10	10	11	10	10	01
100	01	01	01	10	01	01	01	01	01	01	01
101	10	10	10	10	10	10	10	11	10	10	01
110	10	11	10	10	10	10	00	10	10	10	10
111	11	11	10	10	01	10	11	10	10	10	11

ISBN: 978-93-48954-14-5

III. DESIGN, RESULTS, AND DISCUSSION

The schematics of various GAAs under consideration are designed, simulated, and verified using a 'semi-custom-design frame work' (SFW). All the GAAs are designed and simulated as per the SFW using Cadences' EDA tools. The functionality is verified using Spectre circuit simulator using generic 180 nm based nominal MOSFET models. CDMs of respective GAAs are extracted under common PVT conditions as per the simulation environment that have been tabulated in the Table II. Further, the computed EMs is tabulated in Table III.

TABLE II: Performance comparison of approximate FAs in terms of DMs

AFA	AP(µw)	WD(ps)	PDP(fJ)	EDP(fJ·ns)	GC
NFAx	7.631	100.3	0.7654	0.0768	4
RAM1	7.825	219	1.7137	0.3753	3
RAM2	4.901	222.1	1.0885	0.2418	3
RAM3	13.06	234.8	3.0665	0.72	3
RAM4	12.94	340.2	4.4002	1.4976	6
InXA1	11.35	194	2.2019	0.4272	2
InXA2	13.06	214.9	2.8066	0.6031	5
InXA3	10.44	253.7	2.6486	0.6719	5
JAA	12.98	340.2	4.4158	1.5023	6
SAA	8.509	237.2	2.0183	0.4787	3

The generic DMs used in the assessment of the circuit characteristics [12] are as follows:

Total Power: A total power dissipation (Ptotal) in any digital IC is due to the following three main components namely dynamic (Pdynamic), short circuit (Pshort circuit), and static (Pstatic) power dissipation. Thus the total power in terms of Watts(W) is expressed as

Ptotal = Pdynamic + Pshort−circuit + Pstatic

• Power-delay-product (PDP): It is defined as the product of power and delay.

P DP = P ower × Delay = α × CL × Vdd

• Energy-delay-product (EDP): It is defined as the product of energy and delay. It is measured in terms of Joules-second (Js) using the Eq. 1.6 EDP = AverageEnergy × Delay = α × CL × Vdd × 1 fclk

Average Power (AP):It is defined as the total power dissipated over a time period (T) and is given in the Eq. 1.7

AP = Ptotal × 1 T

• Worst-case delay (WD):It is defined as the maximum path delay from input to the output of a circuit.

• Gate Count (GC):It is defined as the number of gates conceived by a circuit.

To assess the the performance of AC circuits, many 'AC error-metrics' (AEMs) are proposed and discussed in the literature [10-12]. Most important and commonly used AEMs are:

• Error Distance (ED): The ED is defined as the arithmetic distance between the precise and imprecise outputs.

ED(p, q) = |p − q|.

• Sum of Absolute Error Distance (SAED):It is defined as the sum of total absolute ED

• Mean Error Distance (MED): It is an effective metric used to measure accuracy of multi-bit approximate circuits. It is also defined as an average value of ED and is given by.

MED = 1 2 2n 2 X2n i=1 |Edi

• Normalized Mean Error Distance (NMED): It is defined as the ratio of MED to maximum value (Pmax) that an exact design can have. And is expressed as:

NMED = MED pmax

Based on the various design metrics extracted from the respective tables: Table II and Table III, the following is the summary of important observations and inferences.

From the Table II, it is observed that the InXA1 is area efficient in terms of GC as compared to any other AFA under consideration, whereas the RAM4 and JAA are found to be having higher hardware cost.

Considering the Table II, it is observed that the NFAx is having lowest delay as compared to other adders and hence it is found to be more efficient, both in terms of energy (PDP) as well as delay (EDP). Whereas, the JAA is found to be having higher power dissipation, delay, PDP, and EDP. This is because, the RAM4 is having higher hardware cost and also having longer critical path.

From the Table III, it is observed that RAM4, InXA2, InXA3, JAA, and SAA are having lower MED and NMED, this is due to lower SAED. On the other side, the adders: RAM3 and InXA1 are found to be having higher MED and NMED, this is due to higher SAED.

TABLE III: Performance comparison of approximate FAs in terms of EMs

AFA	SAED	MED	NMED
NFAx	3	0.375	0.125
RAM1	3	0.375	0.125
RAM2	3	0.375	0.125
RAM3	4	0.5	0.166
RAM4	2	0.25	0.083
InXA1	4	0.5	0.166
InXA2	2	0.25	0.083
InXA3	2	0.25	0.083
JAA	2	0.25	0.083
SAA	2	0.25	0.083

IV APPLICATION OF APPROXIMATE GAAS

This section presents and discusses an application of GAAs for image processing applications. To study the efficacy of the GAAs, they are embedded in the Gaussian smoothing filter. The image sharpening of test image based on Gaussian smoothing are shown in Figure 2 and Figure 3 respectively. The Figure 2 b is the result of image sharpening using exact 8-bit adder. The Figure 3 is the result of image sharpening using HADD based on GAAs. To assess the efficacy of GAAs for image processing, we have measured their performance in terms PSNR and SSIM metrics. These metrics have been computed using MATLAB inbuilt functions ‘psnr’ and ‘ssim’ respectively. All the values of PSNR and SSIM that are extracted have been computed with reference to Figure 2 b. The extracted values of PSNR and SSIM are tabulated in the Table IV. From this table it is found that the SAA has the maximum PSNR=25.7366 dB and NFAx has the minimum PSNR=7.2861 dB. The SAA and RAM3 are having maximum (0.8225) and minimum (0.2815) SSIM values respectively.

(a) Cameraman (b) EFA

ISBN: 978-93-48954-14-5

(a) NFAx (b) RAM1 (c) RAM2

Figure 2: Image Sharpening of Cameraman using EFA

(d) RAM3 (e) RAM4 (f) InXA1

(g)InXA2 (h) InXA3 (i) JAA

(j) SAA

Fig 3: Image Sharpening using various GAAs

To better understand the efficacy of GAAs and provide more insight on their performance we define three Cost Functions (CFs) [18] listed in Eqn. 1-3, with respect to CDMs, EMs, and IQMs respectively. And the overall CF is computed as per the Eqn. 4 The computed CFs are shown in the Fig 4a to Fig 4d.

Cost function 1 (CF1) = EDP × Area (1)

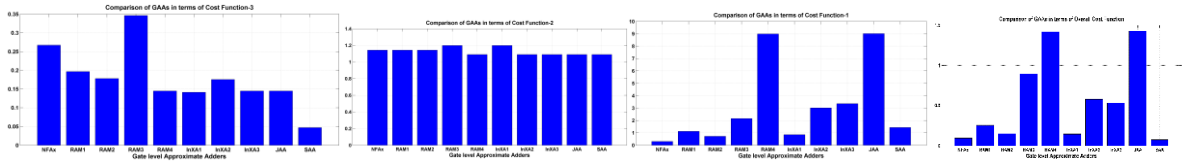
Cost function 2 (CF2) = 1/ (1 – NMED) (2)

Cost function 3 (CF3) = 1/(P SNR × SSIM) (3)

Overall Cost function (OCF) = CF1 × CF2 × CF3 (4)

TABLE IV: Performance comparison of approximate FAs in terms of IQMs

AFA	PSNR	SSIM
NFAx	7.2861	0.5141
RAM1	9.0824	0.5597
RAM2	12.3667	0.4546
RAM3	10.2654	0.2815
RAM4	12.3522	0.5587
InXA1	13.1304	0.5389
InXA2	11.5160	0.4947
InXA3	12.3522	0.5587
JAA	12.3522	0.5587
SAA	25.7366	0.8225



(a) CF1 (b) CF2 (c) CF3 (d) CF4

Fig 4 Comparison of Various GAAs in terms of Cost functions

From computed CFs the following are the important observations concluded

• The CF1 is defined as the product of EDP and area, the comparison of various GAAs in terms of CF1 is shown in Fig. 4a. From this figure it is found that the NFAx has the least cost function (CF). This lowest CF1 is due to least power dissipation and area.

• The CF2 is defined as the reciprocal of (1 − NMED), the comparison results of GAAs in terms of CF2 is shown in Fig. 4b. From this figure it is observed that the SAA is having the least cost function (CF). The lowest CF is mainly due to least SAED value conversely highest (1-NMED) value.

• The CF3 is defined as the as the reciprocal of the product of PSNR and SSIM, the comparison of various GAAs in terms of CF3 is shown in Fig. 4 c. From this figure it is observed that the SAA is having the least cost function (CF) value compared to other adders. This can be attributed to higher PSNR and SSIM values

• Finally, we define the overall CF shown in Eqn. 3.7d and corresponding results in Fig. 4 d. From this figure it is observed that the SAA is having the least overall CF as compared to any other adders.

V. CONCLUSION

In this paper, we have studied, analyzed, and compared the performance of various gate level approximate adders. All these adders have been designed using Cadence's EDA tools, simulated under common PVT conditions, and verified functionality as per their respective truth tables. Further, to assess their suitability for image processing applications, a comparison in terms of various cost functions has conducted. From this comparison, it is found that the SAA is found to be most efficient circuits under gate level approximate adder.

ACKNOWLEDGMENT

I extend my sincere thanks to my research supervisor Dr. Parameshwara M C, HOD, Dept. of ECE, Vemana

Institute of Technology for all his valuable guidance to excel in my research work. I express my sincere gratitude to Management, Veerasaiva Vidhyavardhaka Sangha, Ballari for moral support in pursuing my research work.

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