

Design of 6T Static SRAM computation and 8T SRAM computation for Bit line Leakage Compensation analysis

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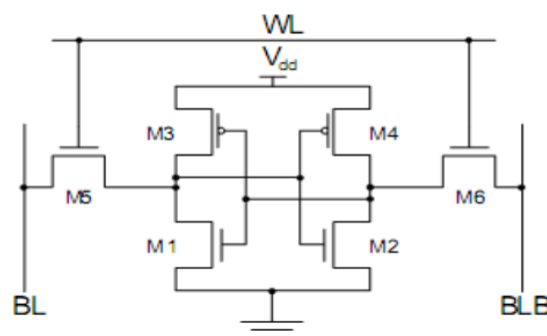
Abstract

The 6T SRAM design finds extensive application in modern integrated circuits and semiconductor systems due to its compactness, high speed, and low power consumption. It is commonly employed as cache memory in CPUs and other processing units due to its fast access times and high density, facilitating rapid data retrieval and storage. Register Files: 6T SRAM cells are often utilized in register files within processors to store frequently accessed data and operands, contributing to faster instruction execution. This study investigates the design of 6T Static Random Access Memory (SRAM) to address bit-line leakage in memory cells. Through detailed computational analysis and simulation, various strategies for bit-line leakage compensation are explored. The research focuses on optimizing the 6T SRAM architecture to mitigate leakage effects while maintaining data integrity and power efficiency. The findings offer valuable insights into effective techniques for enhancing SRAM performance in integrated circuits, crucial for achieving reliable and energy-efficient memory systems in modern semiconductor designs

INTRODUCTION

6T SRAM cell

A 6T SRAM is a static random access memory which is used for bistable latching circuitry by storing each bit is shown below. The term random access means in array of RAM, each one cell can be read and write in any order.

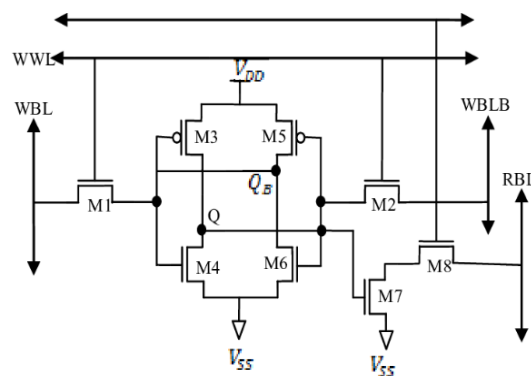


A 6T SRAM (Static Random-Access Memory) cell is a type of memory cell used in digital electronics to store data. The "6T" stands for six transistors, which are used to construct each cell.

The 6T SRAM cell consists of six transistors. Two NMOS transistors and two PMOS transistors. These form two cross-coupled inverters, creating a bistable circuit. The other two are used to control access to the cell during read and write operations.

As we know that we are dealing with the low power VLSI design, we are obviously bound to create and innovate those products which have high performance and low consumption. It has now become possible to reduce the complexity of internal hardware of products.

8T SRAM cell



Here we are using CMOS technology which is used for the above conventional 8T SRAM cell. This uses 6 transistors which are connected to two bit lines for the data access. Two bit lines are used for the data to be written to the SRAM cell and Transistors M7 and M8 are used for the data to be read from the cell. In above figure, WBL means write-bit-line which uses the transistors (M1, M2, M3, M4, M5, M6).

Data stability in the 8T SRAM cell is much enhanced as compare to 6T SRAM cell where RWL and WWL are used for read lines and write lines respectively. Isolation of the nodes is also kept on check while read operation is executed.

EXISTING SYSTEM

In the existing system, the 6T SRAM design is meticulously crafted with a focus on mitigating bit line leakage through comprehensive analysis of compensation mechanisms. Leveraging sophisticated computational modelling and simulation techniques, engineers delve into the intricate details of static SRAM architecture to optimize its performance under varying operational conditions. Central to this optimization is the measurement and evaluation of the SRAM's leakage performance, which serves as



a critical benchmark for assessing its reliability and efficiency. By systematically analysing the leakage characteristics and implementing effective compensation strategies, researchers aim to enhance the stability and energy efficiency of the SRAM design. This endeavour underscores the significance of meticulous evaluation and refinement in ensuring the robustness and efficacy of semiconductor memory systems in contemporary integrated circuits.

Drawbacks

- Dual-Split voltage analysis is made, frequency domain analysis is not made
- Only leakage is focused.

PROPOSED SYSTEM

This study presents a comparative analysis of 6T Static Random Access Memory (SRAM) and 8T SRAM designs, focusing on their efficacy in mitigating bit line leakage in memory cells. Through comprehensive computational modelling and simulation, the designs' performance is evaluated under varying operating conditions. The investigation delves into the intricacies of leakage compensation mechanisms, shedding light on the advantages and limitations of each architecture. Insights gleaned from this analysis offer valuable guidance for optimizing SRAM designs to enhance memory cell stability and energy efficiency in integrated circuits.

Advantages of proposed system

- Comparative study of 6T SRAM and 8T SRAM is developed here.
- Leakage compensation mechanisms, energy efficiency and memory cell stability are focused.

SOFTWARE SPECIFICATIONS

MICROWIND 3.1 VERSION

Microwind, a widely utilized Electronic Design Automation (EDA) tool, offers a plethora of benefits catering to the needs of semiconductor designers and researchers. This comprehensive software package provides a user-friendly environment for designing and simulating various digital and analog circuits at the transistor level. One of the primary advantages of MICROWIND lies in its intuitive graphical user interface, which enables users to create and manipulate circuit schematics with ease, facilitating rapid prototyping and experimentation. Additionally, MICROWIND offers a rich library of predefined components and modules, streamlining the design process and saving valuable time. Its simulation capabilities allow for thorough analysis of circuit behavior, including performance metrics such as timing, power consumption, and signal integrity. Moreover, MICROWIND's support for both CMOS and BiCMOS technologies makes it versatile and adaptable to a wide range of design requirements. Furthermore, the tool's integration with other industry-standard software packages enhances its utility,



enabling seamless exchange of design data and interoperability. Overall, MICROWIND stands as a valuable asset in the arsenal of semiconductor designers, offering efficiency, flexibility, and powerful simulation capabilities to expedite the development of cutting-edge integrated circuits and systems.

CONCLUSION

These above results suggest that managing split voltage analysis is harder and expensive in terms of bit line commands but if we manage to analyse on the basis of frequency domain then we have a better results in analysing the leakage characteristics and implementing effective compensation strategies. It also determines the leakage compensation analysis with memory cell stability and energy efficient methodologies to enhance the intricacy in the semi-structural designs. On the other hand we also come to know the bit by bit differences between 6T SRAM and 8T SRAM cells which is very important for future explorations and its worth it.

Designing a 6T SRAM cell using multiple voltage bit lines involves creating a memory cell that can operate with different voltage levels on the bit lines. The 6T SRAM cell is a basic building block of static random-access memory, and it consists of six transistors. To accommodate multiple voltage levels on the bit lines, you would need to design the cell to handle different voltage levels during read and write operations. Simulation of modified SRAM cell design under various conditions and verify its functionality and performance. Characterize the cell to ensure it meets the specifications for the multiple voltage levels. designing SRAM cells can be complex, and it often requires a thorough understanding of semiconductor device physics and circuit design. Additionally, ensure that the modified design complies with the technology and process parameters of the specific semiconductor technology you are working with. The presented approach developed with better understanding through RTL simulation as well as CMOS evaluation.

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