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IMPLEMENTATION OF CMOS OPERATIONAL AMPLIFIER

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ABSTRACT

Current trend in the design of many amplifier circuits, comparators, converter architectures, regulators and many more is towards low power operation and high operating speeds with optimized area. The unique behavior of the MOS transistors in sub- threshold region not only allows a designer to work at low input bias current but also at low voltage. This op-amp has very low standby power consumption with a high driving capability and operates at low voltage so that the circuit operates at low power. The usage of low power devices are increasing at an unprecedented rate because of the emerging applications in system on chip devices such as cellular mobile phones, microcontrollers used in internet of devices and many other biomedical applications. CMOS technology is the most predominant technology for the design of op-amp based circuits and these op-amp circuits are ubiquitous and found everywhere in the design of analog integrated circuits. In this work, a 2-stage CMOS operational amplifier is designed, simulated and analyzed for different specifications. Lower V_{DD} values entail small input voltage ranges and hence the circuit becomes more susceptible to noise due to various design methods associated with the circuit. In this paper a CMOS two-stage operational amplifier is designed using hands approach, simulated and the important specifications are analyzed. The op-amp is designed for a given set of standard specifications and simulated using CMOS 180nm technology at V_{DD} of 1.8V DC. After analysis of the simulated waveforms, the important parameters such as Phase margin, slew rate, gain, and CMRR are calculated.

Keywords: *Analog signal, digital signal, magnitude response, transconductance, bandwidth and low power.*

INTRODUCTION

Currently VLSI (Very Large Scale Integration) with SoC (System on Chip) technology has made various subsystem components partitioned at digital-analog boundaries to get integrated into a single chip. It offers many advantages and very few disadvantages. But still CMOS technology is the better choice for Mixed signal circuit design (circuits with both analog and digital circuitry on the same

silicon substrate), since it offers good power reserves on the digital circuit design side, offers more complex circuit design and also enough combination of various time dependent circuits.

The operational amplifier is undoubtedly one of the most useful devices in analog electronic circuitry. Op-amps are built with vastly different levels of complexity to be used to realize functions ranging from a simple dc bias generation to high speed amplifications or filtering. With only a handful of external components, it can perform a wide variety of analog signal processing tasks. Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices. Operational Amplifiers, more commonly known as Op-amps, are among the most widely used building blocks in Analog Electronic Circuits. Op-amps are used equally in both analog and digital circuits. The CMOS Op-Amp (Operational amplifier) is the important building block both in the design of mixed signal circuits and analog integrated circuit design. Operational amplifiers are linear circuit operated devices which performs a wide variety of signal processing operations such as low frequency amplification, carrying out mathematical operations such as addition, subtraction, multiplication, log and antilog functions, differentiation, integration, performing low frequency filtering, high pass filtering, band-pass filtering, and band reject filtering functions, clipping and clamping functions, precise rectification of signals, selective signal inversion circuit, V-I and I-V converters, buffers, high speed comparator circuits, voltage follower circuit, different waveform generators, and zero crossing detector circuits. Various functions are realized using operational amplifiers designed with diverse levels of circuit complexity. The main advantage of operational amplifiers over the discrete components is that they offer better AC and DC characteristics. By connecting less number of passive components external to the operational amplifier, it is able to perform wide variety of operations as specified above in this section. Several works have been discussed in the literature regarding the design and simulation of CMOS operational amplifier with better performance characteristics.

LITERATURE REVIEW

S.C.D. Cruz et al. designed a programmable system that operates the op-amp tunable for the parameters such as slew rate, magnitude, phase margin and compensating capacitor. This programmable system is operated with digital input data and engaged on op-amp topologies specifically the CMOS two-stage miller compensated op-amp and folded cascode op-amp and implemented in digital CMOS 0.090µm process [1]. Various CMOS amplifiers and its effects on offset voltages and currents, power supply rejection ratio, transient response, stability issues, common mode rejection ratio, voltage gain, input and output impedances, unity gain bandwidth and power dissipation are analyzed in detail in [2]. A six CMOS operational amplifier implemented in 250nm process technology with rail-to-rail output voltage is described in [3]. This paper illustrated the rail-to-

rail stage variations on the input common mode voltage range. Chow et al. proposed a one voltage rail to rail amplifier, which uses current driven bulk method for decreasing threshold voltages to reduce orthodox hysteresis problem. The one volt amplifier has been designed to realize as a low pass filter and the simulated results were observed and the gain was found to be 71dB and CMRR of 100dB [4].The design and simulation of a two-stage CMOS op-amp using a null resistance, miller capacitance and a CG circuit is presented in [5]. The designed circuit has been simulated in HPSICE and it shows high unity gain bandwidth(UGB), high CMRR and high slew rate values for high speed applications. Parthipan et al. proposed a high performance CMOS operational amplifier designed and simulated in 0.09µm process technology. The operational amplifier includes a low current buffer block to trade off low power to achieve less propagation delay (ns) [6]. The design and simulation of a fully-differential mode folded cascade mode op-amp containing fully-differential enhancing amplifiers is described in [7]. A common mode feedback circuit realized using switched capacitor logic simulated in 250nm demonstrating a gain of 81dB with 0.68GHz unity gain bandwidth and power dissipation of 30mW is presented in this work. Y. Guo et al. described a novel technique of resizing CMOS amplifiers which is carried out by matching the quiescent currents and small-signal AC conductances [8]. The circuit simulation is performed at 180nm CMOS technology and simulated results show that the amplifier shows elevated performance with respect to area/size of the circuit and operating speed. LAYGEN-II, an enhanced layout generation tool is proposed in [9], whereby the circuit designer specifies the process technology, resizing aspect ratios and layout template consisting of technological specifications. Anisheh.S.M. et al. presented the simulations of a fully-differential CMOS two-stage op-amp circuit, that offers high DC gain values without altering the low power consumption, rail-to-rail output swing voltages, input offset voltages and currents, CMRR, PSRR, unity gain bandwidth values and input referred noise voltages [10]. Xin. Y et al. proposed a high output current CMOS two-stage amplifier circuit comprising of first stage as recycled folded cascode amplifier circuit and second stage as tail current transistor [11]. The circuit is simulated in 180nm CMOS process technology and achieves high values of phase margin and unity gain bandwidth. A wideband operational amplifier simulated with a unity gain bandwidth of 30GHz is presented in [12]. The quiescent currents are modified to achieve the optimized performance parameters. A high speed op-amp for use as comparator circuit is used in [13]. The resolution of the circuit was designed at 4-bits.For most general applications of an opamp a negative feedback is used to control the large voltage gain. The negative feedback also largely determines the magnitude of its output (”closed- loop”) voltage gain in numerous amplifier applications, or the transfer function required. The op-amp acts as a comparator when used without negative feedback, and even in certain applications with positive feedback for regeneration. An ideal Opamp is characterized by a very high input impedance (ideally infinite) and low output impedance at the output terminal(s) (ideally zero).to put it simply the op- amp

is one type of differential amplifier. This section briefly discusses the basic concept of op-amp. An amplifier with the general characteristics of very high voltage gain, very high input resistance, and very low output resistance generally is referred to as an op-amp. Most analog applications use an Op-Amp that has some amount of negative feedback. The Negative feedback is used to tell the Op-Amp how much to amplify a signal. And since op-amps are so extensively used to implement a feedback system, the required precision of the closed loop circuit determines the open loop gain of the system.

Op-amps are linear devices which has nearly all the properties required for not only ideal DC amplification but is used extensively for signal conditioning, filtering and for performing mathematical operations such as addition, subtraction, integration, differentiation etc . Generally an Operational Amplifiers a 3-terminal device. It consists mainly of an Inverting input denoted by a negative sign, (”-”) and the other a Non-inverting input denoted by a positive sign (”+”) in the symbol for op-amp. Both these inputs are very high impedance. The output signal of an Operational Amplifier is the magnified difference between the two input signals or in other words the amplified differential input. Generally the input stage of an Operational Amplifier is often a differential amplifier.

EXISTING METHOD

Op-Amps are electronic circuits that provide controlled gain characteristics, large bandwidth, high input impedance, and higher values of slew rate and low output impedance values. It is the vital circuit in all the electronic gadgets used in our day to day activities. Fig. 1 shows a typical diagram of a two-stage op-amp without buffer circuit [14]. The initial input stage of the op-amp is the differential transconductance stage that forms the input and provides the differential to single ended conversion along with gain. It also improves noise and offset performance. This first stage is connected to the next stage namely another gain stage consisting of a common source stage to provide additional amplification of the signal. This stage is further followed by an output buffer (not shown in Fig.1) circuit, in case the op-amp circuit is supposed to drive a pure large capacitive load such as those used in switched capacitor applications. Suppose if the op-amp circuit needs to drive a low-impedance loads, then the gain stage should be followed by a buffer stage. Using a buffer circuit in the output stage increases the output voltage swing and also minimizes output impedance. In this existing system, the operational amplifier generates unwanted oscillations and exhibits poor stability.

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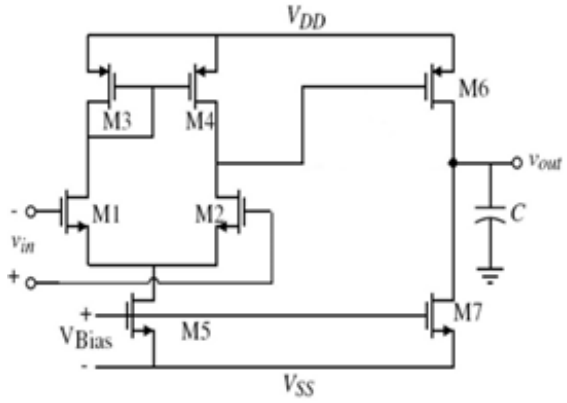

Fig 1: Two Stage operational Amplifier

PROPOSED METHOD

In order to avoid the unnecessary oscillations and increase the stability of the operation, Miller compensation technique is used. This technique increases the stability, phase margin, DC gain, CMRR, improves bandwidth and PSRR of the operational amplifier. In this we add a compensation capacitor in the feedback fashion. A compensating capacitor (C_c) is connected from the output of the second stage to the input of the second stage to reduce the gain at large frequencies. This capacitor is essential, as the output voltage tends to oscillate at higher frequencies and hence stability of the op-amp circuit is reduced.

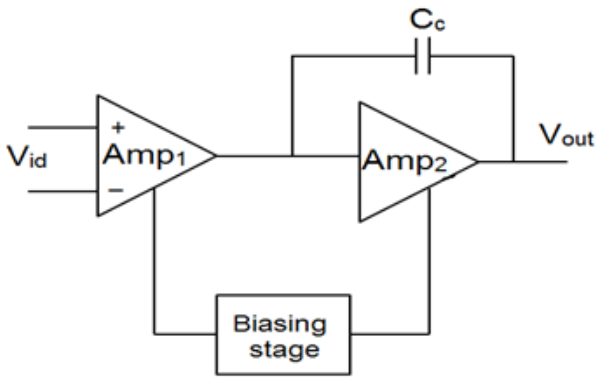

Fig. 2: An op-amp stage indicating different stages

The capacitor Cc also tends to improve the Phase margin of the circuit, which is very vital in the closed-loop circuit operation. The biasing circuit stage provides the necessary currents and voltages i.e. proper quiescent point for each and every stage in the op-amp circuit to operate in Saturation and triode regions.

This two-stage op-amp comprises of a series connection of voltage to current convert circuit and current to voltage converter circuit. The design of a CMOS op-amp starts with the selection of proper structure. In the next step, quiescent voltages, current and sizing of each transistor is carried out. Lastly the value of compensating capacitor is calculated. A typical CMOS op-amp can be carried out

using the following steps: (i) Choosing suitable configuration for a given particular application. (ii) Finding the type of compensation circuitry needed to suit the assumed specification at the start of the design. (iii) Hand calculations are performed to find out the device sizes for AC, DC, transient responses, temperature sweep and optimization is carried out using any available computer simulation tools.

Table 1: Design Specifications

S.No.	Name of the specification	Assumed value
1	V_{DD}	+1.8V
2	Gain	75 decibels
3	Settling Time	≤ 1μs
4	Slew Rate	≥ 60V/μs
5	Common Mode Rejection Ratio (CMRR)	≥ 70decibels
6	Phase Margin	≥ 60 degrees
7	Output Swing	≥ ±1.5V
8	Gain Bandwidth product	≥ 100Mega Hz
9	Power Dissipation	≤ 1mW
10	Input Common Mode Range (ICMR)	(-1.5V to 2.5V)
11	Power Supply Rejection Ratio (PSRR)	≥70dB
12	Operating Temperature	(0-100)°C
13	Offset voltage	≤ ±10mV
14	Technology	180nm CMOS

SIMULATION RESULTS

The simulation results of the proposed circuit design are presented in this section. The presented CMOS op-amp circuit has been simulated using Cadence Virtuoso tool in 0.180μm technology.

The design has been carried out, supposing that all the MOS transistors are operating in saturation region. Operating point analysis is carried out and various node voltages and currents through the transistor have been calculated. For carrying out the frequency response analysis (both magnitude and phase responses) a 0.1mV input signal is applied at the input side. The magnitude plot and phase plot versus frequency is plotted and presented in Fig. 4. From the simulated graphs, the values obtained are Gain=77dB, Phase margin=65°, and a Gain bandwidth product of 108MHz.

The designed CMOS op-amp circuit is simulated using Cadence Virtuoso in 180nm technology and the simulated circuit is presented in Fig. 3.

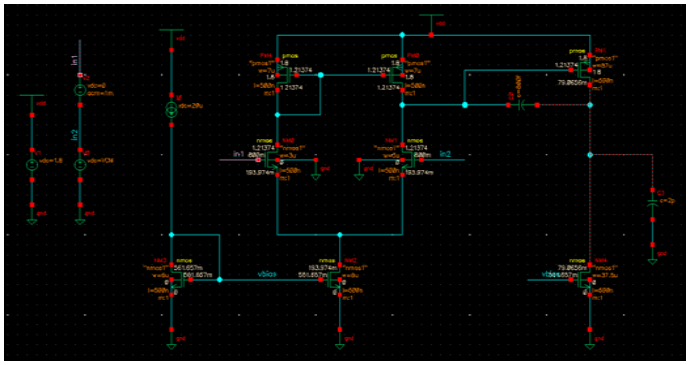

Fig. 3: Simulated CMOS op-amp

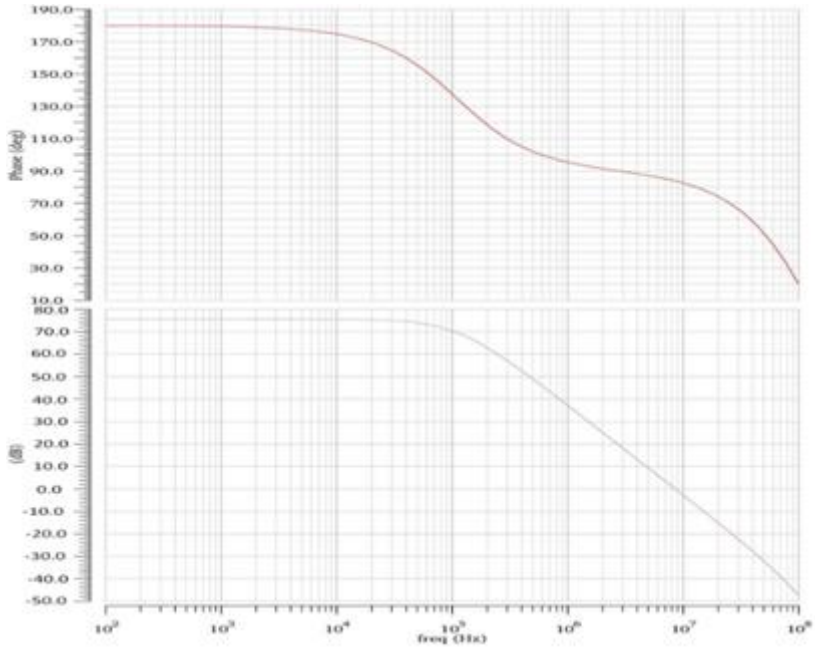

Fig. 4: Simulated AC response of the amplifier

Connect a pulse input to the inverting input terminal of 5µs pulse width and time-period of 10µs. Using transient response analysis the simulated graph is shown in Fig. 5.

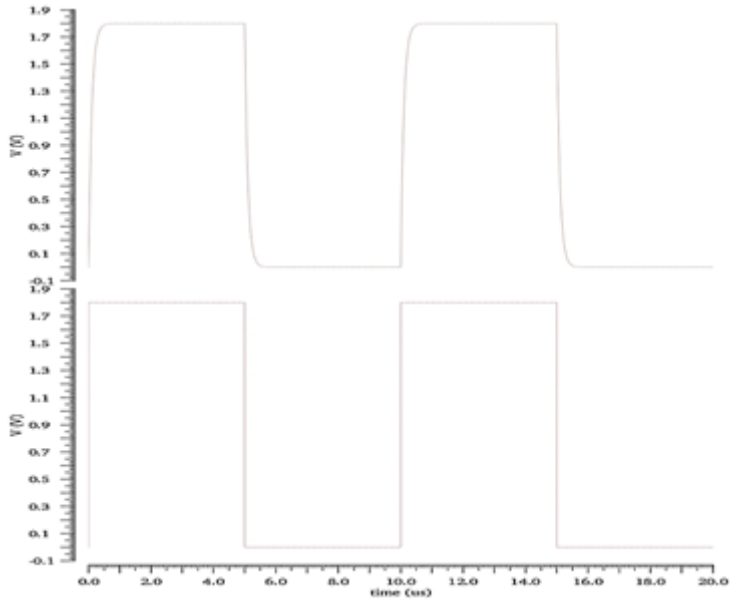

Fig. 5: Transient response calculations

The simulated transient response for sinusoidal input waveform is presented in Fig.6

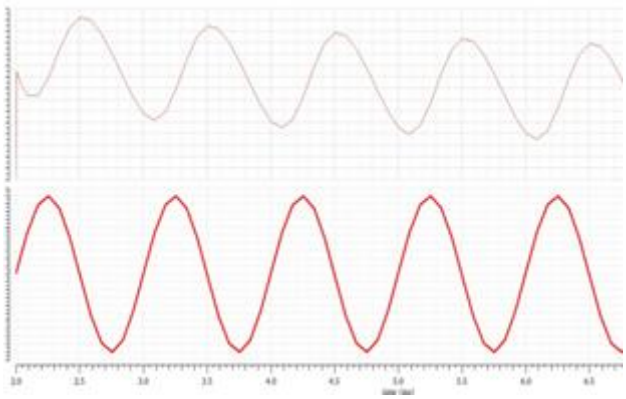

Fig. 6: Transient response graph

Fig. 7 presents the noise analysis response for various frequencies.

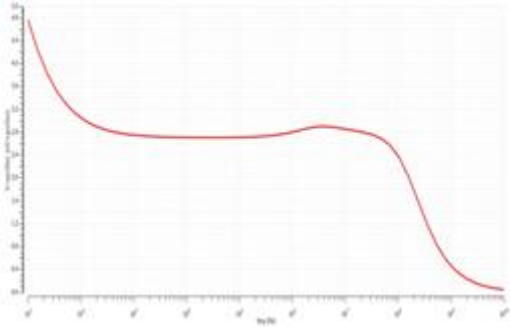

Fig. 7: Noise analysis graph

Table-II presents the simulated values of the CMOS op-amp.

Table II: Simulated values of op-amp design

S.No.	Name of the specification	Assumed value
1	Gain	77 decibels
2	Settling Time	0.38μs
3	Slew Rate	55.8V/μs
4	Common Mode Rejection Ratio (CMRR)	66 decibels
5	Phase Margin	78 degrees
6	Output Swing	±1.7V
7	Gain Bandwidth product	90Mega Hz
8	Power Dissipation	0.76mW
9	Power Supply Rejection Ratio (PSRR)	63dB

CONCLUSION

The presented work related to the design aspects, simulation and analysis of two-stage CMOS operational amplifier is carried out in 180nm CMOS technology and has been optimized for certain important specifications such as gain, high linearity, bandwidth, slew rate, settling time and area. The circuit uses a compensating capacitor due to which stability of the op-amp increased to a large extent. From the obtained values, as the value of compensating capacitor decreases, the gain bandwidth product increases for a particular process. All the transistors were made to operate in the saturation region. After analysis and comparison, it was found that there was a slight difference in the hand calculations and simulated results. Still if any further increase in gain is required, it can be accommodated by adding another common source stage with appropriate biasing circuit. By using a double-ended output at the output side, voltage swing can be enhanced. Also by increasing the bias currents of the CMOS stages, the unity gain bandwidth can be still increased to a bigger magnitude.

FUTURE SCOPE

By using a double-ended output at the output side, voltage swing can be enhanced. Also by increasing the bias currents of the CMOS stages, the unity gain bandwidth can be still increased to a bigger magnitude.

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