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Performance Analysis of Low Power Digital Circuit

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ABSTRACT

In this paper we studied and analyzed the performance analysis of low power XOR and XNOR circuit using GDI (Gate Diffusion Input) technique at 16nm and 22nm technology. Basically, in this paper reduced power dissipation and delay of XOR and XNOR circuit using GDI technique have been evaluated by using SPICE (Simulation Program with Integrated Circuit Emphasis) tool. The performance of the GDI-XOR and GDI-XNOR circuit is compared to other circuits. The simulation results GDI-XOR circuit becomes better performance in terms of power and delay at 16nm technology.

Keywords- Gate Diffusion Input technique; delay; power dissipation; XOR and XNOR gates

INTRODUCTION

With rapid development of portable digital applications, the users demand high speed performance, small in size, reduce heating problem, minimum components are used in fabrication, longer battery life and reduce power dissipation in the VLSI circuit design [9]. The various digital circuits likes as an adder, substractor, multipliers, multiplexer, code converters, parity checkers and error correcting, XOR and XNOR gates. In this paper studied and analyzed XOR and XNOR gates and reduced power dissipation and delay of XOR and XNOR circuit using GDI technique at 16nm and 22nm technology have been evaluated by using SPICE (Simulation Program with Integrated Circuit Emphasis) tool. In the last few decades, a number of digital circuits have been proposed by various researches in order to achieve improved performance of the XOR and XNOR gates [8]. **Hernandez and Aranda** implemented an XOR and XNOR circuit by using double pass transistor logic (DPL).In this circuit two inverters with two pMOS and nMOS pass transistors are used then overcome large power dissipation problem and produced a weak output voltage for all input values [6]. **Ajay kumar Dadoria, Manit Bhopal, India, Kavita Khare, R.P. Singh implemented** low power high speed 11T full adder using Deep Sub-micron (DSM) technology. Optimization of speed, power and area can be achieved by using GDI technique. To reduce the power consumption different logic design techniques like CMOS complementary logic, Dynamic logic, Pseduo nMOS, CMOS Domino logic, Cascade voltage switch logic (PTL) have been proposed [3]. **Omnia Al. Badry, M.A. Abdelghany** implemented low power 1-bit full adder using full swing

GDI technique to reduce power consumption, delay and area and achieve full swing output [1]. **Hamed Naseri and Somayeh Timarchi** proposed low power and fast full adder by exploring new XOR and XNOR gates and reduce power dissipation and delay due to low output capacitance and low short circuit power dissipation. Also proposed six new hybrid 1 bit full adder circuit based on the novel full swing XOR and XNOR gates [4]. Each of the proposed circuits has output in terms of speed, power consumption, power-delay product (PDP) , driving ability and so on**. Pankaj Kumar, Poonam Yadav** implemented design and analysis of GDI based full added circuit for low power applications. Here we introduced a 11T GDI based full added circuit that used for low power applications. Simulations are based on BPTM model at 180nm ,90nm ,65nm technology by using Tanner EDA tool [2].

GDI CELL OVERVIEW

The circuit diagram of convential GDI cell is shown in fig.1 was proposed bu Morgenshtein [7]. It is observed that the GDI cell has only two transistors i.e one nMOS and one pMOS that makes a CMOS inverter and also nMOS and pMOS transistor are connected to a common point then whole circuit build GDI cell. GDI is a new technique for low power design and reduced the number of transistors in logic design which affects the size of the devices [7]. This technique reduces power consumption, propagation delay and area of the digital circuits [7]. GDI cell consists of three terminals- G (common gate input of nMOS and pMOS) and P (input to the source/drain of pMOS) and N (input to the source/drain of nMOS) [7]. Both nMOS and pMOS transistors are connected to N and P respectively [7].The main difference between the CMOS and GDI based on the design, in GDI cell pMOS is not connected to VDD and nMOS is not connected to GND as compared to CMOS while in CMOS circuit pMOS is directly connected to VDD and nMOS is directly connected to GND [2]. GDI cell design is more flexible than CMOS design [2]. Table 1 shows that the different boolean functions implemented by GDI logic based on different input value [2].

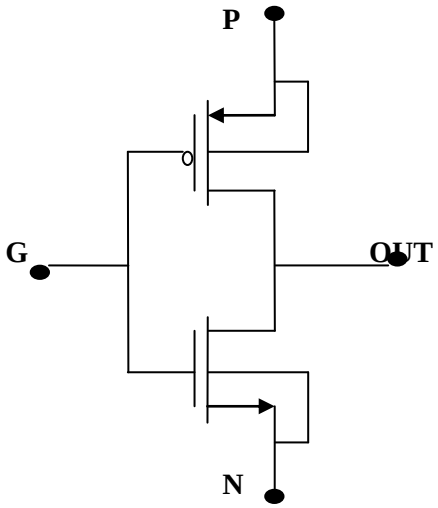

Fig.1 GDI Cell

G	P	N	OUTPUT	FUNCTION
A	'1'	B	A'+B	F1
A	B	'0'	A'B	F2
A	'1'	'0'	A'	NOT
A	B	'1'	A+B	OR
A	'0'	B	AB	AND
A	B	C	A'B+AC	MUX

Table1. different Boolean functions implemented by GDI logic

SIMULATION AND PERFORMANCE ANALYSIS OF GDI XOR AND XNOR CIRCUIT

The GDI cell based XOR and XNOR gates are important digital gates to design of any digital circuit. Fig.2 and fig.3 shows that the GDI based XOR and XNOR circuit [5]. Both circuits i.e GDI XOR and GDI XNOR circuit requires only four transistors. Fig.4 and fig.5 is the transient behaviour of the GDI XOR and XNOR circuit. These circuits are designed at 16nm and 22nm technology, from the fig.4 and fig.5 observed that the output voltage swing of both circuits is weaker. Therefore an inverter circuit and GDI XOR and GDI XNOR circuit are connected in cascade and hence to obtain full output voltage swing. Table 2 shows that the power and delay comparison of the designed GDI XOR and GDI XNOR circuit with some previous literature report [6].

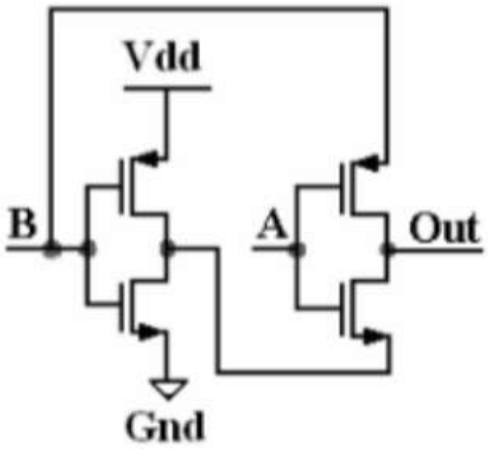

Fig.2 GDI XOR gate circuit

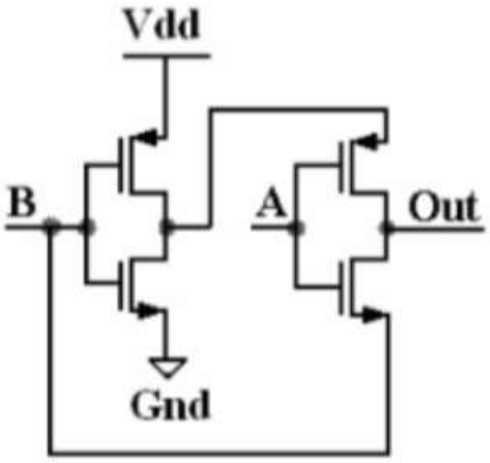

fig.3 GDI XNOR gate circuit

Table 2.Power and delay comparison of the designed GDI XOR and GDI XNOR circuit with some previous literature report.

Circuit Type	CMOS Technology (nm)	Transistor Count	Delay (ps)	Average Power (µW)
CMOS-XOR	45	12	23.2	0.54
Morgenshtein's XOR [7] [10]	45	8	22.0	0.40
Morgenshtein'sXOR[10] [11]	45	9	20.2	0.38
Soba's XOR [10]	45	6	7.5	0.28
Uma's XOR [8]	45	8	21.1	0.39
GDI-CI XOR	22	6	8.28	5.71
GDI-CI XNOR	22	6	8.59	1.93
GDI-CI XOR	16	6	6.89	9.67
GDI-CI XNOR	16	6	5.62	5.34

In table 2 we observed that the circuit proposed by CMOS-XOR, Morgenshtein's XOR [7] [10], Morgenshtein's XOR [10] [11], Soba's XOR [10] and Uma's XOR [10] [8] at 45nm technology hence founded more delay and less average power while XOR and XNOR gates designed by using GDI technique at 16nm and 22 nm technology then found very less delay and very less power as compare to 45 nm technology. The delay of the 16nm GDI-XNOR circuit is found to be 2.66ps, 2.97ps and 1.27ps faster than that of the GDI-CI XOR, GDI-CI XNOR and GDI-CI XOR circuit respectively [6]. However the power dissipation in GDI-XNOR circuit is low in compare to other circuits [6]. The power of the 16nm GDI-XNOR circuit is found to be 3.78µW, 7.74µW and 3.4µW less than that of the GDI-CI XOR, GDI-CI XOR and GDI-CI XNOR circuit respectively [6].Finally we observed that the GDI XNOR circuits at 16nm technology has better performance as compare to other circuits.

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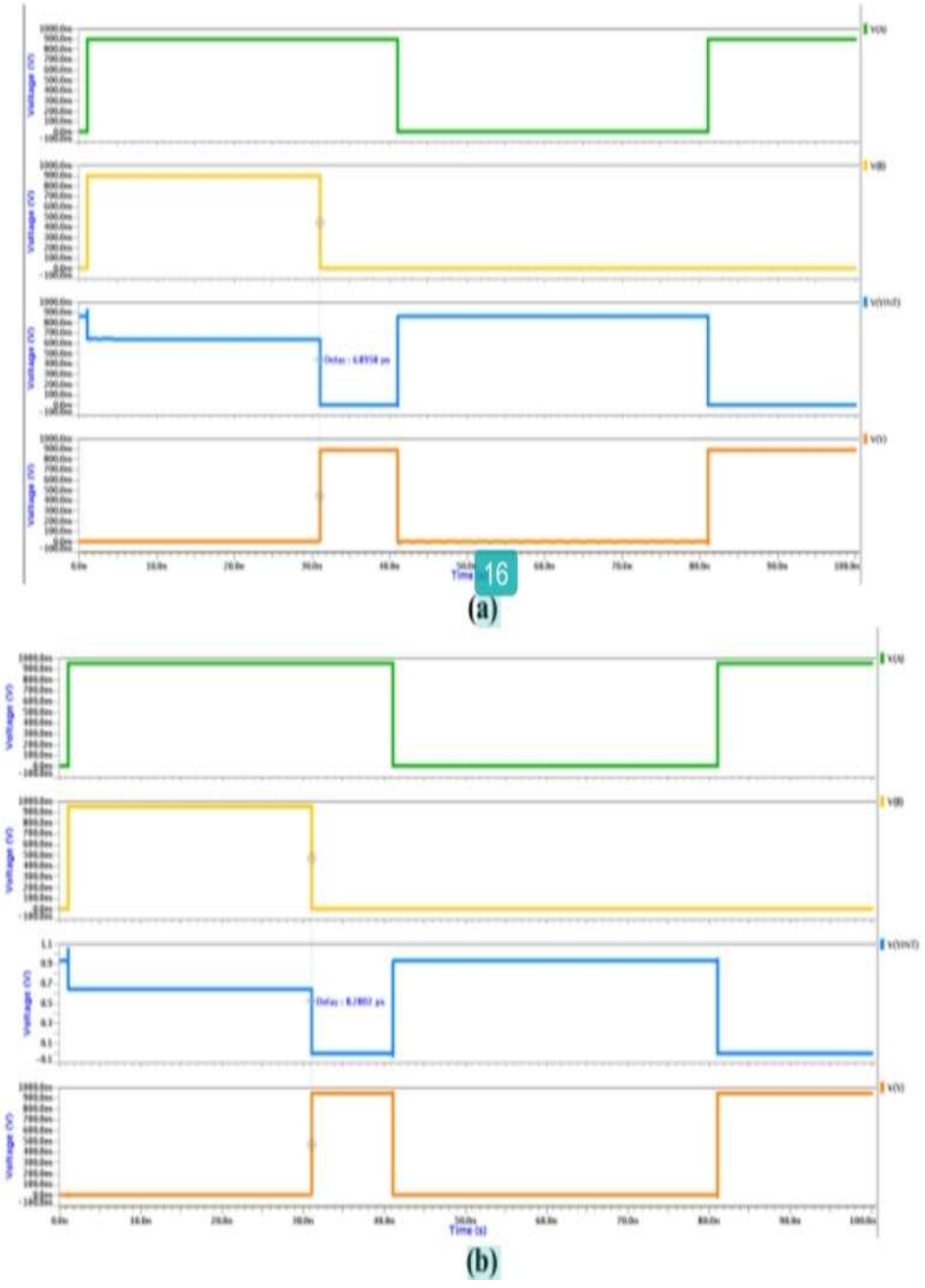

Fig.4 Transient behaviour of the GDI XOR at (a) 16nm and (b) 22nm

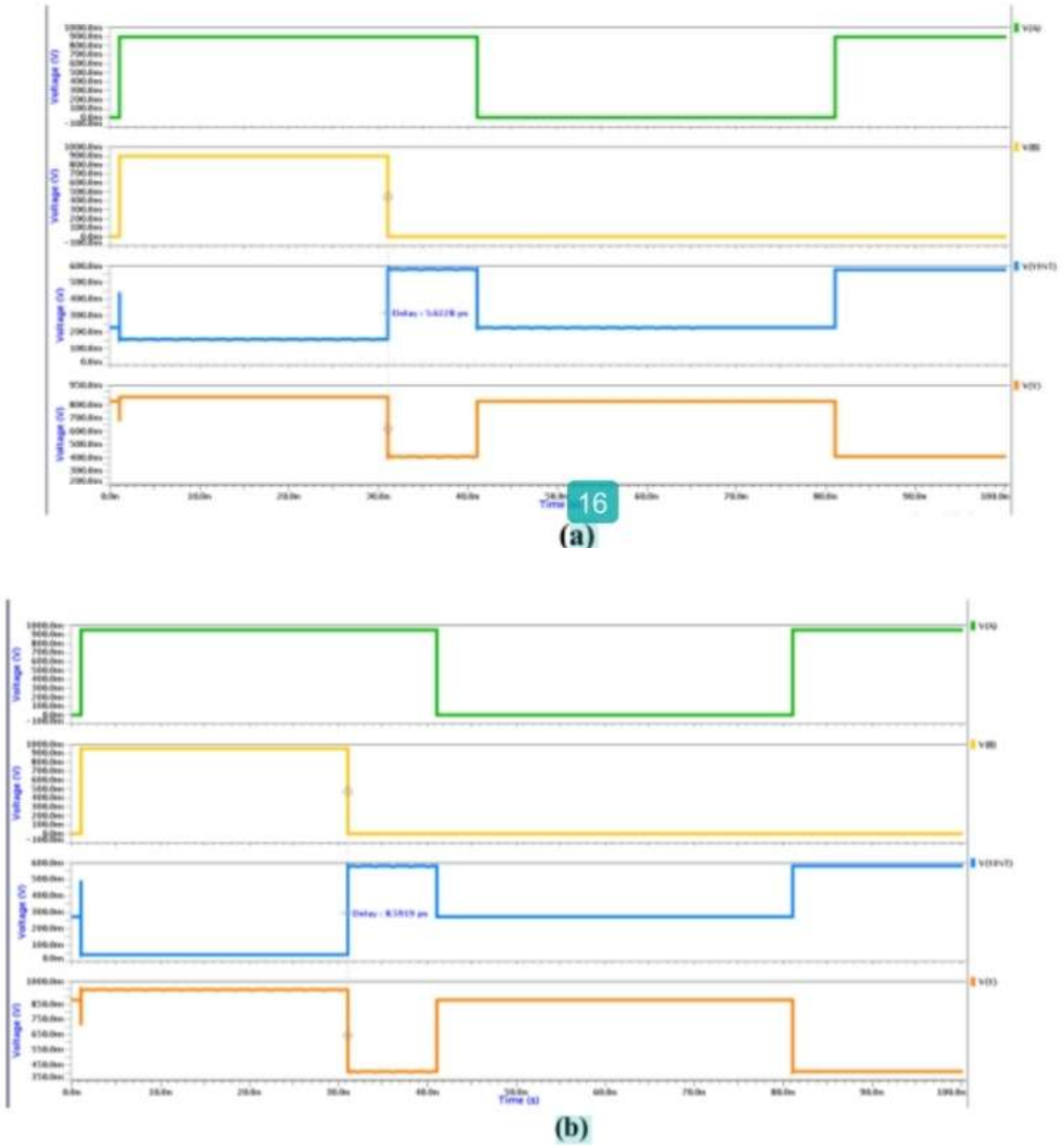

Fig.5 Transient behaviour of the GDI XNOR at (a) 16nm and (b) 22nm

CONCLUSION

In this paper we studied and analyzed the performance of GDI XOR and GDI XNOR circuit. Design the GDI based XOR and XNOR circuit at 16nm and 22nm technology. Only four transistors used in both circuits [7]. GID technique used to reduced power dissipation and delay of any digital circuit [7]. After evaluated, comparison the performance of GDI XOR and GDI XNOR circuit to other circuits in terms of delay and power then found better power and delay [6]. The simulation result has better performance of GDI XNOR circuit at 16nm technology [6]. The delay of the 16nm GDI-XNOR circuit is found to be 2.66ps, 2.97ps and 1.27ps faster

than that of the GDI-CI XOR, GDI-CI XNOR and GDI-CI XOR circuit respectively [6]. However the power dissipation in GDI-XNOR circuit is low in compare to other circuits [6]. The power of the 16nm GDI-XNOR circuit is found to be 3.78µW, 7.74µW and 3.4µW less than that of the GDI-CI XOR, GDI-CI XOR and GDI-CI XNOR circuit respectively [6]. Finally, GDI-CI XNOR circuit has better performance as comparison to other circuits and can be improved output voltage swing [6].

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