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Low Power design of Memory Intensive Functions

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Abstract

This paper demonstrate technique to optimize power consumption of memory intensive application. A design example -a video, vector quantizer encoder - demonstrates how optimization at the algorithms, architecture and circuit level can reduce power consumption by reducing both the effective switched capacitance and the required speed of the system's memory.

I. INTRODUCTION

Generally, the two most significant standards utilized for estimating the presentation of a circuit have been speed and area. However, power consumption is an increasingly significant cost measure in VLSI architecture because of both increased transistor density and the emergence of portable electronics. While a great deal of work has been put in lately for computer-intensive applications of low power technologies, the effects large memory accesses have on power usage and strategies to reduce this power efficiently are frequently disregarded. Picture and video coding however form part of the sharing of knowledge. Increasingly, the number of computer systems with multimedia display and video data storage capability. Since the fundamental aspects of this architecture are reducing the power consumption[1], the development of low-power image and video encoding / decoding schemes is highly important in conjunction with the tremendous popularity of portable computers and phones.

A description of the methods used inother memory-intensive applications, is discussed here. The results are given in this article. A video vector image is quantified by splitting it into blocks of pixels mapped to a codebook of likely vectors with the aid of a mean squared error to calculate distortion[2]. This VQ was built for the Info-Pad Terminal that uses 256 vectors as a compact battery-operated codebook [3]. A 4x4 pixel vector has to be compressed every 11.48psec to process 30 frames / sec.

The paper is organized in the following manner. Section 2 and 3 give a diagram of low-power plan and vector quantization individually. Section 4 investigates the various degrees of intensity advancement design. Section 5 and 6 gives the consequences of various usage zeroing in on structural advancements.

II. BACKGROUND

Several scientists' handheld device resource consumption habits. However, their findings are not necessarily in line and often contradictory because they have researched different platforms. The backlight of the monitor, disc and processor dominates the energy usage of the average laptop computer [4]. Havinga et al. concluded that the network interface at least absorbs equivalent energy (i.e. Newton PDA) as the device [5]. When a computer collects network updates and when 'down' it raises significantly its energy consumption. Felter et al. have found that in recent years there have been an improvement in the contribution of the CPU and memory to power consumption[6]. Laptops use various strategies to minimise energy consumption, mostly by shutting them off or reducing the frequency of the clock after a time of non-use. Any researchers suggested that a flash RAM would replace the hard disc. Notice that the trade between use of energy and efficiency is inherent, because low power technology has drawbacks. For example , reducing the CPU frequency will increase response time and spin down the disc contributes to a high latency of subsequent disc access.

a) Properties of low power design

We discuss 'power utilization' and how to minimise it in this article. And if they can't say this directly, most designers are obsessed with reducing energy consumption. This is because batteries have a limited energy supply (in comparison to power, but batteries often limit peak electricity consumption). Energy is the fundamental component of power's time; if energy usage is constant, it actually increases the energy usage by the time it is expended. Lowering energy consumption just saves energy if not so much time to carry out the mission. The power usage of the static CMOS circuit is determined by a dynamic portion power accomplished by equation 1, which does not include short circuit current.

$$P = C_{sw} V^2 f \qquad (1)$$

where C_{sw} is the successful capacitance exchanged per clock cycle, V is the flexibly voltage, and f is the clock frequency. It has been demonstrated that the best method to decrease power utilization is to lessen the gracefully voltage bringing about a quadratic decrease in power. Clock recurrence may likewise be diminished by the legal utilization of equal or pipelined structures. Equal designs and devoted equipment can likewise be utilized to diminish the successful exchanging capacitance[7].

III. VECTOR QUANTIZATION

A Vector Quantization(VQ) approach is used in voice and video systems for compression of data. The hardware implementation for real-time video decompression on a portable computer is introduced in [8] of a very low-energy decoder based on vector quantification. A second video de-compression method with low power, based on the quantization of subband coefficients by

pyramid vectors, is defined here [9]. Vector quantification is an efficient technique of image coding that achieves lower rates of bit, i.e., below 1 bit per pixel. Equation 2 is defined as vector quantization

$$Q:R^k \rightarrow C \; C=\{y_1, y_2, \cdots, y_N\}$$

$$y_i \in R^k \quad \forall i=1,2,\cdots,N$$

$$y_i = Q(x) \quad if \; d(x,y_i) \leq d(x,y_j)$$

$$\text{for } i, j=1,2,\cdots,N \qquad (2)$$

where x is a k-dimensional info vector having a place with the k dimensional space R^k; C is the codebook of N k-dimensional words y_i, and d is the bending basis utilized. In vector quantization, a vector, which is a square of pixels, is approximated by a delegate vector (codeword) of the codebook, which limits the mutilation among all the codevectors in the codebook. Pressure is accomplished by communicating or putting away the codeword address (record) rather than the codeword itself.

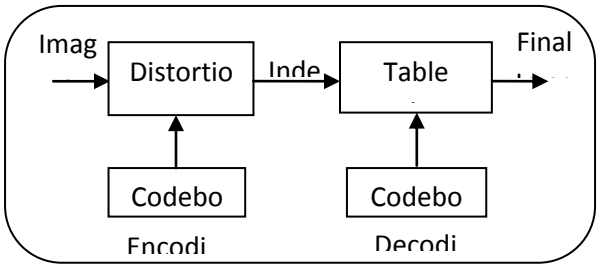

Figure. 1. Coding and Decoding in Vector Quantization.

Expecting a codebook of N words (actualized on-chip) and a vector measurement k (measurement of picture blocks and codewords), the computational unpredictability of the coding of a picture block as indicated by (1) is given as equation 3,

Coding Complexity

$= kN$ Memory Accesses

$+ N$ Distortion Criterion Executions

$+ N - 1$ Comparisons

$+ log_2 N$ Output Operations: (3)

The $log_2 N$ yield tasks compare to the pieces needed to represent to the index of the chose codeword, which is at long last sent off-chip. The computational intricacy of the translating of a picture block is a lot of lower. The translating of a picture block requires basic substitution of the

picture block by the chose codeword (the one that best approximates the square) in the yield picture. The computational intricacy of the interpreting of a picture block is given as condition 4,

Interpreting Complexity = k Memory Accesses + log2 N Input Operations: (4)

The input operations of the $log_2 N$ match the bits of the codeword 's chosen index transmitted from the encoding portion and transmitted from the chip to the decoder's lookup table. Figure 1 demonstrates the configuration of the code and encoding for vector quantization. The asymmetric design of vector quantization-namely coding and decoding-renders vector quantization desirable for low energy applications; in particular, the fact that decoding is far easier. This is because the decoder is typically the mobile component of the device, where the problem of power usage is more important in compact environments.

The key drawback associated with power of classic complete search vector quantization is the memory-based coding and decoding. That is a drawback since the codebook is stored in a large , high power consuming background memory [10]. The emphasis of this approach is the development of a strong, vector-based method for the quantification and decoding of images and videos. The fundamental principle is to substitute arithmetic machines for memory entry. Limited codebooks can be used during codecoding (real codebooks). The codewords will be transformed, so small real codebooks will be expanded to larger virtual codebooks. In contrast to traditional vector quantization, the memory requirements of the proposed device (number of memory accesses, size of the codebook, capacity switched by access) have been reduced which contributes to substantial power consumption reductions.

a) Distortion Measure:

The normal calculation of distortion for VQ is Mean Squared Error $MSE = \sum (C_i - X_i)^2$, whereby C is the codebook, X is the original vector representation for 4x4, and I is the index of the pixel term. An alternative indicator of distortion, Absolute Error $AE = \sum |C_i - X_i|$ gains from fewer computations at the potential cost of a less precise image reproduction [11]. Video accuracy is a subjective discipline, such that creators are expected to determine what is 'precise enough.' For example, if a designer determines that power saved overrides picture considerations, the designer may select AE over MSE to save multiplication operations. The norm, MSE, was selected in this study. Using AE instead will minimise computing resources and accentuate more the benefits of savings in memory resources.

b) Full Search Vector Quantization (FSVQ):

The best way to filter the codebook is conceivably to do everything conceivable. The 4x4 vector and each codevector are contrasted. The vector that gives the smallest twist is chosen to code the image. The key drawback of FSVQ is that the planning needed to pack any vector is normally enormous. This is expensive in the field and the use of power [12]. In order to satisfy continual

constraints, the severe FSVQ measurement includes a widened chip zone as well as a lower clock recurrence and versatile strain. Moreover, according to the necessary measurement measure the traded potential per vector is relatively high.

Tree Search Vector Quantizer (TSVQ) encodingl51 needs way less computation. TSVQ performs a binary search, rather than a full search, of the vector house. As a result, the procedure complexness is proportional to log_2N,rather than N, wherever N is that the range of vectors within the codebook.

c) Tree Search Vector Quantization (TSVQ):

Figure 2diagrams the structure of the tree search. At every level of the tree, the input vector is compared with 2 codebook entries. If for instance at level one, the input vector is nearer to the left entry, then the correct portion of the tree is not compared below level two and an index bit zero is transmitted. This method is continual till a leaf of the tree is reached. Here solely $2*10g_2256 = 16$ distortion comparisons have to be compelled to be created, compared to 256 distortion calculations within the FSVQ [13]. There are several different vector quantization choices that will be explored, like a cropped Tree Search Vector Quantizer (PTSVQ), that has the advantage of requiring fewer memory accesses. an alternative choice, with adaptive codebooks for larger accuracy, are often employed in each FSVQ and TSVQ[S].

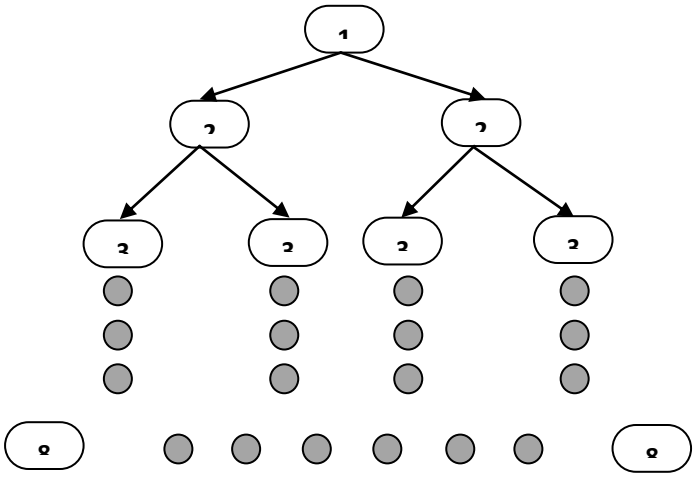

Figure 2. Tree Search Encoding

IV. DESIGN APPROACH

The key profound power outcome is generally high-level recursive choices, but optimization at the gate level is also significant. Memory power is diminished frequently for memory-dominant purposes, at the cost of marginally higher computing power. Video images are vector measurements by splitting them in pixel blocks (vectors), which are mapped on a codebook of

likely vectors with a mean square error due to distortions[14]. The VQ has been developed with the InfoPad handheld battery terminal that uses a 256-vector coding book [15]. A 4x4 pixel vector should be compressed each 11.48 psec in order to process 30 frames per second.

a)Algorithm

Potentially lower energy saves power by the reduction of the turned energy and essential path, and a lower voltages and frequency sanction. The computational complexity of 3 quantum methods is seen in table 1. Full codebook scanning requires an extensive study which can be substantially decreased with just a limited price precision by the use of a binary tree search (TSVQ). Sometimes the combined terms of the differential scan a priori decrease the quantity of calculations additionally. In equation 6, the differential scan of tree was used for both implementations,

$$MSE = \sum_{i=0}^{15} (C_i - X_i)^2 \qquad \begin{matrix} C_i - Code\,vector \\ X_i - Input\,vector \end{matrix}$$

$$MSE_{ab} = \sum_{i=0}^{15} (C_{ai} - X_i)^2 - \sum_{i=0}^{15} (C_{bi} - X_i)^2$$

$$MSE_{ab} = \sum_{i=0}^{15} C_{ai}{}^2 - 2X_i C_{ai} + X_i{}^2 - (C_{bi}{}^2 - 2X_i C_{bi} + X_i{}^2)$$

$$MSE_{ab} = \underbrace{\sum_{i=0}^{15} (C_{ai}{}^2 - C_{bi}{}^2)}_{Calculated\ a\ priori} + \sum_{i=0}^{15} X_i 2 \underbrace{(C_{bi} - C_{ai})^2}_{Calculated\ a\ priori} \qquad (6)$$

Table 1. Computational Complexity

Algorithms	Memory Access	Multiplication	Add / Sub tract
Full Search	4078	4078	8417
Tree Search	262	258	497
Diff. Tree Search	129	122	127

b) Architecture:

One way is to multiplex time, as Figure 3 indicates, through a centralized memory, process feature and power. It includes 18 cycles, which takes 146 vector clock cycles at a frequency of 8,3MHz, to process a tree node. One strategy used commonly for low-power models is parallel reading of bytes of words to reduce the output limit to decrease clock speed and voltage [Z]. The pace demands in TSVQ are not constrained by this architecture, provided that the direction of the vector to be selected depends on the results of the previous tree node. However, this architecture

(Figure 4) decreases the space switched by reducing the number of data accesses. Table2 demonstrates energy efficiency for parallel access for varying byte sizes and memory. Each tree level has special codevectors at the TSVQ level only. The memory can then be separated into distinct memories for individual tree levels.

The same processing elements and controllers are correlated with any memory. The critical path can be significantly shortened as this architecture can be pipelined in Figure 4, thereby reducing the clock frequency by 8 and the delivery voltage from 1.8 V through 0.7 V.

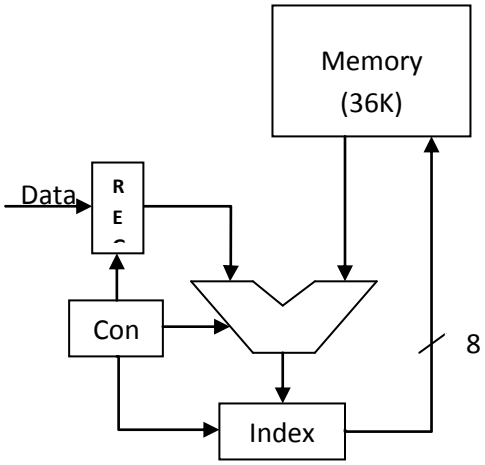

Figure 3. Centralized memory

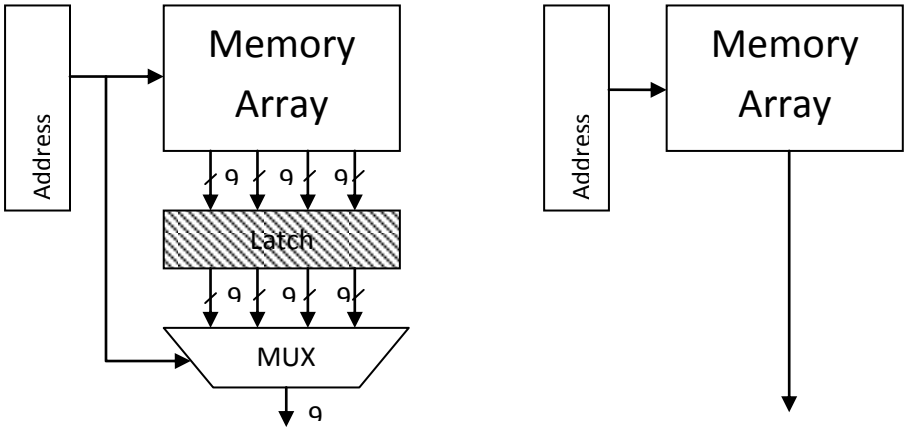

Figure 4. Parallel vs. serial memory

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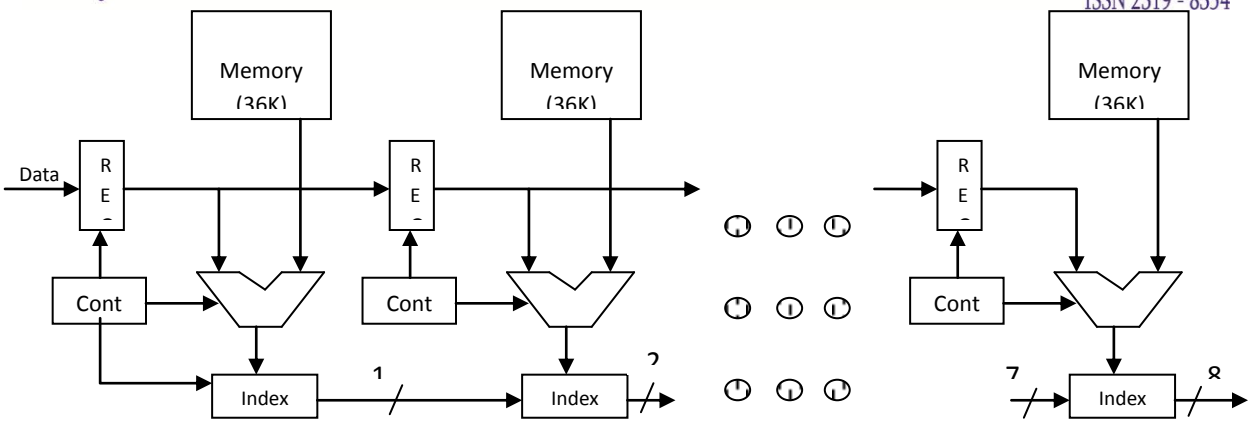

Figure 5. Distribute Memory

The transmitting memory architecture changes considerably less capacity than the clustered case in reading its co-devectors as less overhead is seen in Figure 5. While 8 controls and 8 processors are currently in operation on the chip, they are clocked at a frequency 8 so the energy is not modified by a vector. Interblock power is insignificant since the clocking frequency is eighteen times higher.

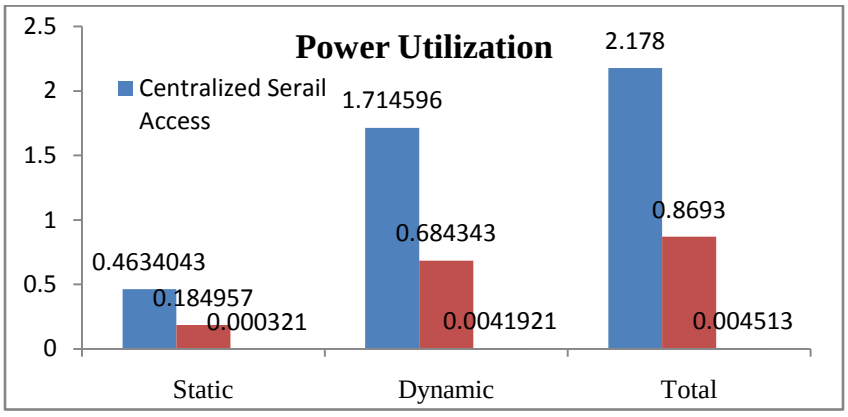

Figure 6. Power utilization Summary

Table 2. Simulation Results

Memory Control	Power (mW)			Area (μm^2)	Delay (pS)
	Static	Dynamic	Total		
Centralized Serial Access	0.4634043	1.714596	2.178	38.173	27.381
Centralized	0.184957	0.684343	0.8693	17.496	16.1872
Distributed	0.000321	0.0041921	0.004513	9.357	11.8743

c) Circuit:

The UC Berkeley cell library, with minimum transistor sizes to decrease parasite performance, was used to build all circuits. Registers with gated clocks retain extra inputs in idle clock periods to minimize their transfer operation. In order to minimizeobserve power, a single clock is used and registers are implemented using a minimal size of the TSPCR. Memory is implemented by using a low-powered SRAM on-chip with NMOSthreshold voltage underneath the power supply.

V. RESULT AND DISCUSSION

Three architectures were introduced to explain the multi-level approach to power reductions: one serial memory access and one-level and distributive TSVQ memory encoders with parallel memory access. The full research was not full at this time, so that all numbers come from detailed simulations carried out with 180 nm GPDK technology by CADENCE Genus. Table 2 summarizes the power and area numbers. Changing the core architecture with parallel memory access decreased the switching power by 73.80%. The capacitance is further reduced by memory partitioning, along with the critical path. A proper choice of algorithm and architecture is necessary to reduce the strength of memory-intensive functions. Decisions at the algorithmic stages have shown that computer complexity is decreased and a factor of 30 memory accesses decreased. Another 23.74-fold decrease in power was seen in Figure 6 by architectural optimizations.

V. CONCLUSION

A new framework was developed for low-power image coding and decoding. It is based on vector quantification and reduces energy consumption by using limited size and memory codebooks. Using quick codeword transformations. In this way, codebooks are generalized computer-based, and instead of memory-based, the coding process. A multi-level strategy is important to achieve major reduction in memory intensive tasks. Usually, a proper algorithm and design collection were the most fundamental force. It has been shown that algorithmic decisions decrease computational complexity dramatically and minimize the amount of memory accesses by a factor of 30 for the TSVQ. Additional power decrease was seen by architectural benchmarks by a factor of 23.74, mainly by a two-factor reduction of the memory percentage and by a reduction of the critical path, which allowed for a low voltage.

REFERENCES

[1] Havinga, P. J., & Smit, G. J. (2000). Design techniques for low-power systems. Journal of Systems Architecture, 46(1), 1-21.
[2] Chang, S., & Carin, L. (2006). A modified SPIHT algorithm for image coding with a joint MSE& classification distortion measure.IEEE transactions on image processing, 15(3), 713-725.

[3] Masselos, K., Stouraitis, T., &Goutis, C. E. (1998). Novel scheme for low-power classified vector quantisation image coding. IEE Proceedings-Vision, Image and Signal Processing, 145(6), 408-414.
[4] Mahesri, A., &Vardhan, V. (2004, December). Power consumption breakdown on a modern laptop.In International Workshop on Power-Aware Computer Systems (pp. 165-180).Springer, Berlin, Heidelberg.
[5]Havinga, P. J., &Smit, G. J. (2001). Energy-efficient wireless networking for multimedia applications.Wireless communications and mobile computing, 1(2), 165-184.
[6] Felter, W., Rajamani, K., Keller, T., &Rusu, C. (2005, June). A performance-conserving approach for reducing peak power consumption in server systems.In Proceedings of the 19th annual international conference on Supercomputing (pp. 293-302).
[7] Asanovic, K., Bodik, R., Catanzaro, B. C., Gebis, J. J., Husbands, P., Keutzer, K., ...&Yelick, K. A. (2006). The landscape of parallel computing research: A view from berkeley.
[8] Akter, M., Reaz, M. B. I., Mohd-Yasin, F., &Choong, F. (2008). Hardware implementations of an image compressor for mobile communications.Journal of Communications Technology and Electronics, 53(8), 899-910.
[9] Ahmad, I., He, Y., &Liou, M. L. (2002). Video compression with parallel processing.Parallel Computing, 28(7-8), 1039-1078.
[10] Awad, A., Manadhata, P., Haber, S., Solihin, Y., & Horne, W. (2016). Silent shredder: Zero-cost shredding for secure non-volatile main memory controllers. ACM SIGPLAN Notices, 51(4), 263-276.
[11] Chatterjee, S., &Sreenivas, T. V. (2008). Predicting VQ performance bound for LSF coding. IEEE Signal Processing Letters, 15, 166-169.
[12] Chang, C. C., & Wu, W. C. (2007). Fast planar-oriented ripple search algorithm for hyperspace VQ codebook. IEEE Transactions on Image Processing, 16(6), 1538-1547.
[13] Wang, S. J., & Yang, C. H. (2005). Hierarchy-oriented searching algorithms using alternative duplicate codewords for vector quantization mechanism. Applied mathematics and computation, 162(2), 559-576.
[14] Jeong, S., Won, C. S., & Gray, R. M. (2004). Image retrieval using color histograms generated by Gauss mixture vector quantization.Computer Vision and Image Understanding, 94(1-3), 44-66.
[15] Masselos, K., Merakos, P., Stouraitis, T., &Goutis, C. E. (1998). A novel algorithm for low-power image and video coding.IEEE transactions on circuits and systems for video technology, 8(3), 258-263.