

DESIGN OF MULTILEVEL INVERTER WITH REDUCED SWITCH TOPOLOGY

T.Arun Prasath¹, P.kiranmai², V.Priya dharshini³

1,2,3 Department of Electrical and Electronics Engineering, Kalsalingam Academy of
Research and Education, Krishnankoil, Sriviliputtur, Tamilnadu, India

ABSTRACT

To design a new general cascaded multi-level inverter using developed H-bridges. Generate the 9 voltages levels using H-bridge the modified inverter single cell topology. To design a new general cascaded multi-level inverter with less number of voltage sources. Propose a topology which requires a lesser number of dc voltage sources and power switches. To design an modified inverter topology that consist of lower blocking voltage on switches , which results in decreased complexity and total cost of the inverter.

1.INTRODUCTION

In Now-a-days multi-level inverter having several advantages such as high power quality , lower orders harmonics, lower switching losses, and better electromagnetic interference for high power and medium voltage operations. The cascaded multi-level inverter is composed of a number of single –phase H-bridge inverters. The major advantages of this topology is to generate a considerable number of output voltage levels by using a low number of dc voltage sources and power switches, for generating multi-levels of voltages the H-bridge has to be provided with separate dc isolated sources which makes the inverter costlier than other.

2. LITERATURE SURVEY

A novel multi-level inverter based on switched dc sources, it required more number of dc sources for each cell in the topology /switches capacitors can be used in each cells to supply each H-bridge .Hybrid seven level converter based on T-type converter and H-bridge cascaded under SPWM and SVM, Capacitor balancing gets complex with increasing the output levels/optimal PWM techniques can be employed to balanced the capacitor voltages . A new boost switched capacitor multi-level converter reduced circuit devices , the capacitor voltage balancing and boosting process may not generate the required voltages/Pi based PWM control can be applied to generate the required voltage levels.

3.PROPOSED SYSTEM

The proposed method is designed based on the reduction of switches . Proposed inverter can synthesize up to nine voltage levels with a single dc bus. A combination of the H – bridge and the flying capacitor mode is used to generate the MLI. The inverter uses only 2 H-bridges where one of the full bridges is supplied by a flying capacitor . A suitable switching strategy is employed to regulate the flying –capacitor voltages, improve the efficiency which maintains the voltages level of the inverter

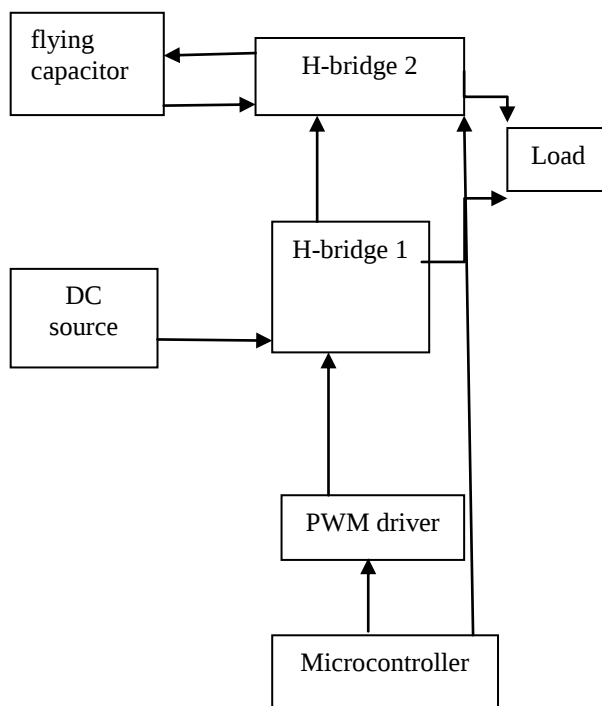


Fig3.2: Block Diagram

3.3. WORKING PRINCIPLE

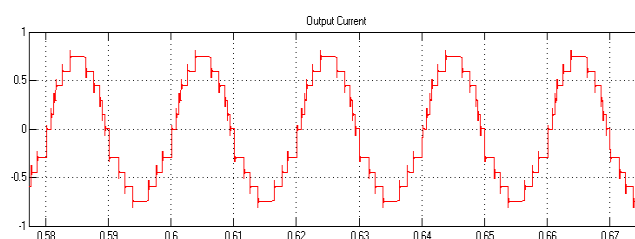
The proposed switching strategy aims at reducing the switching power losses. Reduction in the switches –per-output voltage- level ratio can be achieved in CFB structures if different supply voltages are chosen for each full bridge in the system to asymmetrical CFBs generating nine output voltages. In this proposed system the DC voltage source supplies one of the full bridges, where as a flying capacitor suppliers the other one. It is maintained as the study state the flying capacitor voltage V_{FC} is lower than the DC link voltage V_{DC} , for this reason the full bridge supplied by the flying capacitor is defined as the low-voltage full bridge (LVFB) while the other is defined as the high-voltage full bridge (HVFB). The majority of the communications have to happen in the LVFB, in order to limit switching losses. The operating structures of the inverter are divided into zones with a modified SVPWM to generate exact voltage levels without redundant. By suitable controlling the ratio between the two voltages different sets of output levels can be obtain.

S.No	Component	Specification
1	MOSFET-IRF 840	Third generation power MOSFETs that provide the best combination of fast switching ruggedized device design low on-resistor and cost effectiveness.
2	Opto-coupler	An opto-coupler TLP 250 is used to isolate the gate drive circuit and the MOSFET based multilevel inverter circuit. The single phase induction motor is fed by cascade H-bridge multilevel inverter.
3	Flying-Capacitor	Flying capacitor is of series connection of capacitor clamped switching cells. In this inverter switching states are like in the diode clamped inverter. The output is half of the input to the DC voltage so it is the drawback of flying capacitor multilevel inverter.
4	DC sources	A cascade H-bridge multilevel inverter topology is presented. This cascade H-bridge is designed with single DC source with the only single DC source, the proposed topology is able to generate up to seven voltages level with a voltage boosting gain.
5	Power supply	A power supply is an electrical device that supplies electric power to an electrical load. The power supply is to convert electric current from a source to the correct voltage, current and frequency to power the load.

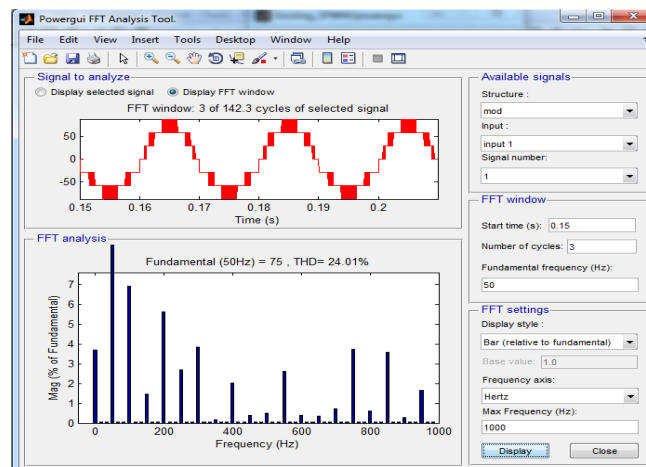
Table 3.4: Components description

4.RESULT

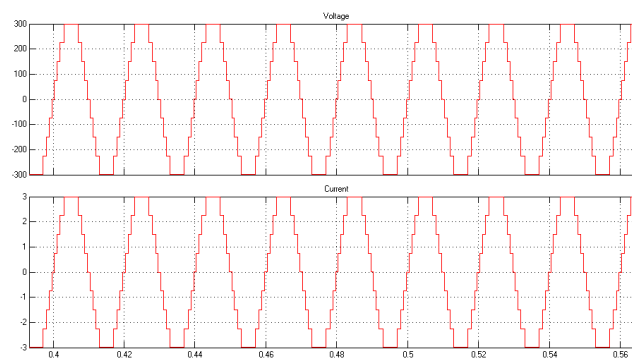
Output Current :



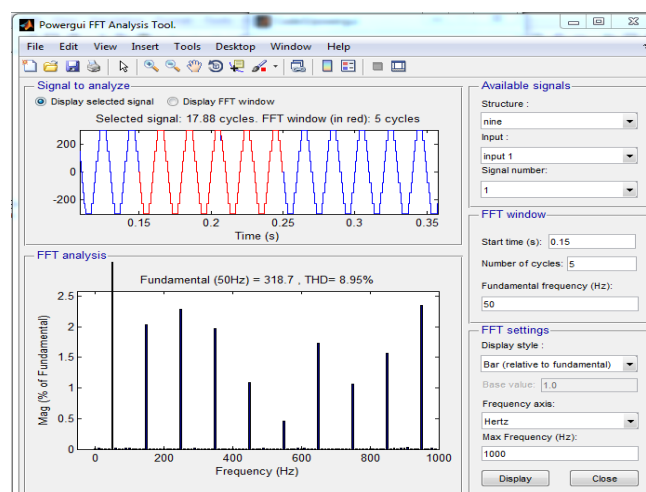
THD of output voltage :



9 Level output voltage and current wave form:



THD of 9 level output voltage:



5. CONCLUSION

We can conclude that in cascade multilevel inverter topology with proper switching angle and conduction period derived from the calculation based on fourier analysis. THD can be reduced at further more amount at least in software based simulation .we can eliminating considerable amount of harmonics and we can reduced THD and

by adding harmonic filter of proper frequency. So , finally by using proper switching angles and by adding filter we have reached at the THD level.

6.REFERENCES

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