International Journal of Advance Research in Science and Engineering
Volume No.08, Issue No.03, March 2019
www.ijarse.com
IJARSE
ISSN: 2319-8354

Design of 16 bit Vedic Multiplier Using Modified Carry Select Adder

Farheen Banu Khan[1], Asst.Prof.Sonia Kuwelkar[2]

[1,2]Department of Electronics and Telecommunication Engineering,
Goa College of Engineering (India)

Abstract:

This paper proposes a high speed and low power 16 x 16 Vedic Multiplier using Modified Carry Select Adder(MCSA).An ancient technique of Vedic Mathematics is introduced namely Urdhva-Tiryagbhyam sutra which is quite different from normal shift and addition operations. Carry Select Adder(CSA) is known to be fastest among conventional adder structures.In this paper,we employ a newly incremented circuit in CSA architecture.The main focus of this paper is to design a low power and high speed Vedic Multiplier using a high speed and low power MCSA architecture. This multiplier is simulated using Modelsim SE 5.7g.

Keywords—*Vedic Multiplier, Carry Select Adder, Binary to Excess-1 converter, Ripple Carry Adder.*

1. INTRODUCTION

Real time digital signal processing(DSP) involves rigorous multiplication operations, which increases the computational complexity of modern day processors[10].Thus need of fast and efficient multiplication units is essential. Performance of Multiplier is essential in the entire processing system. Performance of multiplier speed and area has become a major challenge in today's DSP systems and microprocessor applications. The ancient mathematical techniques known as Vedic Mathematics is implemented to reduce computional complexity, increases speed and requires less hardware[5].Sri Bharti Krishna Trithaji(1884-1960) proposed a theory of Vedic Mathematics consisting of 16 sutras which is related to different branch of mathematics like algebra, arithmetic geometry[9][5].Associating Vedic multiplication techniques with processing systems would save computional time.

2. RELATED WORK

Devika Jaina[1]implemented a high speed and low power Vedic Multiplier using conventional carry save adder.In this paper, combinational delay is compared with Modified Wallace Tree Multiplier.Here,Vedic multiplier shows better performance in terms of delay.

Prabha S[2] presented a technique for implementing squaring operation using Vedic multiplier.It is implemented using VHDL and synthesized using Xilinx tool. Computational Time, Delay, area have been evaluated and compared .

Vaijyanath Kunchigi[3] presented implementation of Vedic multiplier and synthesized using Xilinx tool. It is implemented for 4x4 bit multiplication using Verilog HDL language.

R. Pushpangadan[4] implemented high speed Vedic multiplier for digital signal processors.

International Journal of Advance Research in Science and Engineering
Volume No.08, Issue No.03, March 2019
www.ijarse.com
IJARSE
ISSN: 2319-8354

3. VEDIC ALGORITHM

3.1 Urdhva-Tiryagbhyam Sutra

In this section, we propose a Vedic multiplication technique called "Urdhva-Tiryagbhyam"(Vertically and Crosswise algorithm) which is used for decimal as well as binary multiplication. This technique mainly consists of generation of partial products parallel and have to perform addition operation simultaneously[5].As high frequency operation increases processing power it leads to power dissipation at high operating temperature.Vedic Multiplier does not depend upon the clock frequency operation[5][13].The use of Vedic multipliers reduces power dissipation, delay and area as compared to other multipliers.This Vedic multiplier is used for n x n bit multiplications.

Figure 1 shows the steps required for multiplication by using Urdhva-Tiryagbhyam sutra.For this we consider the multiplication example of 576 x 324.From figure 1 first multiply the left most digit 6 of the multiplicand vertically by the left most digit 4 and it gives the result as 24 from that result product 4 and carry 2 set down as the left hand most part of the answer,then multiply 7 x 4 and 6 x 2 crosswise and add them get 40 and add carry 2 from previous as the sum set it down as the middle part of the answer and so on.lastly we get the result as 576 x 324 = 186624[9].

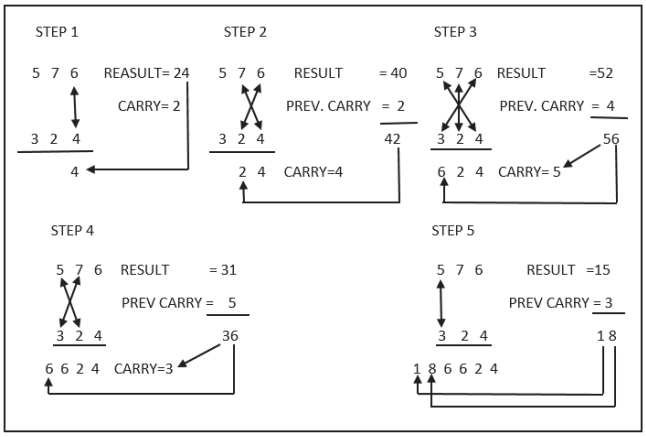

Fig 1:Multiplication steps of Urdhva-Tiryagbhyam sutra[9].

4. IMPLEMENTATION OF VEDIC MULTIPLIER ARCHITECTURE

In this section, the Vedic multiplication for 2 x 2 ,4 x 4,8 x 8,16 x 16 bit are discussed.The main advantage of Vedic Multiplier is that generation of partial products and addition is done simultaneously.This feature of parallel processing of results becomes more attractive to binary multiplications.

International Journal of Advance Research in Science and Engineering
Volume No.08, Issue No.03, March 2019
www.ijarse.com
IJARSE
ISSN: 2319-8354

4.1 Implementation of 2 x 2 Vedic Multiplier

For implementation of 16 x 16 Vedic multiplier we use 2 x 2 Vedic multiplier as the basic building block.As shown in figure 2, let us consider 2 bit numbers A and B where A =*a*1*a*0 and B = *b*1*b*0.The least significant bits(LSB) are multiplied which gives the LSB of the final product(vertical).Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with the product of the LSB of the multiplier and next higher bit of the multiplicand (crosswise).The sum gives second bit of the final product and the carry is added with the final product obtained by multiplying the most significant bits(MSB) to give sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit of the final product.

*s*0 = *a*0*b*0; (1)

*c*1*s*1 = *a*1*b*0 + *a*0*b*1; (2)

*c*2*s*2 = *c*1 + *a*1*b*1; (3)

The final result will be *c*2*s*2*s*1*s*0.This multiplication methods is applicable for all the cases[11][5].

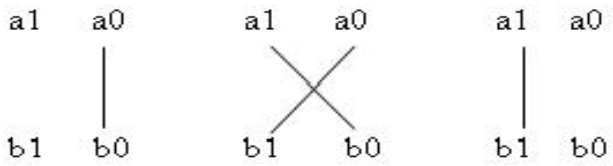

Fig 2:Vedic Multiplication method for 2 bit binary numbers[11].

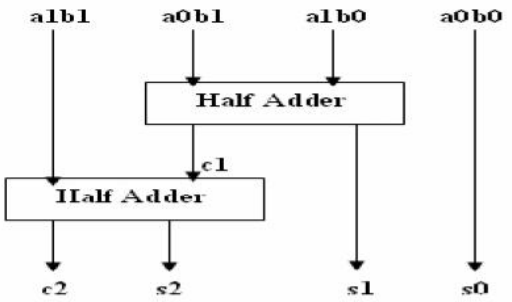

Fig 3: Block Diagram of 2 x 2 Vedic Multiplier[11]

The 2 x 2 bit Vedic multiplier block is implemented using four 2-input AND gates and two half adders.

4.2 Implementation of 4 x 4 Vedic Multiplier

The 4 x 4 bit Vedic Multiplier module is implemented using four 2 x 2 bit Vedic Multiplier modules as described in figure 4.Let us consider 4 x 4 multiplications ,say A =A_3 A_2 A_1 A_0 and B = B_3 B_2 B_1 B_0.The output line for the multiplication result is S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0.Lets divide A and B into two parts, say A_3 A_2 and A_1 A_0 for A and B_3 B_2 and B_1 B_0 for B. By using Vedic Multiplication technique, taking two bit at a time and using 2 bit multiplier block,we have the following structure for multiplication as shown in figure 4[11].

International Journal of Advance Research in Science and Engineering
Volume No.08, Issue No.03, March 2019
www.ijarse.com
IJARSE
ISSN: 2319-8354

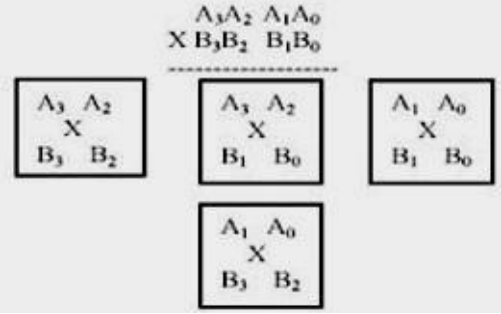

Fig 4:Vedic Multiplication method for 4 bit binary number[11].

Observe the block diagrams for 4 x 4 as shown in figure 5 and within the block diagram, there are four 2 x 2 Vedic Multiplier blocks and three ripple carry adders which are of four bit size are used.The four bit ripple carry adders are used for addition of two four bits and likewise totally four are used at intermediate stages 3 of multiplier.The carry generated from the first ripple carry adder is passed on to the next ripple carry adder and there are two zero inputs for second ripple carry adder.The arrangement of the ripple carry adders are shown in fig 5 below.

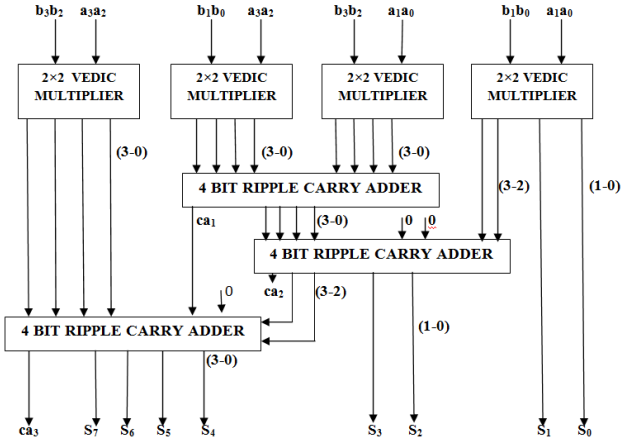

Fig 5:Block Diagram 4 x 4 Vedic Multiplier[5]

4.3 Implementation of 8 x 8 Vedic Multiplier

In this section,we will discuss about 8 x 8 bit Vedic Multiplier.Let us consider two 8 bit numbers A and B can be respresented as A[7:0] and B[7:0] respectively.The final output can be obtained as S[15:0].The partial products are calculated in parallel and delay is decreased effectively.Here the multiplication is followed according to the steps shown in the below diagram in figure 6.After the performing all the steps the sum (Sn) and carry (Cn) is obtained and in same way at each step the previous stage carry is forwarded to the next stage and the process goes on.

International Journal of Advance Research in Science and Engineering
Volume No.08, Issue No.03, March 2019
www.ijarse.com
IJARSE
ISSN: 2319-8354

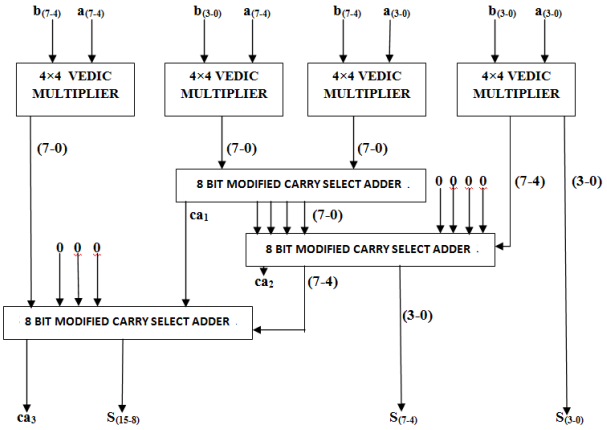

Figure 6. Block Diagram of 8x8 bit Vedic Multiplier[5]

Observe the block diagrams for 8 x 8 as shown above in figure 6 and in the block diagram there are totally four 4 x 4 Vedic multiplier modules and three 8 bit Modified Carry Select Adders(MCSA).The two 8 bits are added in the 8 bit MCSA and totally four are used at intermediate stages of multiplier.The carry generated from the first MCSA is passed on to the next modified carry select adders.Thus,this adder reduces the computational time[5][11].

4.4 Implementation of 16 x 16 Vedic Multiplier

In this section, we will discuss about 16 x 16 Vedic multiplier. Let us consider two 16 bit numbers A and B that are represented as A[15:0] and B[15:0] respectively.The final output can be obtained as C16S[31:0].The partial products are calculated in parallel and delay is decreased effectively.

16 bit Modified Carry Select Adder: The block diagram consists of the following parts

1. Ripple Carry Adder(RCA)
2. Basic Unit(Binary to Excess-1 converter)
3. Multiplexer

1)Ripple Carry Adder: The RCA uses multiple full adders to perform addition operation. Each full adder inputs a carry-in which is the carry-out of the preceding adder[].Each carry bit 'ripples' to the next full adder. RCA is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder.It uses large AND, OR, NOT gates[12].

2)Binary to Excess-1 converter(BEC-1):BEC-1 is used to add 1 to the input numbers. We are using XOR, AND ,NOT gates and by implementing this gates we are reducing the area,time delay, power consumption because of reduction in number of gates when compared to ripple carry adder. The 4 bit BEC-1 is shown in figure 7.Using BEC together with a multiplexer(mux) one input is the output of ripple carry adder gets as it input and another input of the mux is the BEC output. This gives the two partial results in parallel and the mux are used to select either BEC output or the direct inputs accordind to the given control signal[5][8].

International Journal of Advance Research in Science and Engineering
Volume No.08, Issue No.03, March 2019
www.ijarse.com
IJARSE
ISSN: 2319-8354

The Boolean expressions of 4-bit BEC are listed below:

$$X0 = \sim B0$$

$$X1 = B0 \wedge B1$$

$$X2 = B2 \wedge (B0 \,\&\, B1)$$

$$X3 = B3 \wedge (B0 \,\&\, B1 \,\&\, B2)$$

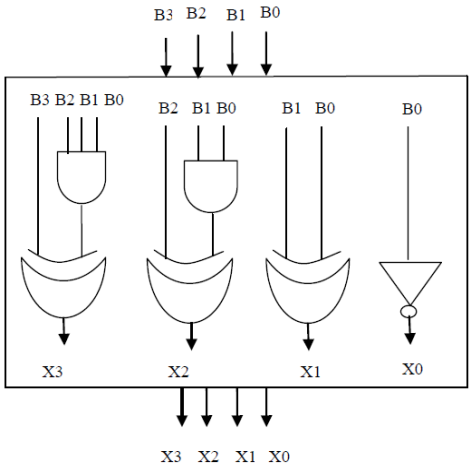

Fig 7: 4 bit Binary to Excess-1 converter[8]

3)Multiplexer: Multiplexer has 2^n inputs having n select lines. Depending upon the select line the input is send to the output. In this architecture, for each RCA we are using five 2:1 Multiplexers and the outputs can be obtained as the five values and among them one can be used as the carry for the next block and remaining can be used for the representation of the output[5].

Figure 8 shows 16 bit Modified Carry Select Adder. MCSA makes use of single RCA and BEC-1 instead of using dual RCAs to reduce area and power consumption.Here the number of logic gates are used less than that of RCA.Thus BEC replaces the RCA with Cin=1 instead of using dual RCAs to reduce area and power consumption of the conventional CSA.To replace the N-bit RCA,an N+1 bit BEC is required[8]. The five multiplexers can give the outputs as the ripple carry adder or BEC-1 output,based upon the control signal we are selecting the output.

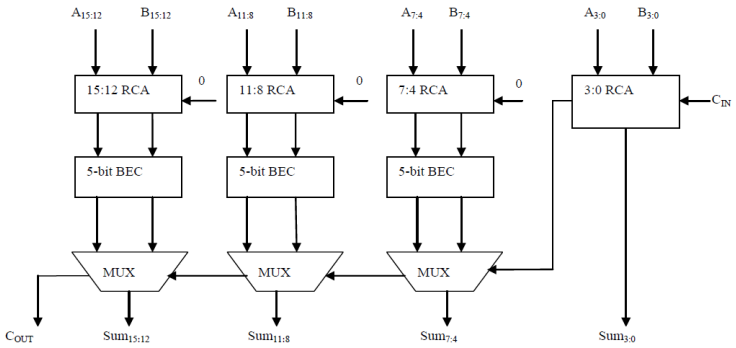

Fig 8: 16 bit Modified Carry Select Adder[8]

International Journal of Advance Research in Science and Engineering
Volume No.08, Issue No.03, March 2019
www.ijarse.com
IJARSE
ISSN: 2319-8354

Observe the block diagrams for 16 x 16 as shown below in figure 9 and within the block diagram there are four 8 x 8 Vedic multiplier modules and three Modified Carry Select Adders which are of 16 bit sized.

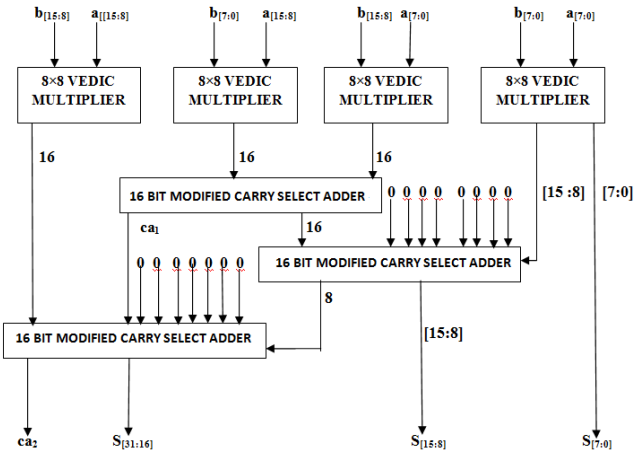

Fig 9: Block Diagram of 16 x 16 Vedic Multiplier[5]

5. RESULTS

2x2, 4x4, 8x8, 16x16 multiplication operations are designed and simulated using Verilog HDL and Modelsim SE 5.7g.

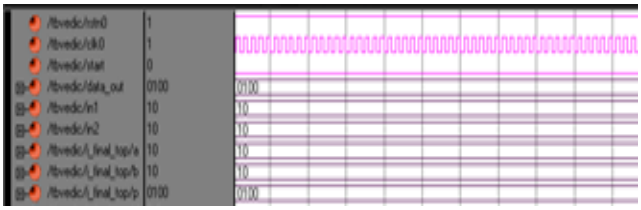

Fig 10:Simulated Waveform of 2 x 2 Vedic Multiplier

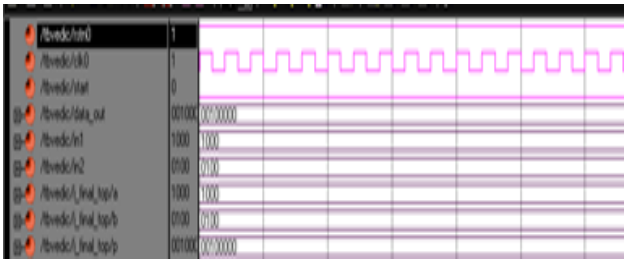

Fig 11:Simulated Waveform of 4 x 4 Vedic Multiplier

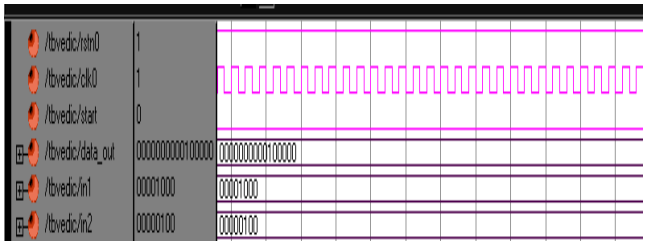

Fig 12:Simulated Waveform of 8 x 8 Vedic Multiplier

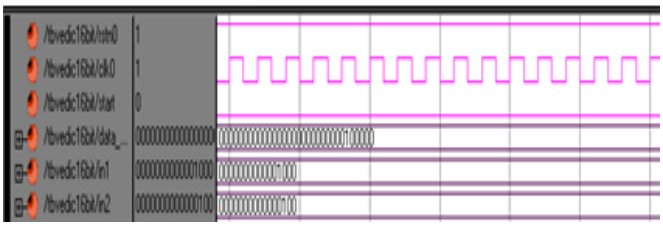

Fig 13:Simulated Waveform of 16 x 16 Vedic Multiplier

6. CONCLUSION

From the results it can be observed that Vedic Multiplier for 2 x 2, 4 x 4, 8 x 8, 16 x 16 is simulated and designed. Further can be extended to implement pipelined architecture of Vedic Multiplier to improve the speed of the multiplier.

REFERENCES

[1] Devika, K. Sethi and R.Panda, "Vedic Mathematics Based Multiply Accumulate Unit," IEEE 2011 International Conference on Computational Intelligence and Communication Systems, CICN 2011, pp.754-757, Nov. 2011.

[2] Prabha S., Kasliwal, B.P. Patil and D.K. Gautam, "Performance Evaluation of Squaring Operation by Vedic Mathematics", IETE Journal of Research, vol.57, Issue 1, Jan-Feb 2011.

[3]Vaijyanath Kunchigi, Linganagouda Kulkarni, Subhash Kulkarni"High Speed and Area Efficient Vedic Multiplier" IEEE 2012 International Conference on Devices, Circuits and Systems (ICDCS), March 2012.

[4] R. Pushpangadan, V. Sukumaran, R.Innocent, D. Sasikumar, and V.Sundar, "High Speed Vedic Multiplier for Digital Signal Processors," IETE Journal of Research, vol.55, pp.282- 286, 2009.

[5] Bhavani Prasad.Y, Ganesh Chokkakula, Srikanth Reddy.P and Samhitha.N.R, " Design of Low Power and High Speed Modified Carry Select Adder for 16 bit Vedic Multiplier" IEEE International Conference on Information Communication and Embedded Systems (ICICES2014), Feb. 2014.

[6] G.Challa Ram, D.Sudha Rani, R.Balasaikesava, K.Bala Sindhuri , "VLSI Architecture for delay efficient 32-bit Multiplier using Vedic Mathematic sutras", IEEE International Conference On Recent Trends In Electronics Information Communication Technology, May 20-21, 2016, India.

[7] K.Anirudh Kumar Maurya,Y.Rama Lakshmanna,K.Bala Sindhuri,N.Udaya Kumar, "Design and Implementation of 32-Bit Adders Using Various Full Adders", International Conference on Innovations in Power and Advanced Computing Technologies [i-PACT2017].

[8] Sarabdeep Singh, Dilip Kumar, "Design of Area and Power Efficient Modified Carry Select Adder", International Journal of Computer Applications (0975 – 8887) Volume 33– No.3, November 2011

[9] S.P.Pohokar, R.S.Sisal, K.M.Gaikwad, M.M.Patil, Rushikesh Borse, "Design and Implementation of 16 x 16 Multiplier Using Vedic Mathematics",2015 International Conference on Industrial Instrumentation and Control (ICIC) College of Engineering Pune, India. May 28-30, 2015.

[10] Suryasnata Tripathy, L B Omprakash, Sushanta K. Mandal, B S Patro "Low Power Multiplier Architectures Using Vedic Mathematics in 45nm Technology for High Speed Computing", 2015 International Conference on Communication, Information & Computing Technology (ICCICT), Jan. 16-17, Mumbai, India.

[11] B.Ratna Raju, D.V.Satish, "A High Speed 16x16 Multiplier Based On Urdhva Tiryakbhyam Sutra", International Journal of Science Engineering and Advance Technology, IJSEAT, Vol 1, Issue 5, October – 2013, ISSN 2321-6905

[12] Samiappa Sakthikumaran, S. Salivahanan, V. S. Kanchana Bhaaskaran, V. Kavinilavu, B. Brindha and C. Vinoth, "A Very Fast and Low Power Carry Select Adder Circuit", Electronics Computer Technology (ICECT), 2011 3rd International Conference on, Volume: 1,May 2011.

[13] Nikhil R. Mistri, Prof. S.B. Somani, Prof.Dr.V.V.Shete, "Design and Comparsion of Multiplier using Vedic Mathematics", International Conference on Inventive Computation Technologies(ICICT),26-27Aug 2016,Coimbatore,India.