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IMPLEMENTATION OF HIGH EFFICIENCY FULL ADDER

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ABSTRACT

A combinational logic circuit is said to be independent of time since it gives the results based on present input alone.This paper is concerned about the comparison between the full adder circuits using CMOS logic, pass transistor logic and transmission gate logic.Analysis of their delay and power dissipation and simulations of three full adder circuits was made.The theoritical analysis and simulations show that a worst case delay and total power dissipation in the PTL design and TG design are better than conventional CMOS logic design.Observing the distortion in the result of both full adder the behaviour of efficient full adder is designed.

Keyword: CMOS,Full adder, ,PTL,TG,Tanner.

I. INTODUCTION

The high speed,low power and efficiency in Very Large Scale Integration(VLSI) can be implemented with different logic styles.There are many proposed logics for high speed and low power dissipation.But each logic style has its own advantage in terms of power,efficiency and layout implementation.

In this research,CMOS logic and complementary pass transistor logic are compared to implement an efficient full adder circuit.CMOS logic is selected as it is the most common logic style and CPL is selected as it is believed to have more advantages over CMOS design.Full adder circuit is choosen as it is the most commonly used arithmetic blocks in CPU and DSP,therefore its performance and power optimization is of atmost important.The main goal of this research is to provide high efficiency and a better logic style for implementing full adder logic circuit.

II. LOGIC DESIG

A. CMOS logic design

CMOS are built from an NMOS pull-down and a PMOS pull-up logic network.Input signals are connected to transistor gates only ,which facilitates the usage and characterization of logic cells .The layout of CMOS gates is straight forward and efficient due to the complementary transistor pairs.Advantages of the CMOS logic style are its robustness against voltage scaling and transistor sizing(high noise margins) and thus reliable operations at low voltages and arbitrary(even minimal) transistor sizes(ratioless logic).A disadvantage of complementary CMOS is the substantial number of large PMOS transistors,resulting in high input loads(higher power,higher delay,higher area).

A CMOS full adder circuit is the logic that has three inputs:A,B and C and two outputs:Sum and Carry.CMOS full adder uses more than one NMOS and one PMOS transistor(s).The NMOS(s) is used in pull down network and PMOS(s) is used in pull up networks.

BASIC OPERATION:

When input logic is low(0),the NMOS is off and the PMOS is on.Hence,the output is connected to VDD through PMOS.When the input logic is high(1) the NMOS is on and the PMOS is off.Hence,the output is connected to ground through NMOS.Now for more number of transistor design using CMOS VLSI design there are two rules to be followed:

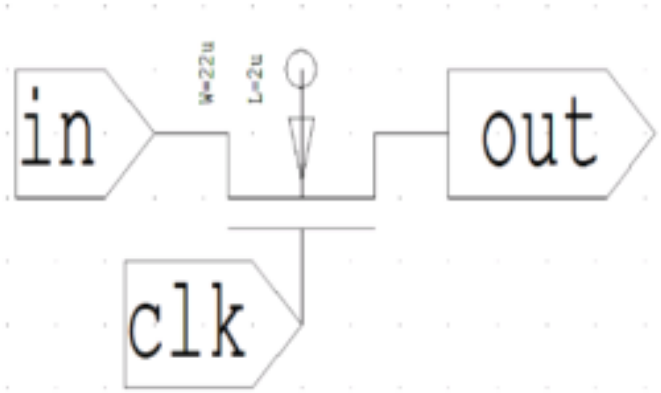
(i) If AND operation(multiplication) is to be designed,then NMOS transistors need to be connected in series at PDN and PMOS transistors in parallel at PUN.
(ii) If OR operation(addition) is to be designed,then NMOS transistors need to be connected in parallel at PDN and PMOS transistors in series at PUN.

(iii) PASS TRANSISTOR LOGIC(PTL) DESIGN

The basic difference of pass transistor logic compared to the CMOS logic style is that the input signal is to the source side of the logic transistor network the advantage is that one pass transistor network(either NMOS or PMOS) is sufficient to perform the logic operation which results in the smaller number of transistors and smaller input loads,especially when NMOS networks are used however the threshold voltage drop(Vout=Vdd-Vtn) through the NMOS transistors,output is weak"1",which will cause static currents at subsequent output inverters or logic gates.

The pass transistor is driven by a periodic clock signal and acts as an access switch to either charge up or charge down the parasitic capacitance Cx,depending on the input signal Vin.Thus,two possible operations when the clock signal is active (clk=1) are logic"1" transfer(charging up the capacitance Cx to a logic-high level) and

logic"0" transfer(charging down the capacitance Cx to a logic low level).In either case,the output of the depletion load NMOS inverter obviously assumes a logic-low or a logic-high level depending on the voltage Vx.



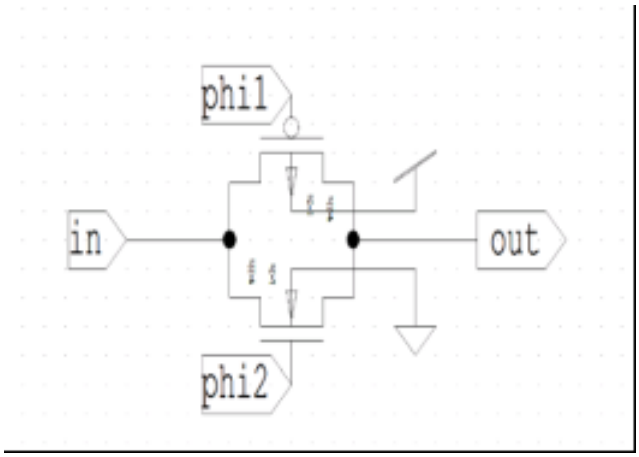
a.Pass transistor logic

B. **TRANSMISSION LOGIC DESIGN**

A transmission gate(TG) is similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential.It is a CMOS based switch,in which PMOS passes a strong one but poor zero,and NMOS passes strong zero but poor one both PMOS and NMOS works simultaneously.

When the control input is a logic zero (negative power supply potential), the gate of the n-channel MOSFET is also at a negative supply voltage potential. The gate terminal of the p-channel MOSFET is caused by the inverter, to the positive supply voltage potential. Regardless of on which switching terminal of the transmission gate (A or B) a voltage is applied (within the permissible range), the gate-source voltage of the n-channel MOSFETs is always negative, and the p-channel MOSFETs is always positive.Accordingly,neither of the two transistors will conduct and the transmission gate turns off.

When the control input is a logic one, the gate terminal of the n-channel MOSFETs is located at a positive supply voltage potential. By the inverter, the gate terminal of the p-channel MOSFETs is now at a negative supply voltage potential. As the substrate terminal of the transistors is not connected to the source terminal, the drain and source terminals are almost equal and the transistors start at a voltage difference between the gate terminal and one of these conducts.

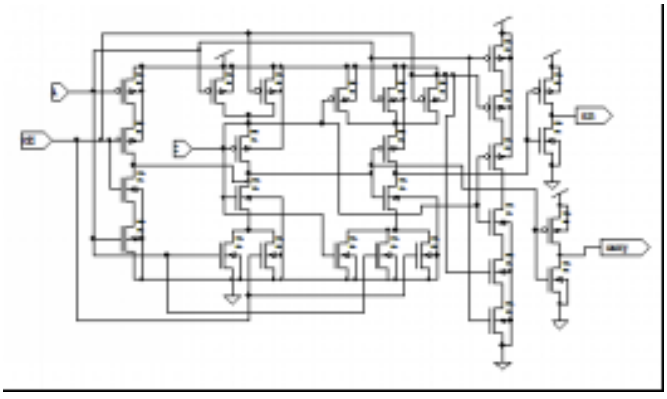


b.Transmission gate logic

III.FULL ADDER CIRCUITS

A .CMOS FULL ADDER CIRCUIT

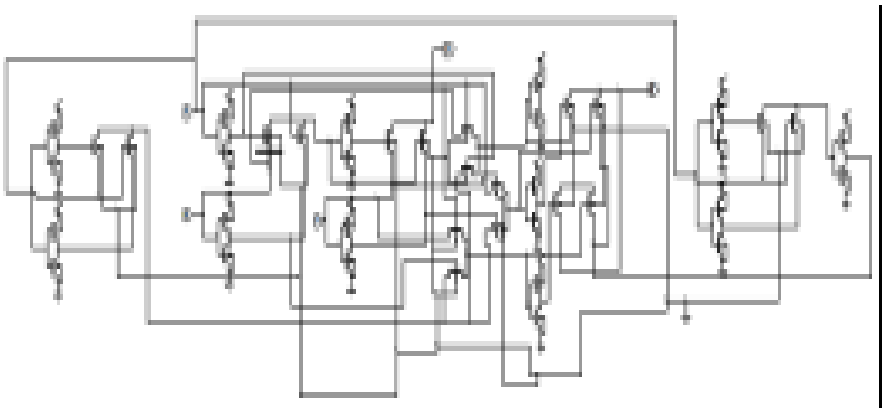
A complementary static CMOS circuit consists of an NMOS pull down network connecting the ground to the output and a PMOS pull up network connecting the power to the output.A typical CMOS full adder logic circuit is designed shown in below circuit.



a. CMOS full adder circuit

B. PTL FULL ADDER CIRCUIT

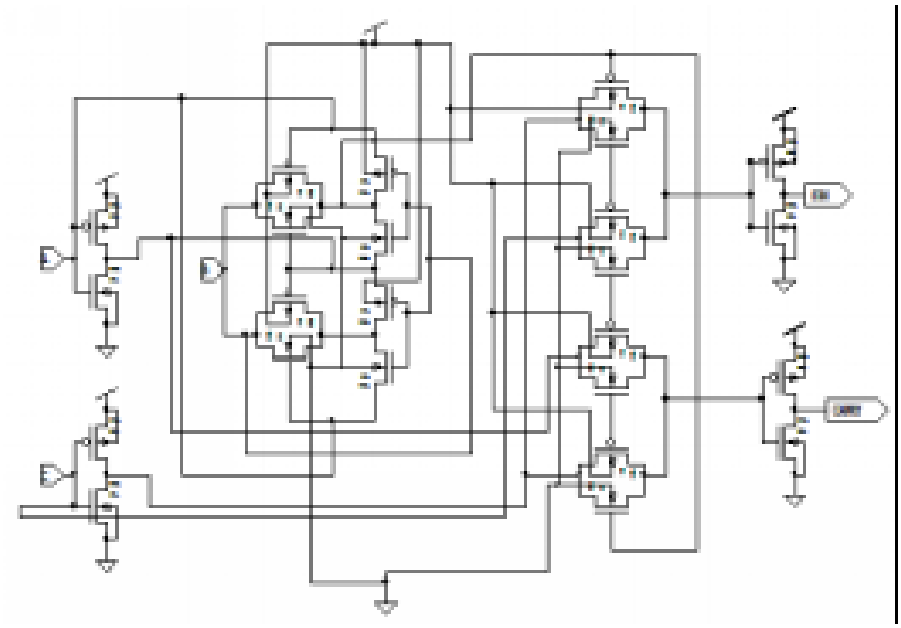
A PTL full adder logic circuit is designed shown below.In this circuit,one small pull-up NMOS transistor for swing restoration in the sum output signal and another one small pull-up NMOS transistor for swing rotation in the carry output signal.



b. Pass transistor full adder circuit

C. TRANSMISSION GATE FULL ADDER CIRCUIT

A TG full adder logic circuit is designed shown below.Transmission gates are widely used as a CMOS design style to implement digital function.TG based implementation is similar to pass transistor with a difference that TG logic uses both NMOS and PMOS transistors connected in parallel where as pass transistor logic uses only one type of transistor either PMOS or NMOS.



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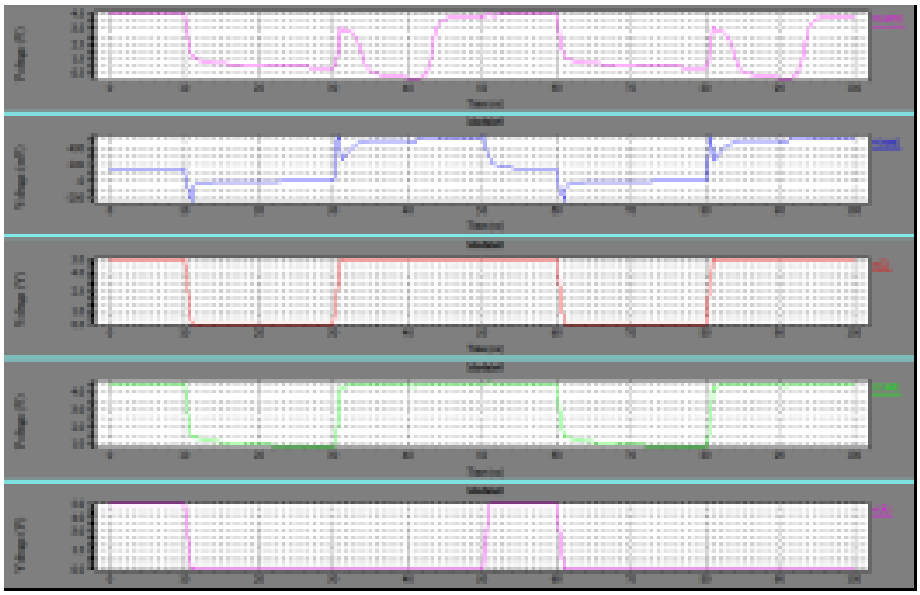
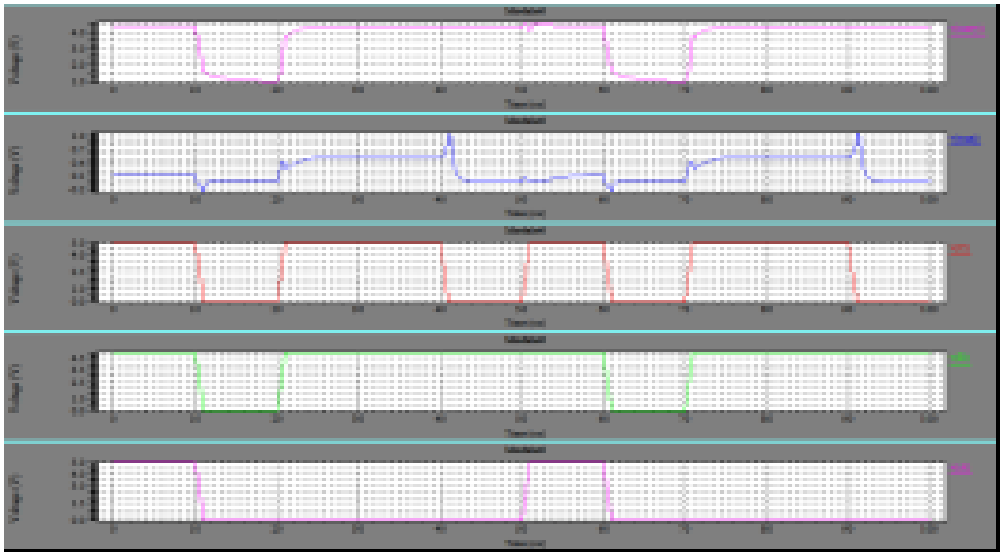
IV.RESULT ANALYSIS

ANALYSIS OF CMOS,PTL,TG FULL ADDER LOGICS

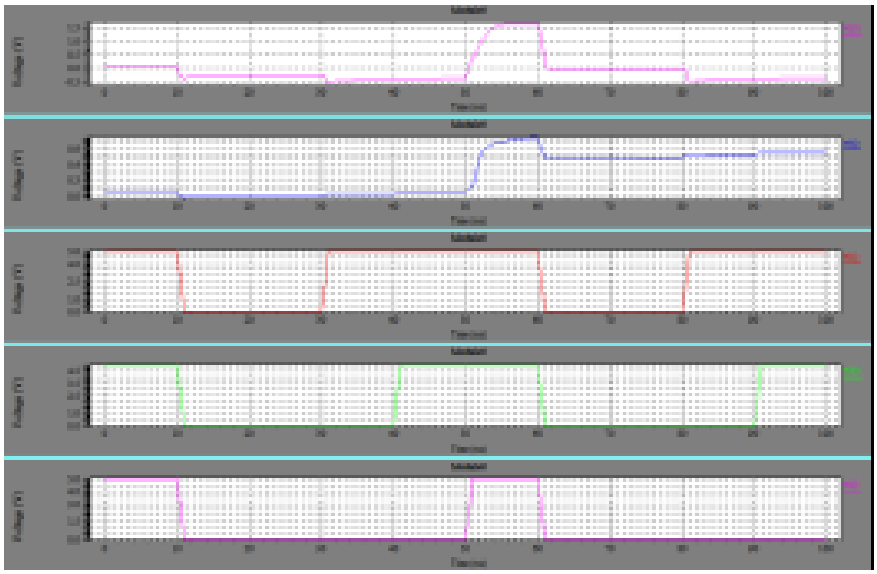
OUTPUT WAVEFORMS



a.Output waveform for CMOS full adder



b.Output waveform for PTL logic full adder



c.Output waveform of RG logic full adder

V. CONCLUSION

We have designed three full adder circuits using CMOS ,PTL and TG logic in which the simulation shows that the power dissipation in CMOS is 32.186 micro -watts and PTL is 26.124 micro-watts and TG is 27.842 micro-watts .The design simulation shows a worst case delay only 0.45 ns for PTL as compared to 0.90 ns delay for conventional CMOS and 0.62 ns for TG .The theoretical analysis and simulations show that a worst case delay and total power dissipation in the PTL logic design are better than both TG and CMOS logic design .

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