International Journal of Advance Research in Science and Engineering
Volume No.07, Issue No.03, March 2018
www.ijarse.com
IJARSE
ISSN: 2319-8354

Multilevel Inverter topologies with Reduced Power Switch Count: - A Review

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***Abstract*— A multilevel inverter is a power electronic device that is used for high voltage and high power application because of its characteristics of synthesizing a sinusoidal voltage on several DC levels. They give good quality output resulting with lower harmonic distortion in the output. In this paper various Multi level inverter topologies with reduces power switch count are reviewed and analyzed. Topologies are analyzed, based on both the qualitative & quantitative parameters and a detailed comparison of these topologies as presented**

***Index Terms*— Multilevel inverter, Terminology, Topologies Assessment** Parameter, Power **Transmission and** Distribution, Fundamental **switching frequency** operation, reduced **device count.**

I. Introduction

Multi level inverter has been introduced since 1975 as alternative in high power and medium voltage conditions. It's used for industrial applications as voltage situations. It's give a high power output from medium voltage source. Sources like super capacitors, batteries, super capacitors, solar panel are medium voltage sources. It's consists several switches.multi level inverter the arrangement switches' angles are very important. Based on the nature of the output waveform, classification inverters as: square wave inverters, quasi-square wave inverters two-level pulse width modulation (PWM) inverters, and multi-level inverters (MLIs) [1] [2] [3] [4].

A. Multilevel DC to AC Conversion and Classical Topologies

The staircase waveform not only exhibits a better harmonic profile but also reduces the *dv*/*dt* stresses. Thus, the filter requirements can be greatly brought down (or even eliminated), while electromagnetic compatibility problems can be reduced.

1) The voltage stresses on the semiconductor devices are much lesser as compared to the overall operating voltage. Thus, a high-voltage waveform can be obtained with comparatively low-voltage rated switches.

2) MLIs much giving smaller common mode voltage thus; the stress in the bearings of a motor connected to a drive can be reduced.
Many multilevel topologies offer the possibility to obtain a given voltage level with multiple switching combinations. These redundant states can be utilized to program a fault tolerant operation. MLIs can draw input current with low distortion. Renewable energy sources such as fuel cells photovoltaic, wind, and fuel cells and can be easily interfaced to a multilevel converter system and can be controlled for equal load sharing amongst the input sources.

B. Advent of New Topologies with Application-Oriented

Classical topologies" have attracted maximum attention both from the academia and industry. Still, no specific topology seems to be absolutely advantageous as multi-level solutions are heavily influenced by application and cost considerations. Because of its intrinsic characteristics, a given topology can be very well adapted in some cases and totally unsuitable in some others.

C. Topologies with Reduced Device Count and Scope of This Paper

In view of their many advantages, MLIs are receiving much more and wider attention both in terms of topologies and control schemes. MLIs, however, exhibit an important limitation for an increased number of output levels; they require a large number of power semiconductor switches, thereby increasing the cost, volume, and control complexity. Although low-voltage-rated switches can be utilized in an MLI, each switch requires a related gate driver unit, protection circuit, and heat sink.

II. Terminology, Assessment Parameters, And Classification Of Topologies

A. *Terminology*

Topologies are reducing the number of controlled switching
power semiconductor devices for a given number of phase voltage levels are referred to as RDC-MLI topologies [5][6].

1. Reduced Device Count Multilevel Inverter (RDC-MLI) Topologies: Topologies reducing the number of controlled switching power semiconductor devices for a given number of phase volt-age levels are referred to as RDC-MLI topologies. In this paper, nine such topologies [5]–[6] are reviewed.

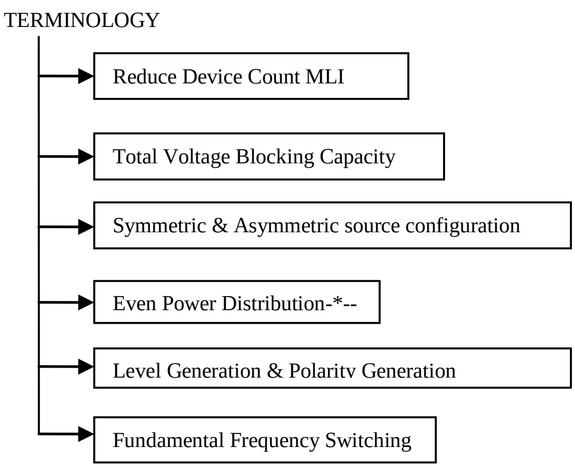

Fig. 1. Classification of Terminology

2. Total Voltage Blocking Capability: A topology, the total sum of the voltage blocking capability requirement for all its power switches is referred to as the "total voltage blocking capability [7].

3. Symmetric and Asymmetric Source Configuration: The source configuration is known as symmetric when the voltages of the input dc levels to an MLI are all equal; otherwise it's called asymmetric. Two popular asymmetric source configurations are: binary and trinity. There are many other asymmetric source configurations are presented by various researchers [8][9].

4. Even Power Distribution: Inverter conversion is carried out in such a way that each input source contributes equal power to the load, the "power distribution" amongst the sources is said to be "even." Some authors also refer to it as "charge balance control" or "equal load sharing" , the control algorithm is designed such that the average current drawn from each source is equal, thereby making average powers equal [10].

5. Level-Generation and Polarity-Generation: An MLI synthesizes a stepped waveform consisting of the input dc levels and their additive and/or subtractive combinations. Thus, the volt-age waveform consists of multiple "levels" with both "positive" and "negative" polarities generation part need to have a minimum voltage rating equal to the operating voltage of the MLI [11].

6. Fundamental Frequency Switching: The switching losses in a converter are proportional to the current, blocking voltage, and switching frequency. To minimize the switching losses, it is preferred to operate higher voltage-rated power switches at a low frequency and if possible [12].

B. *Assessment Parameters*

Merit of any given topology can be primarily judged based on the application for which it has to be employed. Still, in the context of this paper, the general criteria for an overall assessment of the merit of an RDC-MLI and its comparison with the other topologies can be:

1) the number of power switches used;
2) the total blocking voltage of the converter;
3) the optimal controllability of the topology, in terms of the possibilities of charge-balance control (or "even power distribution" amongst the input sources) and appropriate distribution of switching frequencies amongst the differently voltage-rated switches;
4) possibility of employing asymmetric sources/capacitor
Voltage ratios in the topology.

While parameters 1 and 2 affect reliability of the inverter, efficiency is influenced by parameters 1, 2, and 3 and application, performance, and control complexity are governed by parameter

3. Number of redundant states and consequently, programmability of fault tolerant operation, is directly influenced by 1 and

4. In addition, apart from 1 and 2, the cost of a converter also depends on the dispersion of power switching ratings (e.g., using one 400 V switch and one 800 V switch would be, in principle, more expensive than using two 600 V switches).

C. Categorization of RDC-MLI Topologies

In this paper, nine different RDC-MLI topologies, as presented in [5][6], are evaluated.

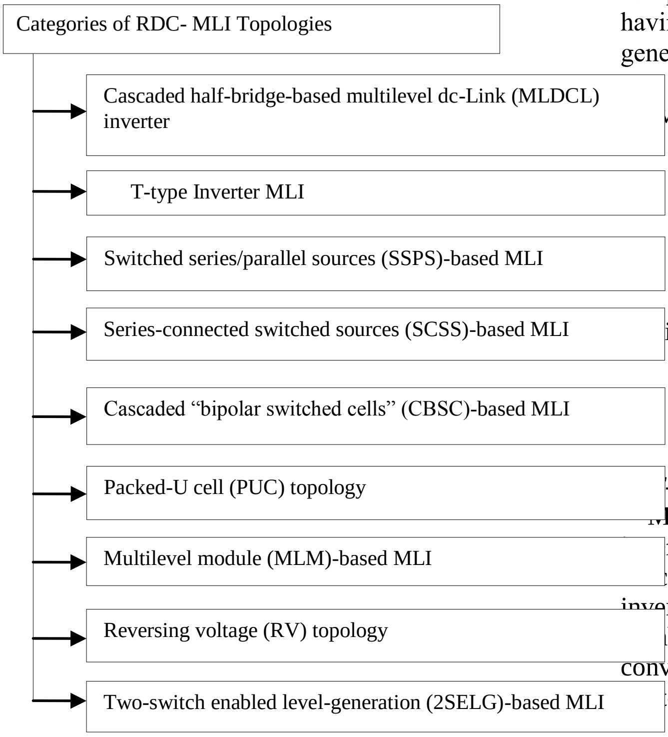

Fig. 2. Categories of RDC- MLI Topologies

These topologies are enlisted as follows.

1) Cascaded half-bridge-based multilevel dc-Link (MLDCL) inverter [5]-[12].
2) T-type Inverter [13]- [14].
3) switched series/parallel sources (SSPS)-based MLI [15], [16];
4) series-connected switched sources (SCSS)-based MLI [17], [18];
5) cascaded "bipolar switched cells" (CBSC)-based MLI [19];
6) packed-U cell (PUC) topology [20]–[21];
7) multilevel module (MLM)-based MLI [7];
8) reversing voltage (RV) topology [22], [11];
9) two-switch enabled level-generation (2SELG)-based MLI [6].

While a detailed analysis of these topologies is presented in Section III, it is important to appreciate that there are several similarities between the different RDC-MLI topologies which can be clearly seen if they are drawn with a similar structure,

III. Review Of MLI Topologies With Reduced Device Count

A. Cascaded Half-Bridge-Based MLDCL Inverter

An MLDCL inverter with four input dc level, comprises of cascaded half-bridge cells, with each cell having its own dc source. It has separate "level-generation" and "polarity-generation" parts.

vantage:-

- Highly modular and simple
- Requires only unidirectional switches
- Equal load sharing is possible amongst symmetric input Sources
- Highest voltage rated switches can be operated at fundamental switching frequency.

itation:-

- Requires isolated input dc levels
- Trinity source configuration cannot be employed.

-Type Inverter

MLI topology, here-with referred to as the "T-type rter." The primary introduction to the topology is ribed in with the help of a five-level single-phase inverter which results in a significant reduction in the ber of power devices as compared to the conventional topologies. A single-phase structure of opology

Advantage:-

- Simple structure
- Requires non isolated input dc levels

Limitation:-

- Requires a mix of unidirectional and bidirectional switches,
- Equal load sharing is not possible, asymmetric source
- configuration is not possible
- Highest voltage rated switches cannot be operated at
- fundamental switching frequency

C. SSPS-Based MLI

Single-phase MLI consisting of an H-bridge and DC sources which can be switched in series and in parallel. The topology is herewith referred to as "SSPS-based MLI." The topology requires the same of numbers of voltage sources as required by a CHB topology but it synthesizes same number of output levels with lesser number of power switches. An important application suggested is for electric vehicular applications where a single battery composed of a number of series-connected battery

IJARSE
ISSN: 2319-8354

cells is available, which can be rearranged using the switched sources topology, hence reducing the requirement of switching devices. More importantly, possibility of combining two or more sources in series and parallel gives enough flexibility for meeting voltage/power requirements in the vehicle drive system.

Advantage:-

- Input dc sources can be combined in both series and parallel
- Equal load sharing is possible amongst input dc sources
- Binary source configuration can be employed

Limitation:-

- Highest voltage rated switches cannot be operated at fundamental switching frequency
- Trinity source configuration cannot be employed

D. SCSS-Based MLI

A topology with sources connected in series through power switches is described in the literature The topology with four input dc sources The low potential terminals of the sources are all connected through power switches while being also connected to the higher potential terminal of the preceding source through power switches,

The possibilities of synthesizing various combinations of input dc levels are summarized. It can be seen that the structure, though simple, allows very restricted possibilities of synthesis of various levels at the bus end. In fact, not even the individual levels offered by the sources can all be

Advantage:-

- Simple structure
- Highest voltage rated switches can be operated at fundamental switching frequency

Limitation:-

- Symmetric source configuration is mandatory
- Power switches are differently voltage-rated
- Equal load sharing is not possible
-

E. CBSC–BASED MLI

This is a single phase structure of the topology with four input source. The topology requires all the switches to be bidirectional blocking –bidirectional –conducting in order to synthesize the required voltage levels at the output .the structure is such that each cell consisting of a sources & power switches can synthesize voltage levels with both its polarities at the load terminals .although each bidirectional switch required two IGBT'S .The total no. of gate drives circuit is equal to the no of bidirectional switches .this result in reducing the cost & overall complexity of the converter.

Advantage:-

- Non-isolated input dc levels are required
- All switches are bidirectional
- Only two switches conduct simultaneously to synthesize a given voltage level

Limitation:-

- Equal load sharing is not possible
- Asymmetry is not possible,
- Switches are differently voltage rated

F. PUC Topology

Multi-level converter topology that is very competitive compared to the classical topologies. The topology is named as the "PUC" topology. It consists of the so-called "packed U-cells." Each U-cell consists of an arrangement of two power switches and one dc input level (obtained with a voltage source or a floating capacitor). Authors claim that the topology offers high energy conversion quality using a small number of active and passive devices and consequently, has very low production cost. A single-phase structure of the packed U-cell topology with four input dc levels, [21][22]the authors has presented an elaborate methodology to calculate the asymmetric voltage levels. For a structure with two input sources, switching of middle two switches can be performed at fundamental frequency as demonstrated in This feature, however, is not feasible for the PUC topology with more than two number of input dc levels Sources. One source is taken as a floating capacitor in which the voltage is maintained at one-third of the voltage level of the other source (obtained with the rectification of input ac). The control scheme, though, is fairly complex in nature

Advantage:-

- Simple structure
- Low losses

Limitations:-

- Sources need to be mandatorily asymmetric
- Complex control
- Isolated input dc levels are required

G. MLM-Based MLI

Topology consists of separate "level-generation" and "polarity-generation" parts. The level-generation part consists of input dc sources and bidirectional-blocking-bidirectional-conducting switches. The voltage stress on these switches is not distributed uniformly. The switches in the polarity-generation part are unidirectional-blocking-bidirectional-conducting and have to withstand the maximum voltage generated by the level generation part. How-ever, these switches can be operated at line frequency as the level generation part is able to generate the zero level. Thus, these switches are high-voltage low-frequency switches.

Advantage:-

- Requires non isolated dc sources
- Simple structure
- Highest voltage rated switches can be operated at fundamental Frequency

Limitation:-

- Requires a mix of unidirectional and bidirectional switches
- Equal load sharing is not possible
- Asymmetric source configuration not possible. RV Topology

Reversing voltage" MLI (RV-MLI) topology which separates the output voltage into two parts: "level-generation" and "polarity-generation." A single-phase RV-MLI with four in-put dc sources,. In this way, the components are utilized effectively. The switches in the polarity-generation part need to withstand the total additive voltage of the level generation part. The topology exhibits modularity for the level generation part.

To overcome the issue of voltage balancing, have presented use of separate dc sources. It is, however, true for several topologies that separate sources can solve the voltage unbalance problem. If separate sources are not used, balancing will have to be achieved by proper utilization of redundant states.

Advantage:-

- Requires non isolated dc sources
- Single dc link feeds all the three phases
- Highest voltage rated switches can be operated at fundamental switching frequency

Limitation:-

- Equal load sharing is not possible
- Asymmetric source configuration is not possible

I. Two-Switch-Enabled Level Generation (2SELG)-Based MLI

This topology presenting specialty of separated parts of "level-generation" and "polarity-generation". In this topology its consisting parts only two conducting switches to synthesize any valid voltage level, irrespective of the number of input sources. Therefore, this topology is referred to as "2SELG-based MLI."

Advantage:-

- Requires non-isolated input dc levels
- Low conduction losses

Limitation:-

- Equal load sharing is not possible
- Asymmetric sources cannot be employed
- Highest voltage rated switches cannot be operated at Fundamental frequency.

Multilevel inverters have experienced, in terms of research, MLI consisting the modulation techniques, and control strategies. In addition, other interesting research topics such the fault tolerant operation, efficiency improvement, optimized control strategies, and new applications are also important. Power electronics community the most recent advances with topics such as the following:

1. New multilevel inverter topologies;
2. New modulation and control strategies for multilevel inverters;
3. Industrial applications of multilevel inverters;
4. Multilevel inverters for renewable energy applications;
5. Common-mode voltage reduction methods in multilevel inverters;
6. Fault-tolerant design of multilevel inverters.

IV. DISCUSSIONS

Based on the analysis of RDC-MLI topologies presented in the previous section, comments can be made on them based on qualitative and quantitative parameters. Based on the qualitative features of these topologies, MLDCL-MLI is a highly modular structure whereas the PUC topology can be appreciated for its sheer simplicity in terms of its structure. Both the topologies, however, require isolated dc sources. SSPS-MLI presented novelty in terms of enabling series and parallel combinations of all the input dc levels. Structures such as T-type inverter, CBSC-MLI, MLM-MLI, and RV topology require non-isolated input dc levels. Also, three-phase configurations with the T-type inverter and RV topology can be implemented with a single dc link. An important feature of 2SELG-MLI is that only four switches need to conduct to obtain a given voltage level across the load terminals. It can be said that when attempts are made to reduce the power switch count, the number of states are reduced and following features may be hampered: even power distribution among the symmetric

V. Conclusion

A review of nine reduce device count multilevel topologies is presented. Based on the review, it can be concluded that in the process of reducing the power switch count, various compromises are involved such as:

1) increased voltage rating of semiconductor switches;
2) requirement of bidirectional switches;
3) increased number of sources and/or requirement of asym-metric input dc levels;
4) loss of modularity;
5) reduced number of redundant states;
6) Complex modulation/control schemes7) difficulty in possibility of charge balance control.

As qualitative and quantitative features of RDC-MLI topologies have been discussed and a comparison has been made so as to facilitate a well-informed selection of topology for a given application. In addition, the paradigm presented in the paper will also help to evaluate the RDC-MLI topologies that will be presented in future.

MLIs continue to gain increasing importance for both high power and low power applications, many researchers have pro-posed specific topological solutions for intended applications. Also, newer multilevel topologies have been presented, offering high output resolution with a reduced number of power switches.

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