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Low-Voltage Current-Mode Realization of Digital Logic Gates using CMOS

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ABSTRACT:

In this paper a new technique is introduced for implementing the basic logic function by using analog current-mode techniques. By expanding the logic function in power series expression, and using adder and sub-tractor realization of the basic logic function is simplified. To illustrate the proposed technique, a CMOS circuit for simultaneous realization of the logic function NOT, AND, OR, NAND and XOR is considered. PSPICE simulation results, obtained with ±2V supply, are included.

Key Word: Current Mirror; CMOS analog multiplier; Current mode; Translinear principle; Digital logic circuits;

I.INTRODUCTION

The current-mode implementation of logic gates is a very important for current mode analog signal processing system. Mixed analog/digital electronic circuits are becoming increasingly important. Digital electronic circuits are mostly designed in CMOS technology. To be able to integrate the digital and analog parts on to one chip, high performance analog CMOS circuits are required [1] and a large number of mixed analog/digital VLSI integrated circuits realized in state-of-the-art digital CMOS technologies are now available [2]. In fact the emergence of ICs incorporating mixed analog and digital functions on a single chip has led to an advanced level of analog design [3]. Of particular interest here is the current-mode approach for designing analog ICs. It is well known that current-mode analog signal processing offers some important speed advantages over the traditional voltage-mode signal processing [4]. At present current-mode implementations are available for a wide range of analog electronic circuits including A/D and D/A converters, continuous time filters, neural-networks, sampled data filters and microwave and optical systems. This raises the following question: Can digital ICs be realized using current-mode analog techniques? In fact analog-based realizations of digital logic circuits may result in avoiding the traditional problems of fan-in and fan-out, inherent in digital-based implementations, less complexity, low-voltage as well as higher speed of operation [5]. In an attempt to answer this question, the translinear principle [6] has been used to realize a digital inverter circuit [7,8] a bistable

element [9] and NOT/OR/NAND/XOR functions [10] . All the realizations of logic gates in current mode reported in references [7,8,9,10] use bipolar technology.

In this paper, we present such an approach, a low-Voltage CMOS analog digital circuit in current-mode where it works with a supply voltage of V_{DD}=-V_{SS}=2V. The circuit is based on the four-quadrant CMOS analog multiplier [12].

II.POWER SERIES REPRESENTATION OF LOGIC FUNCTIONS

Using their truth tables, it is easy to show that the input-output relations of the basic digital logic function can be expressed as [5]:

$$Z= 1- I_x \quad (1)$$

for the NOT operation,

$$Z= I_x*I_y \quad (2)$$

for the AND operation,

$$Z= I_x + I_y – I_x*I_y \quad (3)$$

for the OR operation,

$$Z= 1- I_x*I_y \quad (4)$$

for the NAND operation, and

$$Z= I_x + I_y - 2I_x*I_y \quad (5)$$

for the XOR operation.

In equations (1)-(5) the signs +, - and * carry their normal mathematical operation, that is sum, subtract and multiply respectively. Using equations (2)-(5) in combination with equation (1) the digital-logic functions NOR and XNOR can be realized. Analog implementation of the basic logic functions (1)-(5) requires analog multipliers, inverters and adder. Using a modified version of the four-quadrant multiplier reported in [11], voltage-mode analog implementation of two-input AND, NOT and OR functions have been reported [5]. These implementations, however, are built around voltage-mode operational amplifiers, analog switches and use a large number of resistors and requires relatively large supply voltages. This paper presents alternative current-mode analog implementations of the digital logic functions. Using, no resistors, except for realizing constant

current-sources, no switches, no operational amplifiers, and only a small number of transistors, the proposed implementations requires low supply voltages and are very attractive for integration. The proposed implementation is designed for CMOS technology, which is now the most preferable technology for integrated circuit fabrication.

III. CIRCUIT DESCRIPTION

Fig.1 shows Low-Voltage Current-Mode Realization of Digital Logic Gates using CMOS. We will use this circuit to realize the Digital Logic Gates. MOS transistors M_1–M_7 form a set of current mirrors for the input current Ix, and MOS transistors M_8–M_{17} form a set of current mirrors for the input current Iy. MOS transistors M_{18}–M_{22} form current mirrors for the drain current of MOS transistor M_{18}. MOS transistors (M_{25}–M_{26}) form current mirrors for the sum of drain current of MOS transistor M_4 and M_{14}. MOS transistors (M_{23}–M_{24}) form current mirrors for the subtraction of drain current of MOS transistor M_3 and M_{10}.

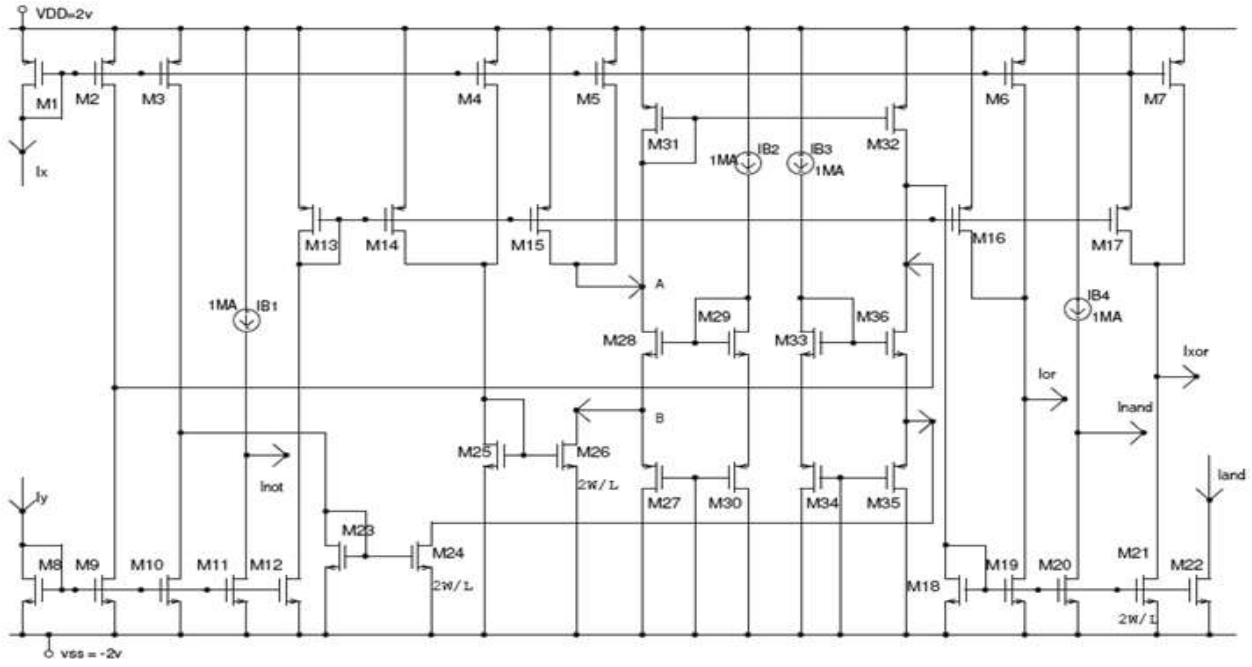

Figure 1. Proposed implementation of the NOT/OR/NAND/XOR /AND digital logic functions using analog techniques.

The circuit consists of a dual translinear loop (M_{27}-M_{30}). The drain-to-source current (I_{DS}) of an MOS transistor operated in the saturation region is given by

$$I_{DS} = K(V_{GS} - V_t)^2 \qquad (6)$$

$$V_{GS} = V_t + (I_{DS}/K)^{1/2} \qquad (7)$$

Where

$K=0.5\mu_0 C_{OX}(W/L)$ is transconductance parameter of transistor, μ_0 is the electron mobility, C_{OX} is the gate oxide capacitance per unit area, W/L is the transistor aspect ratio, V_{GS} is the gate-to-source voltages and V_t is threshold voltage of the MOS transistor. Consider a I[st] loop of MOS transistor M_{27}-M_{30}; summing the gate–source voltages around the loop gives [13]:

$$V_{GS28} + V_{GS27} = V_{GS30} + V_{GS29} \quad (8)$$

Transistors M_{27}-M_{30} form a dual translinear loop in Fig. 1. They are biased in saturation region and are well matched and have the same transconductance value, that is $K_N=K_P$. Then using (6) and (7) and considering $I_{DS29} = I_{DS30} = I_B$, we have

$$(I_{DS30})^{1/2}+(I_{DS29})^{1/2}=(I_{DS27})^{1/2}+(I_{DS28})^{1/2} \quad (9)$$

$$2(I_B)^{1/2} = (I_{DS22})^{1/2} + (I_{DS28})^{1/2} \quad (10)$$

Writing KCL at nodes A and B

$$I_{DS28} = I_{out1} + (I_x+I_y) \quad (11)$$

$$I_{DS27} = I_{out1} - (I_x+I_y) \quad (12)$$

Substituting (11) and (12) in (10) and squaring both sides

$$4I_B = (I_x + I_y)+I_{out1} + I_{out1} -(I_x + I_y) +2\{I^2_{out1} - (I_x+I_y)^2\}^{1/2} \quad (13)$$

Eliminating $(I_x+ I_y)$ and squaring both sides again

$$16I^2_B - 16I_BI_{out1}+ 4I^2_{out1} = 4I^2_{out1}- 4(I_x + I_y)^2 \quad (14)$$

The output current I_{out} of the circuit in Fig. 1 can be written as

$$I_{out1} = \{(I_x + I_y)^2 /4I_B + I_B\} \quad (15)$$

Similarly the second loop (M_{33} – M_{36}) provides a $(I_x - I_y)$ input function to the squarer function $(I_x - I_y)^2$

$$I_{out2} = \{(I_x - I_y)^2 /4I_B + I_B\} \quad (16)$$

$$I_{out} = I_{out1} - I_{out2} \quad (17)$$

Substituting (15) and (16) into (17) results in

$$I_{out} =(I_x*I_y)/I_B \quad (18)$$

it is easy to show that the drain current of MOS transistor M_{18} can be expressed as

$$I_{DM18} = (I_x * I_y)/I_B \quad (19)$$

With the aspect ratio of MOS transistor M_{21} equal to twice the aspect ratio of MOS transistor M_{20} the drain current in MOS transistor M_{21} can be expressed as

$$I_{DM21} = 2\, I_{DM20} = 2(I_x * I_y)/I_B \quad (20)$$

Using Eqs. (19) and (20) it is easy to verify that the output currents INOT, IAND,IOR, INAND and IXOR realize the logic functions NOT, AND,OR, NAND and XOR given by Eqs. (1)–(5). Realization of the logic functions NOR and XNOR is a straightforward extension of the implementations of Figure 1.

IV. SIMULATION RESULTS

The performance of Low-Voltage Current-Mode Realization of Digital Logic Gates using CMOS circuit as shown in Fig.1 are simulated using PSPICE simulator. The transistors aspect ratios as given in Table II and the supply voltage are VDD=-VSS=2V, I_B is set to 1MA. The results obtained from the NOT, AND, OR, NAND and XOR operations are shown in Figure 2. In Figure 2 the currents are sensed using 1 kΩ load resistances. The results obtained are in excellent agreement with the theory presented in equations (1)-(20).

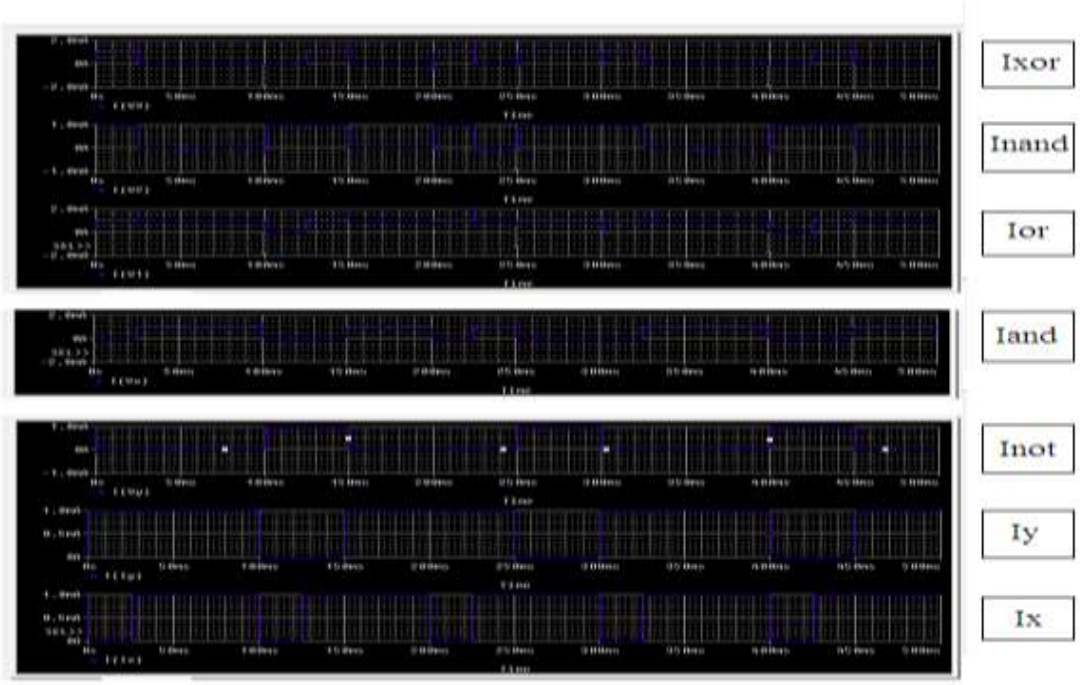

Figure 2. Results obtained from the proposed circuit of Fig. 1 with DC supply voltage=±2V.

V. CONCLUSION

We have seen that logic function can be expressed as power series expansion. Power series expression are used to implement basic logic function with the help of current sources, translinear circuit, add and subtract, current mode technique is used to implement logic gates such as NOT, AND, OR, NAND and XOR. All the simulation are done in PSPICE. Power supply of ±2 volt is used. The proposed circuit can be used for high package density and low power consumption in integrated circuits.

This circuit can be used as a basic building block. These sub-circuit may be used to design various integrate analog circuits (such as modulator, decoder etc) for faster response.

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