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# IMPLEMENTATION OF DDR I SDRAM MEMORY CONTROLLER USING ACTEL FPGA

**Vivek V S[1], Preethi R[2], Nischal M N[3], Monisha Priya G[4] , Pratima A[5]**

[1,2,3,4,5] *School of Electronics and Communication, REVA university,(INDIA)*

## ABSTRACT

*The efficient memory controller plays a very important role in developing high end application , where it doesn't contain microprocessors. Command signals for memory refresh, read and write operation and SDRAM initialisation has been provided by memory controller. The work will mainly focus on FPGA implementation of Double Data Rate(DDR) SDRAM controller .The DDR SDRAM controller is placed in between the DDR SDRAM and bus master. The operation of DDR SDRAM controller is to simplify the SDRAM command interface to standard system read/write cycle. The proposed design will offer dedicated power utilisation , reduce the gate count, reduce the area of chip and improves the speed of the system by reducing the gates. The proposed design is implemented on Actel FPGA platform.*

***Keywords:*** *Burst access, DDR SDRAM, FPGA (Field Programmable Gate Arrays), SDR, VHDL.*

## I. INTRODUCTION

Single data rate (SDR) SDRAM (Synchronous Dynamic Random Access Memory) drives/latches the data and command information on the rising edge of the synchronous clock. DDR SDRAM is a type of SDRAM that inherits technologies from SDR SDRAM and realizes faster operation and lower power consumption. DDR SDRAM most commonly used in various embedded application like signal processing, networking, image/video processing etc which require cheap and fast memory. DDR SDRAM was the initial development of SDRAM memory technology , to improve its performance. DDR SDRAM utilises various techniques including very tight timing controls , to increase the data transfer rates by almost a fact of two[1][2]. The very tight timing requirements often require the use of phase locked loops and self-calibration techniques to ensure the timing is sufficiently accurate.

DDR SDRAM achieves a data transfer rate that is twice the clock frequency by employing 2-n bit prefetch architecture [3]. In this architecture, 2n bits of data are transferred from the memory cell array to the I/O buffer every clock. Data transferred to the I/O buffer is output of n bits at a time , for every half clock (both rising and falling edges of the clock (CK). The proposed memory controller and CoreDDR is used to interface memory to rest of the embedded system design. CoreDDR provides a high-performance interface to double data rate (DDR). CoreDDR accepts read and write commands using the simple local bus interface and translates this request to the command sequences required by SDRAM devices. It also performs all initialization and refresh

functions using memory controller. This Memory controller design has been implemented in VHDL. The focus of this work is to design and implement DDR SDRAM controller which provides memory interface between the DDR SDRAM memory module and main embedded system.

## II. LITERATURE REVIEW

Advanced operating systems, like Windows, started the RAM era . The PCs that were used, required high capacity of RAM ,for implementing various kinds of operations . The first Windows operated PCs could address 2 MB RAM, but 4 MB soon became standardized .The development has continued through the 90s, as RAM prices have dropped dramatically. Today no PC is less than 32 MB RAM . From the original SDRAM, further generations of DDR (or DDR1) and DDR2 and then DDR3 emerged, with DDR4 currently being designed and anticipated to be available in 2012. Although the concept of synchronous DRAM was primitive,it was used in early Intel processors, it was only in 1993 that SDRAM began its path to universal acceptance in the electronics industry. In 1993, Samsung introduced its KM48SL2000 synchronous DRAM, and by 2000, SDRAM had replaced virtually all other types of DRAM in modern computers, because of its greater performance. SDRAM latency is not inherently lower (faster) than asynchronous DRAM[4]. Indeed, early SDRAM was somewhat slower than contemporaneous burst EDO DRAM due to the additional logic. The benefits of SDRAM's internal buffering come from its ability to interleave operations to multiple banks of memory, thereby increasing effective bandwidth[5].

## III. FUNCTIONAL DESCRIPTION

*3.1 Description of DDR*

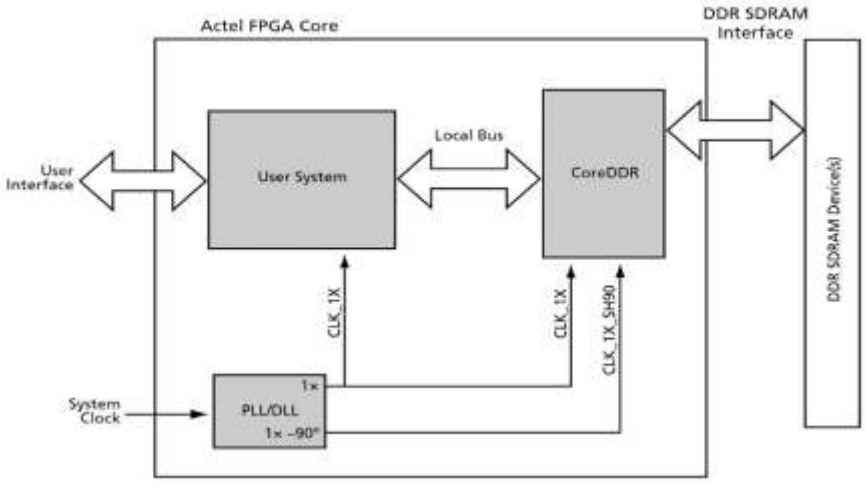



FIG 1. BLOCK DIAGRAM OF CORE DDR SYSTEM

Double data rate(DDR) is advanced version of dynamic random access memory (SDRAM). SDRAM waits for a clock signal before responding to control input. DDR uses both raising and falling edge of the clock signal. The main difference between DDR SDRAM is how many times data is transmitted within each cycle. DDR

transfers data twice per clock cycle whereas SDRAM sends signals once per clock cycle , but same frequencies are used by both DDR and SDRAM.

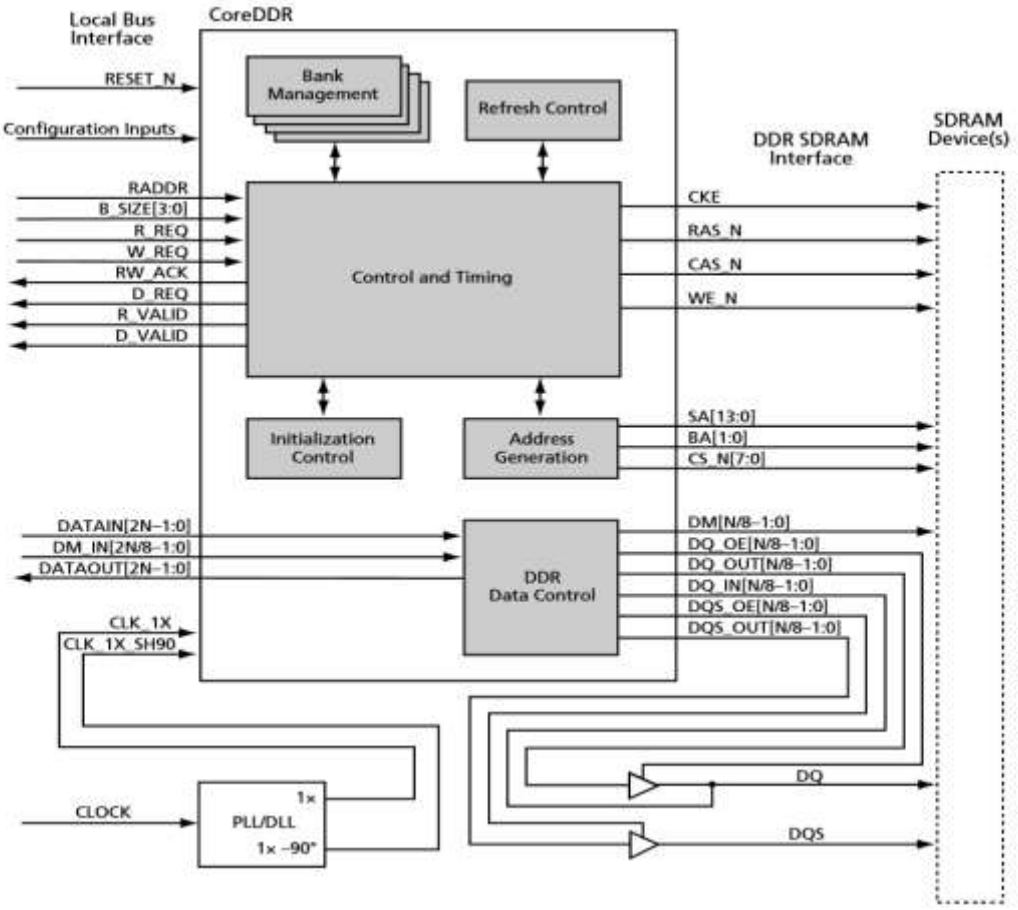


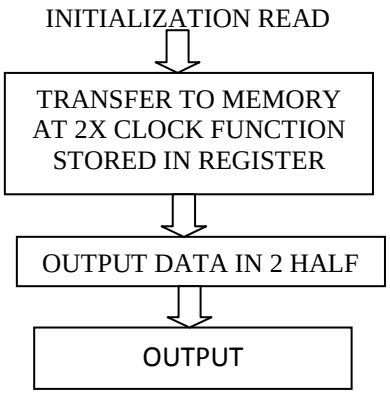

FIG 2. DDR SDRAM CONTROLLER BLOCK DIAGRAM

*3.1 Description of DDR SDRAM*

The DDR SDRAM uses double data rate architecture to achieve high speed data transfer. DDR SD RAM transfers data on both falling and raising edge of the clock cycle. This DDR controller is implemented in a system between DDR and bus master[5]. DDR center keeps up a data base of all banks actuated and also lines enacted in every bank. This data , which the DDR SDRAM controller selects dynamic or pre-charge command if it is required . This inactivity of read /write commands are then issued to the DDR SDRAM. DDR SDRAM controller deals with initiating / pre-charging the banks, as user needs to provide read/write command.

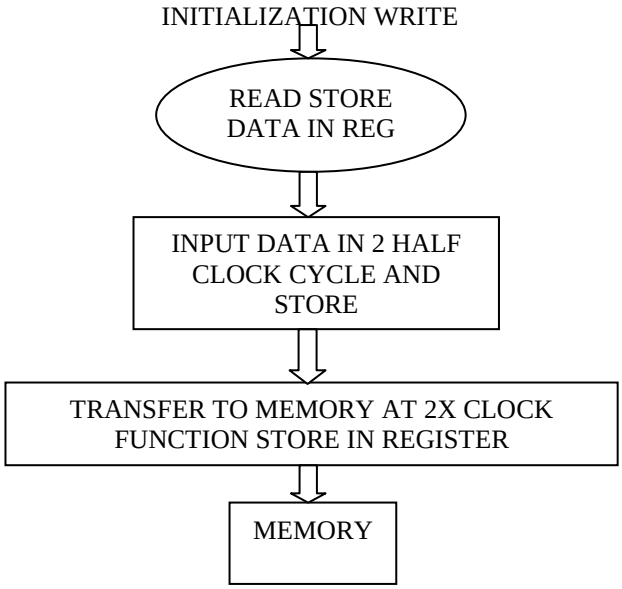
*3.1.1 Read operation in DDR SDRAM*

The Flowchart explains read operations in DDR SDRAM .When data is initialized in read operation data is read from memory at 2x clock cycle, ensures that the data is read at both the half cycles, This intimates data is extracted at high speed in memory.




*3.1.2 Write operation in DDR SDRAM*

When the write command is initialized, the data is first read and stored in temporary register .When a clock cycle occurs, the data from input side is sent to the memory in second half clock cycle which then gets stored in the memory[6]. The data is not written to the memory directly but it is stored in the register and then transferred to the memory.




## IV. CONCLUSION

In this paper an effective functional DDR SDRAM is implemented. The controller generates different types of control and timing signals, which synchronous the timing and control the flow of the operation. The memory system operates at double data rate frequency of processor without affecting the performance The proposed DDR controller is implemented with 1Gb DDR SDRAM. It is a high speed CMOS dynamic random access

memory containing 1,073,741,821 bits. It is internally configured as a 4 bank DRAM. The proposed design is modelled in VHDL and then simulated in FPGA.

## REFERENCES

[1]. **General DDR SDRAM Functionality Micron** Technology Micron Technology, Inc., reserves the right to change products or specifications without notice 2003 Micron Technology, Inc. All rights reserved.

[2]. **1Gb: x4, x8, x16 DDR SDRAM Micron**. Micron Technology, Inc., reserves the right to change products or specifications without notice 2003 Micron Technology, Inc. All rights reserved.

[3]. **Burchardt, A., Hekstra-Nowacka, E., and Chauhan, A**.,"A Real-time Streaming Memory Controller", Design, Automation and Test in Europe 2005 Proceedings, 2005, vol.3, pp. 20-25.

[4]. **Heithecker, S. and Ernst, R.**, "Traffic Shaping for An FPGA Based SDRAM Controller with Complex QoS Requirements", Design Automation Conference 2005,June 2005, pp. 575-578.

[5]. **ALTERA, DDR SDRAM Controller** White Paper, Ver1.1, 2002.

[6]. **Guo Li, Zhang Ying, Li Ning, and Guo Yang,** "TheFeature of DDR SDRAM and the Implementation of DDR SDRAM Controllers via VHDL", The Journal of China Universities of Posts and Telecommunications, 2002, vol.9,no. 1, pp. 61-65.