International Journal of Advance Research in Science and Engineering
Volume No.07, Special Issue No.04, March 2018
www.ijarse.com
IJARSE
ISSN: 2319-8354

High performance Hetero Gate Schottky Barrier MOSFET

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ABSTRACT

In this paper, we propose a new high performance hetero gate material Schottky barrier MOSFET. The proposed device consists of two gate metal workfunctions, two different oxides and the device is being named as Hetero gate Schottky Barrier MOSFET (HG-SBMOSFET). In the proposed device, Source and Drain regions consists of metal silicides (Nickel Silicide (NiSi)), gate metal consists of two different metal work-functions (4.72eV and 3.9eV) and dual oxide (silicon dioxide (SiO_2) and Hafnium dioxide (HfO_2)) has been used as a gate oxide. The use of HfO_2 and metal work-function 3.9eV(Hafnium) serves as tunneling gate and SiO_2 and 4.65eV acts main gate for the proposed device. A 2D simulation study have shown significant improvement in various performance measuring parameters in proposed device in comparison to conventional Schottky Barrier MOSFET (SB-MOSFET). It has been observed that ON current, ON/OFF ratio, Subthreshold Swing (SS) and Transconductance (g_m) shows significantly improved performance in comparison to conventional SB-MOSFET.

Key words: MOSFET, Dual oxide, metal workfunctions, Schottky Barrier

I.INTRODUCTION

The scaling of MOS device dimensions has reached to its limits. The scaling of device dimensions till now has resulted in increased speed, high density ICs, chips with increased functionality, and reduced cost [1-2]. However, decrease in MOS dimensions below 22/32nm technology node is very difficult due to short channel effects, gate tunneling, parasitic effects, channel transport limitations, increase in source/drain series resistance etc [3]. One of the challenging issue for realizing the Nano devices is the increase in source/drain resistance with decrease in silicon film thickness. The increase in Source/Drain resistance can be addressed by raised Source/Drain technique, increasing the area of Source/Drain region or by increasing the doping of the Source/Drain region. However, the above mentioned solution leads to the fabrication process complexity. In order to address high Source/Drain resistance issue a novel technique of metal (or metal silicide's) source drain technique has been presented in literature [4-7]. Metal source/drain devices are planner in nature, act as highly abrupt junctions, reduces the source/ drain resistance and such type of devices possess least process variation

effects and can fabricated at low temperatures [8-9]. However, the main problem with these type of devices is there low on state performance due Schottky barrier height at metal semiconductor junction.

In this paper, we present a new structure of Schottky Barrier MOSFET (SB-MOSFET) having Dual gate metal and Dual gate oxide. The use of dual metal and dual oxide in the proposed device gives the name of the device as hetero gate Schottky Barrier MOSFET (HG-SB-MOSFET). In the proposed device two types of gate metal workfunction have been used are 3.9eV, 4.65eV and dual oxide dielectric is employed to improve the performance of the proposed device. Thus in the proposed device, the single gate structure is divided into two parts one act as tunnel gate (TG) and other act as main gate (MG). The TG act as performance booster for the proposed device, as it increases the electric field at the source metal and channel interface which is responsible for reducing the tunneling width and increases the tunneling rate [10-12]. The increase in tunneling rate improves the ON state performance of the proposed device.

The paper is divided into four sections. Section II discusses various device structures studied in this work. Various results and discussion are discussed in Section III. The work is concluded in Section IV.

II.DEVICE STRUCTURES

The schematic cross sectional views of conventional SB-MOSFET and Proposed Hetero Gate SB-MOSFET devices are shown in Figure 1. A single gate geometry is considered with gate length (L_G=50nm), gate oxide (T_{OX1}=2nm), silicon film thickness (T_{Si}=10nm) and gate metal work-function of 4.65eV has been used. The proposed device consists of dual oxide (silicon dioxide and Hafnium Oxide) and Dual metal with workfunction 4.65eV and 3.9eV. In the proposed device Hafnium oxide (HfO_2) and metal workfunction 3.9eV form one part of gate and named as tunnel gate (T-Gate) and other part of the gate consists of silicon dioxide (SiO_2) and metal workfunction 4.65eV named as main gate (M-gate).

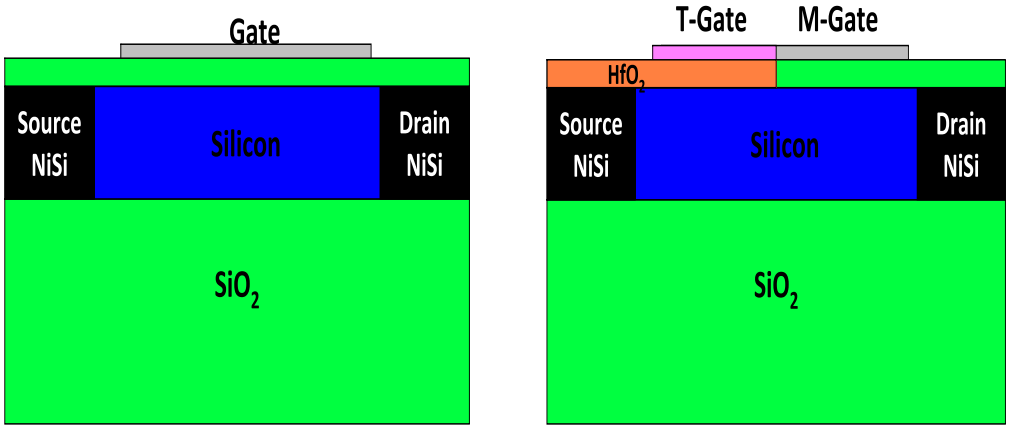
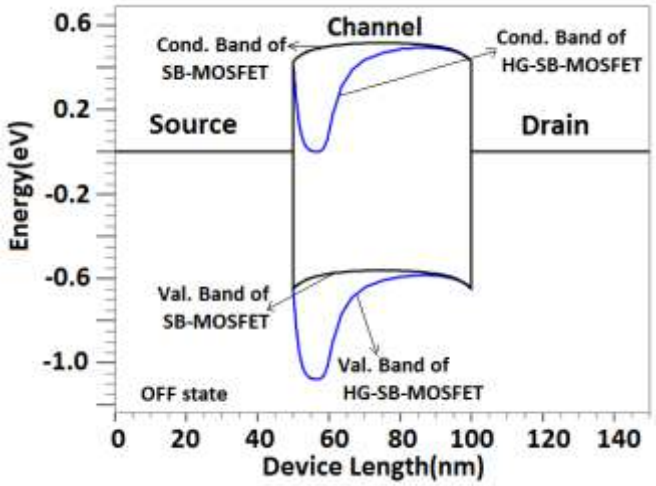


Figure 1: Schematics of (a) conventional SB-MOSFET (b) Proposed Hetero Gate SB-MOSFET

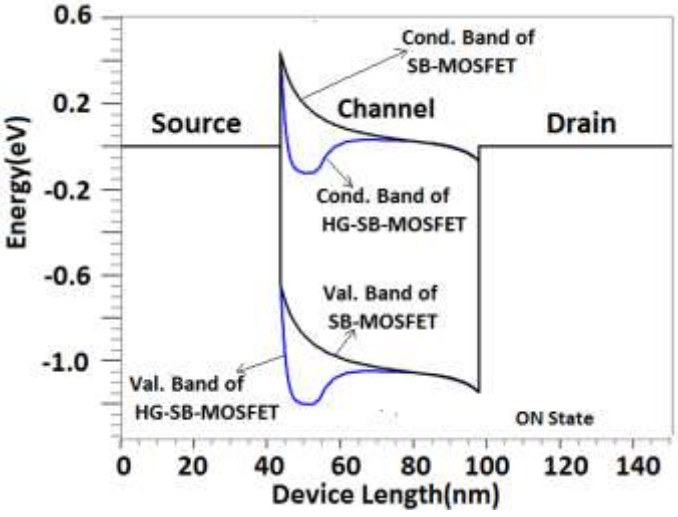
The use of T-gate modulates the barrier and increases the performance of the proposed device, while main gate controls the other part of the channel. Besides this, Drain and Source regions are made of Nickel Silicide (NiSi) for proposed and conventional device.

III.RESULTS AND DISCUSSION

Atlas device simulator [13] has been used for monitoring the performance of conventional SBMOSFET and Hetero Gate SB-MOSFET. The different models have been activated in simulation for better comparison are *drift diffusion, fldmob, conmob, srh, fermi, consrh, BGN and ust.* The use of conmob and fldmob takes into account the concentration dependent and field dependent mobilities respectively. Drift diffusion model is mainly responsible for carrier transport in the channel. Universal Schottky tunneling (UST) model has been used in the simulation in order to capture tunneling across the metal semiconductor junction. Figure 2 shows the energy band diagram in ON and OFF state of the HG-SBMOSFET and conventional SB-MOSFET.



(a)



(b)

Figure 2: Band diagram of conventional SB-MOSFET and the proposed Hetero SB-MOSFET in (a) OFF state (b) ON state

It has been observed that due tunnel gate in the proposed device, the tunneling width gets narrower in comparison conventional SB-MOSFET. This band bending is responsible for higher drive current in the proposed device in comparison to conventional device.

The transfer characteristics of two devices are shown in Figure 3. The OFF current (I_{OFF}) is calculated for V_{GS} = 0V and V_{DS} = 0.5V, is of the order of ~ 4×10^{-10} A/ µm in the proposed device. The ON current (I_{ON}), calculated for V_{GS} = 0.5V and V_{DS} = 0.5V, is of the order of ~ 3.75×10^{-5} A/ µm in the proposed device. It has been observed that the I_{ON} and I_{ON}/I_{OFF} ratio in the proposed HG-SB-MOSFET device has increased by ~400 times and ~10 times respectively in comparison to Conventional SB-MOSFET (I_{ON}= 1×10^{-7}A/µm, I_{OFF} = 2×10^{-11} A/ µm). Further, it clearly seen from Figure 3 that their huge improvement in Transconductance and Subthreshold slope in the proposed device in comparison to conventional device.

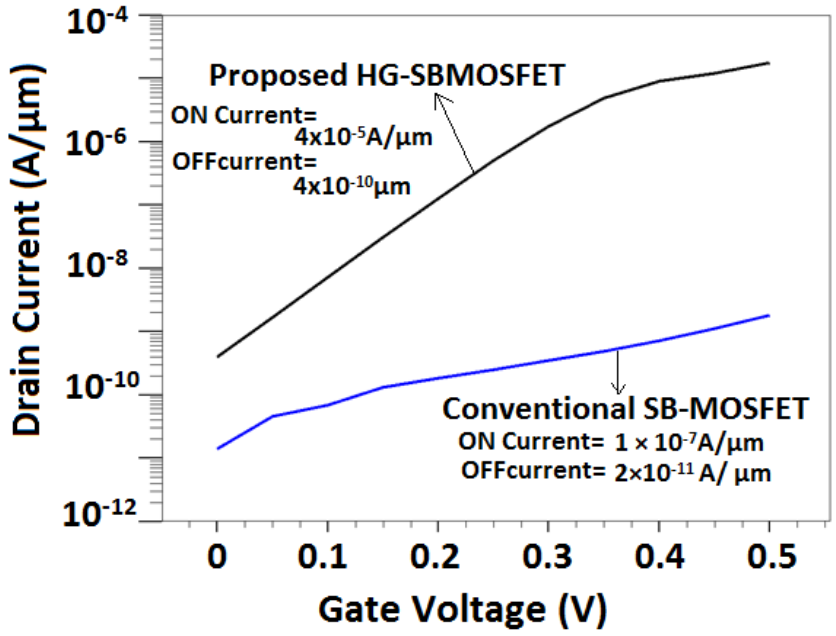


Figure 3: Transfer Characteristics of conventional SB-MOSFET and Proposed HG-SB-MOSFET

The high driving capability of the proposed device can attribute to Tunnel gate which modulates the tunneling width between metal source and channel by using the combined low metal workfunction material and high K dielectric HfO_2. The tunnel gate (TG) increases the electric field and electron concentration on the channel, the increase in electric field and increase in electron concentration in the channel is responsible for improved performance of the proposed HG-SB-MOSFET. Figure 4 show the electric strength inside the proposed and conventional devices.

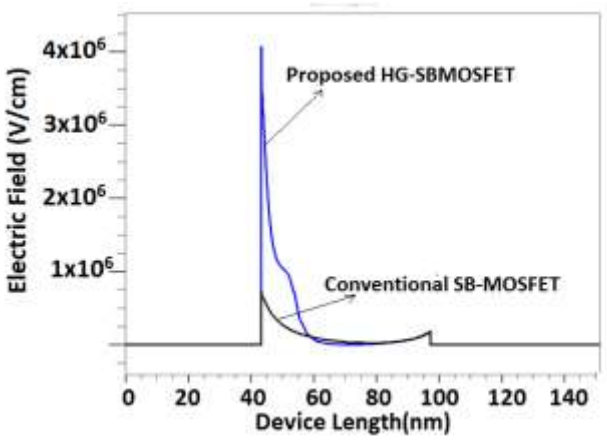


Figure 4: Electric Strength inside the proposed and conventional SB-MOSFET

Figure 5 shows the concentration of electrons in the channel of the proposed and conventional devices, it is clear that higher electron concentration is observed in the proposed, which results in lower resistance for the proposed during the conduction process and results in higher driving capability.

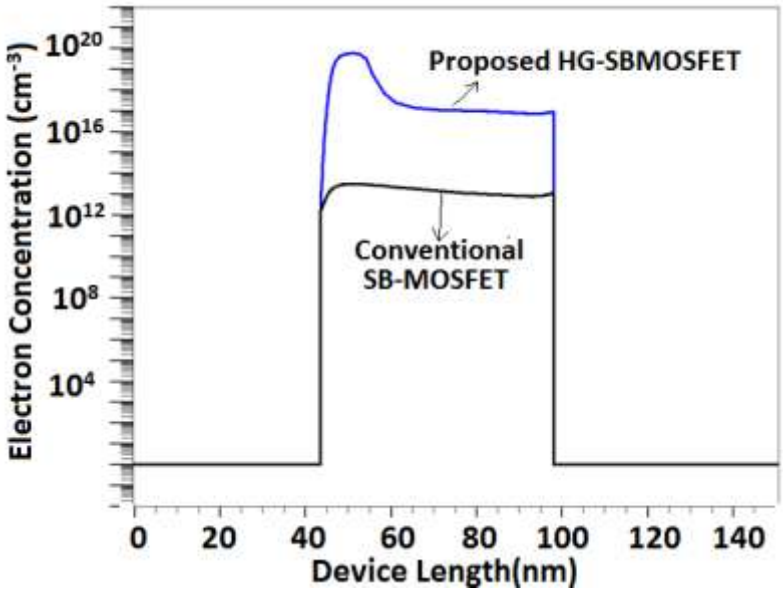


Figure 5: Electron Concentration in channel of the proposed and convention SB-MOSFET in ON state

IV.CONCLUSION

In this study, a new hetero gate Schottky Barrier MOSFET have been designed and simulated. The proposed consists of Nickel Silicide material for Source/Drain regions, two different gate metals and dual gate oxide have been used in order to improve the performance of the proposed device. The proposed device shows significant improvement in various performance measuring parameters in comparison to conventional SB-MOSFET. It has

been observed that the HG-SB-MOSFET not only possess advantages of conventional SB-MOSFET, but it outperforms the conventional SB-MOSFET in various performance measuring parameters.

REFERENCES

[1] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, Oct. 1974.

[2] T. Skotnicki, J. A. Hutchby, T.-J. King, H.-S. P. Wong, and F. Boeuf, "The end of CMOS scaling: Toward the introduction of new materials and structural changes to improve MOSFET performance," *IEEE Circuits Devices Mag.*, vol. 21, no. 1, pp. 16–26, Jan./Feb. 2005.

[3] S. A. Loan, S. Qureshi, and S. S. K. Iyer, "A novel partial-groundplane based MOSFET on selective buried oxide: 2-D simulation study," *IEEE Trans. Electron Devices*, vol. 57, no. 3, pp. 671–680, Mar. 2010.

[4] J. M. Larson and J. P. Snyder, "Overview and status of metal S/D Schottky-barrier MOSFET technology," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1048–1058, May 2006.

[5] M. Östling, J. Luo, V. Gudmundsson, P.-E. Hellström, and B. G. Malm, "Nanoscaling of MOSFETs and the implementation of Schottky barrier S/D contacts," in *Proc. 27th Int. Conf. Microelectron. (MIEL)*, Niš, Serbia, 2010, pp. 9–13.

[6] F. Bashir, S. A. Loan, M. Rafat, A. R. M. Alamoud, and S. A. Abbasi, "A high-performance source engineered charge plasma-based Schottky MOSFET on SOI," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3357–3364, Oct. 2015.

[7] J. P. Snyder, "The physics and technology of platinum silicide source and drain field effect transistors," Ph.D. dissertation, Stanford Univ., Stanford, CA, USA, 1997.

[8] M. Östling, J. Luo, V. Gudmundsson, P.-E. Hellström, and B. G. Malm, "Nanoscaling of MOSFETs and the implementation of Schottky barrier S/D contacts," in Proc. 27th Int. Conf. Microelectron. (MIEL), Niš, Serbia, 2010, pp. 9–13.

[9] G. Larrieu, D. A. Yarekha, E. Dubois, N. Breil, and O. Faynot, "Arsenic-segregated rare-earth silicide junctions: Reduction of Schottky barrier and integration in metallic n-MOSFETs on SOI," IEEE Electron Device Lett., vol. 30, no. 12, pp. 1266–1268, Dec. 2009.

[10] FAISAL BASHIR, A G. ALHARBI, S A. LOAN, "Electrostatically Doped DSL Schottky Barrier MOSFET on SOI for Low Power Applications" IEEE journal of Electron Device Society VOLUME 6, 2018, pp 19-25.

[11] F. Bashir, S. A. Loan, M. Rafat, A. R. M. Alamoud, and S. A. Abbasi, "A high performance gate engineered charge plasma based tunnel field effect transistor," J. Comput. Electron., vol. 14, no. 2, pp. 477–485, 2015.

[12] Faisal Bashir, S A. Loan, M. Rafat, A M Murshid, A M. Alamoud, "Charge plasma based partial-ground-plane-MOSFET on selective buried oxide (SELBOX) proceeding in IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2016 IEEE.

[13] ATLAS, ATLAS Device Simulation Software, Silvaco Int., Santa Clara, CA, USA, 2012.