

IMPLEMENTATION AND DESIGN OF SR FLIP FLOP USING ADIABATIC TECHNIQUE

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ABSTRACT

The electronic circuits are comprised of a number of transistors which exhibit the power dissipation due to which performance of the circuits was effected. The immoderate power reduces reliability, which elevates the cost of cooling system and packaging. As, with the furtherance of electronic circuits which are dealing with the digital circuitry are implemented with the use of CMOS technology. The power loss can further reduce by the use of Adiabatic Technology. In this paper, the sequential circuit (SR flip flop) is implemented with the use of two adiabatic technologies which are Efficient Recovery Charge Logic (ECRL) and Diode Free Adiabatic Logic (DFAL).

Keywords— Adiabatic Technique, Power dissipation, SR flip flop, ECRL, DFAL

1.INTRODUCTION

In today's breakthrough world, power reduction is the prime concern for the designers and researchers have increased their endeavour in interpretation for its sources and reduce its impact. The average power dissipation in the CMOS circuits can be described by the following equation.

$$P_{avg} = P_{dynamic} + P_{short} + P_{leakage} + P_{static} \quad (1)$$

Dynamic power consumption, $P_{dynamic}$ is defined as the power consumed during output switching of CMOS gate. When transition at the input causes a change in the conductive state of the pull up and pull down network, electric charge is transferred from the power supply to the output capacitance C_{out} or output capacitance to ground [1,2]. This type of transition causes power dissipation in pull up and pull down network.

$$P_{dynamic} = K * C_{out} * V_{dd}^2 * f \quad (2)$$

When input transit time is larger than 0, the pull up and pull down are both on for short period of time. During this time, there is connection between power and ground and some current is drawn from supply and flows directly to ground, this is called short circuit current. Leakage power is mainly due to diode leakage and sub threshold leakage current of transistors and static power is caused by DC current flow from V_{dd} to GND when pull up and pull down are both conducting and gate output is not transitioning. For scaling down the power losses in the circuits, the revolutionary approach is followed i.e, adiabatic techniques.

II. ADIABATIC TECHNIQUE

The adiabatic techniques profound the energy saving mechanisms to the logic circuits by recycling or reuse the energy. It refers to the process in which transition occurs without power either loss or gain in the system environment which is termed as thermodynamics [3]. So, the energy losses in the adiabatic logics are very less as compared to the conventional circuits. In real time systems, such as ideal circuitry is not possible as it contains resistive elements. There are some classical approaches for CMOS circuits to minimize the power losses such as voltage scaling, decreasing physical capacitance and reduces the switching activity. The compositions of all the factors originate the complications such as weight, lifetime of the battery and size [5]. The adiabatic logic deals with the switching activity which is possible to diminish the effect of power by giving back the stored energy to the supply [7].

This adiabatic technique exerts on the charge recovery logic as the charge from the circuit is successfully transferred from one point to another without any energy dissipation. This charging and discharging phenomenon is termed as adiabatic switching. When the circuits are implemented by the use of adiabatic postulates then the changes occurs with a very slow rate, which caused the system to dissipate the less energy.

A. Efficient Charge Recovery Logic (ECRL)

In this type of adiabatic logic, the two pairs of pull down and pull up network is used which uses only NMOS and it also uses the two pairs of PMOS transistors which are in cross coupling manner to each other. This type of connection helps the circuit in pre charge and evaluation. These operations are the main part of the efficient Charge Recovery Logic. The NMOS pull up network is inverted of the NMOS pull down network. In the ECRL, sometime it uses undesired power when it is operating in two phase clock because the value at the previous stage may affect the value at the next stage. So, for clocking system is recommended in the ECRL logic families because values of preserved in the hold stage and used as the input for evaluation of next stage. These types of circuits may experience the coupling effect as the PMOS are connected in that manner. The basic implementation of the ECRL logic is shown in the Fig. 1.1.

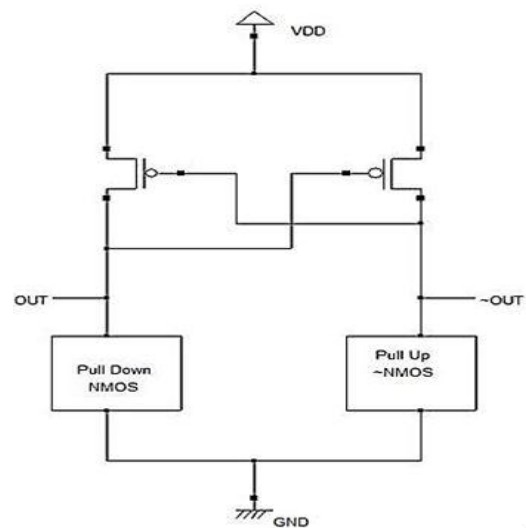


Fig.1.1. Basic ECRL Structure

B. Diode Free Adiabatic logic(DFAL)

In this type of adiabatic logic, the circuits are free from diode which means that its charging and discharging path is free from the diode effects. It is identical to the static CMOS circuits except that another NMOS is used below the pull down network, which is used to eliminate the diode for discharging. As, the main power dissipation observed in the discharging path at the diode due to threshold voltage drop.

The additional NMOS transistor is used to recycle the charges from the circuit. The power losses are not completely eliminated in the logic, but the performances of this circuit compared with the diode based adiabatic techniques are superior. The basic logic can be shown by the Fig. 1.2.

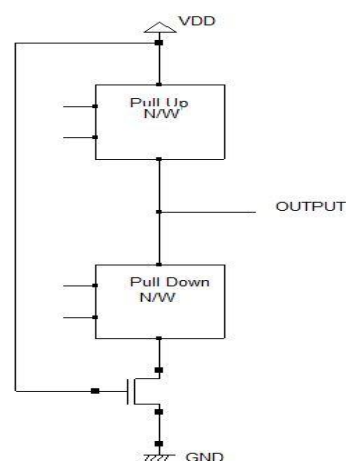


Fig. 1.2. Basic DFAL Structure

III. CMOS SEQUENTIAL CIRCUIT

The sequential circuit is defined as the circuits in which output is not only depends upon its present state but also depends on the sequence of the past outputs. It is the basic building block of digital circuitry, as they are the combination of sequential and combination circuit.

The sequential circuit are of two types: synchronous and asynchronous. The synchronous sequential circuits are capable to change its output at the discrete time interval according to the clock signal and asynchronous sequential circuits are capable to change its output at any instant of time without in accordance with the clock signal.

A. S R Flip Flop

Flip Flop is the sequential circuit which can able to change its input and gives it output in accordance with the instant of time. It is considered as the edge triggered device. The SR Flip Flop can be implemented in the using clocked and unclocked form of structure. In the unclocked flip flop circuits, the clock pulse is not used as the input does not depend upon the clock. The state of the flip flop settles after the input change.

The flip flop can be designed by the use of NOR and NAND gate. This device is considered as the 1-bit memory device, since it is able to store the pulse when another bit is in execution.

The basic unclocked SR flip flop using NAND gate is shown in the Fig. 2.1. The complication with simple flip flop is that they are level sensitive to the control signal. With due reason of this, the circuit becomes a transparent device.

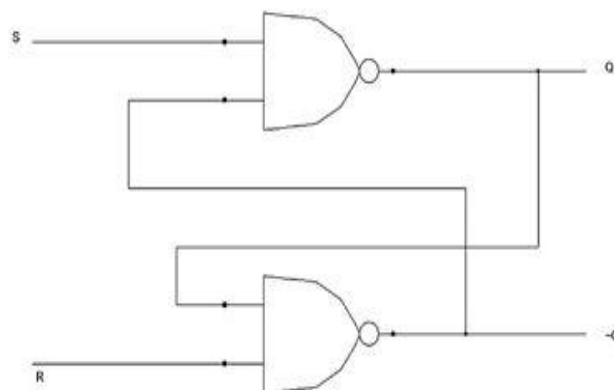


Fig. 2.1. Basic unclocked SR Flip Flop

The operation of the unclocked SR flip flop varies as Set and Reset condition. Initially, when the $S=1$ and $R=0$ then the flip flop is in set condition as the $(\sim Q)=1$ and when both input terminals will become 1 then it will not

change its output. The other condition is Reset which is present when $S=0$ and $R=1$ then $\sim Q$ will reset to 0 and further any change to the input terminal, it will not change. The operation summarizes in the Table I.

TABLE I Truth Table of unlocked SR Flip Flop

State	S	R	Q	$\sim Q$	Description
Set	1	0	0	1	Set $\sim Q=1$
	1	1	0	1	No change
Reset	0	1	1	0	Reset $Q=0$
	1	1	1	0	No change
Invalid	0	0	1	1	Invalid condition

The improved version of this circuit is clocked SR flip flop which uses the pair of NAND gate and one of its inputs is clocked as shown in Fig. 2.2. The circuit can be implemented by the use of the AND gate as the operation is same when the clock is high, but when the clock is low the output state will be in no change state.

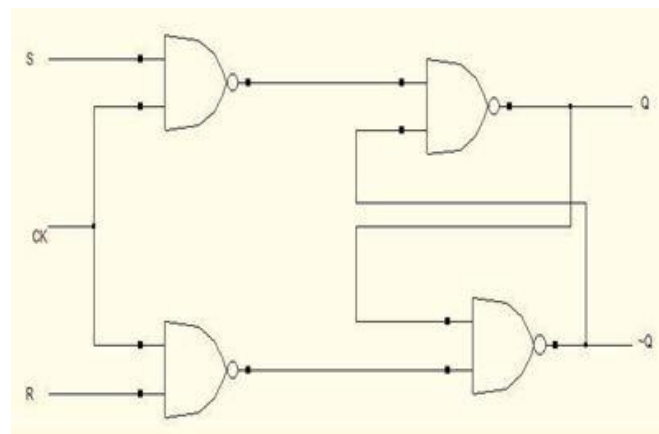


Fig. 2.2. Basic clocked SR flip flop

In the figure, the circuit is implemented by the use of a NAND gate. This circuit is working in a similar way except that the inputs are active high and the invalid condition exists when both its inputs are at logic level 1. This clocked circuit is modified to avoid the circuit oscillations due to some discrete events. The real flip flop would enter a random state based on the current operating parameters like temperature etc. As, the circuit is controlled by the clock signal, such type of flip flops are called as level sensitive.

Hence, we obtained that the transition of the clock signal is the key functioning of the device. This clocked version of the SR flip flop eliminates some of the problems. It allows the circuit to better control of the latching action which is not able for the basic SR flip flop.

The operation of the clocked SR flip flop that output can only change its state while CK input is logic 1 and, when the CK is logic 0, the S and R inputs will have no effect. For the truth table of clocked SR flip flop is shown in the Table II.

TABLE II Truth Table of clocked SR Flip Flop

Inputs			Output	State
CK	S	R	Q	
X	0	0	No change	Previous
HIGH	0	1	0	Reset
HIGH	1	0	1	Set
HIGH	1	1	-	Forbidden

IV. ADIABATIC SEQUENTIAL CIRCUIT

The basic sequential circuits are capable to perform as accordance with the requirement, but the problem of energy dissipation is still adjacent to the designing of the circuit. The two types of circuit are implemented which is used to charge and discharge the output capacitance. This process is able to shield the energy store at the output and redeem the energy at the power supply which can again use by the circuit. This is not possible in the conventional form of the sequential circuit. So, the refinement is build and abolishes the inducement of the energy dissipation. The circuits can be implemented with the help of two adiabatic logics: ECRL and DFAL.

A. ECRL SR Flip Flop

This adiabatic logic requires two PMOS which are connected in the crossed manner. The pull up network is connected on the one side as the inverted manner with the help of the NMOS and the pull down network is connected to the other side as the non-inverted manner. The design of the SR flip Flop with ECRL technique is shown in the Fig. 3.1.

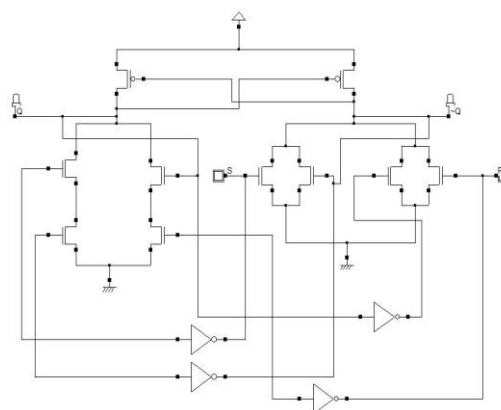


Fig. 3.1. ECRL SR Flip Flop

B. DFAL SR Flip Flop

This adiabatic logic is same as the usual CMOS circuit besides the auxiliary NMOS is used below the pull down network which is fed back to the network. The main source of the energy dissipation is discharging route which occurs in normal MOS diodes because of the threshold voltage drop. This kind of drop has abolished in the adiabatic form of structure and this type of mechanism helps the circuit to conquer the discharging losses by making it diode free. The design of SR Flip Flop with DFAL technique is shown in the Fig. 3.2.

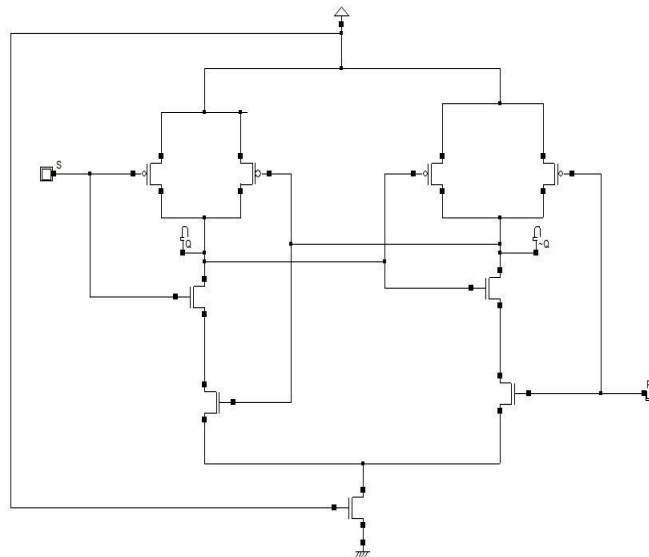


Fig. 3.2. DFAL SR Flip Flop

V. WAVEFORM

The waveform for SR Flip Flop based on ECRL and DFAL method is shown in Fig. 4.1. From both the analysis of adiabatic, we obtained that the Set and Reset condition creates the unbalance condition which can affect the one of its outputs to switch faster as expected. This unstable state can be termed as the meta-stable state of flip flop. This can be understood by the fact that when the circuit is unable to make the decision between 0 and 1 logic level within a specified period of time for the proper functioning of the circuit.

The flip flop is in set condition by applying the logic 0. As shown in the waveform when the S and R are in low that result is in high state and when the S changes its state to 1. The results changes to low, but when both the condition is activated to high then the metastable state arises and it shown by the shaded region in the diagram.

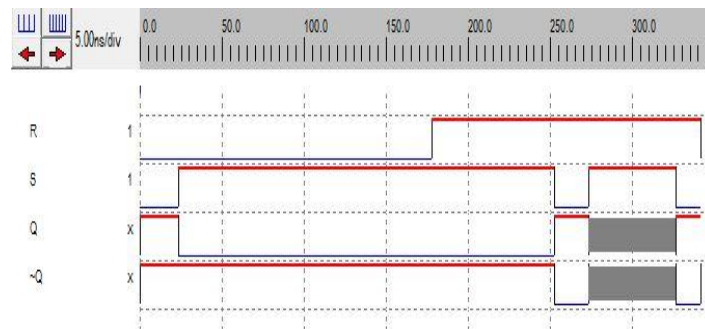


Fig. 4.1. Waveform for SR Flip Flop

VI. APPLICATION

Flip flops are the main components in the sequential circuit and edge triggered flip flop are mainly used and the most resourceful way to use in any sequential circuit. It can have a wide range of applications like:

- Data Transfer
- Data storage
- Registers
- Frequency Divider circuits
- Counters

The flip flop store one bit of the data at the time and if we want to store more than one bit, then the flip flop is connected in the form of series and parallel which is called registers. It can also use to transfer the data for this function, shift registers can be used which is able to shift or transfer the data either its right or left. But, the data can be transfer or store the data one bit at a time, when the clock signal is applied. This can use for the temporary data of storage and the further it can use for multiplication and division where bit shifting is needed.

Another major application of flip flop is counters. This is used to count the pulses or the events which can be made by the series connection of the flip flop. The flip flop is able to divide the frequency of periodic waveform and the output of the waveform is the half of the frequency of the input. These are some applications of the flip flop which can further designed by the adiabatic logic for the power saving circuits.

VII. CONCLUSION

The sequential circuit is studied successfully in this proposed paper. From the types of the sequential circuits, SR flip flop is studied which can be implemented by clocked and unclocked version of the flip flop. The basic structure of the SR flip flop is designed and truth table is verified. The SR flip flop is then designed by the adiabatic logic families by Efficient Charge Recovery logic (ECRL) and Diode Free Adiabatic Logic (DFAL).



The circuit was able to perform the Set and Reset conditions same as the conventional structure and the truth table is also verified. The waveform for the subsequent circuit was performed which can able to perform the logic level results same as the SR flip flop.

In this paper, the major aim to design a circuit for the SR Flip with the use of adiabatic technology and the energy consumed by the circuit can be reduced. The performance and evaluation techniques of the circuit are improved by these profound techniques.

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