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Performance Enhancement Of Complex Digital Circuit usingDynamic CMOS Logic

M.RoopaNandini[1], P.Mor[2] , J.M. Keller[3]

Department of Physics and Electronics, R.D.V.V., Jabalpur, Madhya Pradesh,(India)

[1]M.RoopaNandini,Research Scholar, Department of Physics and Electronics,RDVV, Jabalpur,(India)

[2]Dr P Mor Senior Scientific Officer, Department of Physics and Electronics, RDVV, Jabalpur,(India)

[3]Dr J.M. Keller professor, Department of Physics and Electronics, RDVV, Jabalpur,(India)

ABSTRACT

The performance of any logic circuit is measured in terms of area, delay and the power consumption of the circuit.The Power Delay Product is used as a unit to define the performance of the circuit. Static logic proves to be beneficial for simple and low fan in circuits on the other hand as the circuit complexity increases and the fan in is increased, static circuit power delay product increases compared to dynamic logic. The dynamic logic proves to be beneficial for high fan in and complex circuit as compared to static version. The integrated circuit designer has to make a choice for designing after considering these parameters in order to optimize the design. This paper presents a comparative study and analysis of thedynamic logicusing different technology files.

Index Terms: PDP, Dynamic Logic, Precharge,Evaluation,Power consumption, Logic synthesis

I.INTRODUCTION

The performance of any digital circuit is measured in terms of area, delay, powerconsumption or the Power Delay Product (PDP).The power in any digital circuit is mainly dependant on two things, static power dissipation and the dynamic power dissipation. The dynamic power in turn is dependent on the switching activity of the circuit. It is well known that, dynamic logic is less low-power consuming and have high speed than static logic [1]. In dynamic logic, the reduction in power is mainly due to the reduced switching activity.

II.STATIC LOGIC

Static logic circuits allow versatile implementation of logic functions based on static, or steady-state, behavior of simple CMOS structures or in other words commonly for combinational circuits[2]. A typical static logic gate generates its output levels as long as the power supply is provided. This approach, however, may require a large number of transistors to implement a function, and may have cause considerable time delay. Fig 1a shows the generalized block diagram of static logic [3].

*The author RoopaNandini is a Research Scholar,,Dr P Mor is working as a Senior Scientific Officer, Dr J.M. Keller is working as a professor, at RDVV Jabalpur.

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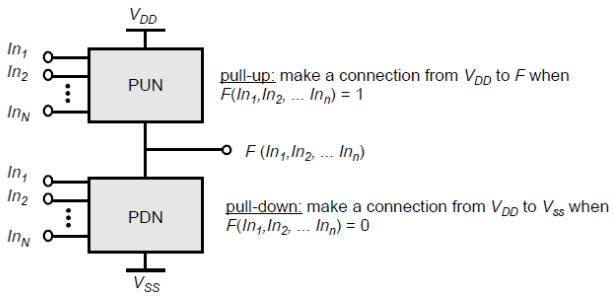
It consists of a PULL UP network formed by P transistors and a PULL DOWN network formed by N transistors. Output rises to VDD when P network is ON and drops to GND when N network is ON. The basic function of static CMOS logic is explained with example of 2- input NAND gate as shown in 1b. There is conducting path between the output node and the ground only if input voltage VA and VB are equal to logic high value. If one of theinputs are at low logic value then there is a path between voltage supply and output node is created i.e. except during switching, output connected to either VDD or GND via a low resistance path.



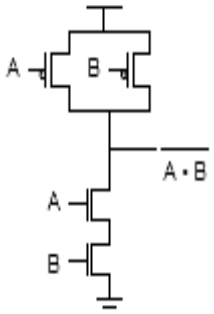


Fig 1a. Generalized Static Logic circuit.

Fig 1b. NAND logic using Static CMOS

III.DYNAMIC LOGIC

In high density, high performance digital implementations where reduction of circuit delay and silicon area is a major objective, dynamic logic circuits offer several significant advantages over static logic circuits[4-5]. Dynamic circuit uses a clocked pull up transistor rather than a pMOS that is always ON [6]. Fig.1, shows a generalized CMOS dynamic logic circuit [7]. The operation of all dynamic logic gates depends upon on temporary storage of charge in parasitic capacitance [3].This operational property necessitates periodic updating of internal node voltage levels, since stored charge in capacitor cannot retain indefinitely. Consequently, dynamic logic circuits require periodic clock signals in order to control charge refreshing. In the following, a dynamic CMOS circuit technique which allows us to significantly reduce the number of transistors used to implement any logic function is introduced. The circuit is based on first precharging the output node capacitance and subsequently, evaluating the output level according to the applied inputs.

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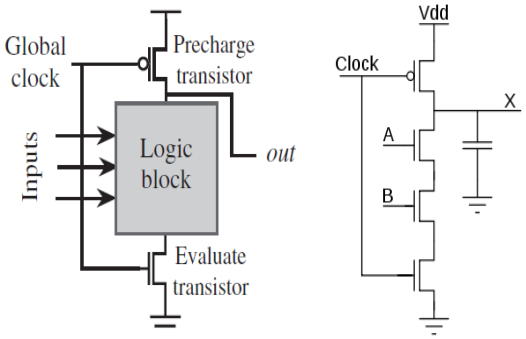
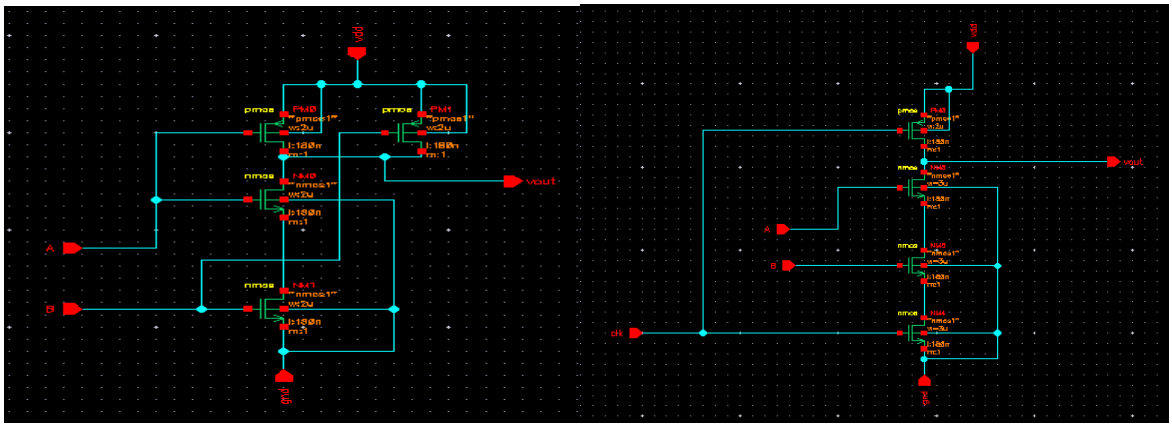


Fig 2a: Generalised Dynamic Logic circuit.**Fig 2b:** 2 input NAND(Dynamic Logic).

IV.EFFECTS OF TECHNOLOGY ON DESIGNS

It is theoretically proven that dynamic circuit provides better performance measures for high fan in and complex circuits[8]. As the technology is decreased, the size of the transistor is further reduced and the design requires less area and less silicon for implementation. In this paper many circuits starting from low fan in to high fan in and complex are designed using three different technology files using Cadence tool. The analysis and the results of the same shows that the performance of complex digital circuits are improved by using the dynamic logic. The results also show the effects of lower technology files, i.e., smaller transistor size can greatly improve the performance both for static and dynamic logic. Better results are obtained using Dynamic Logic. NAND gate with different fan in is designed forverification and also simple expressions are designed and verified. Fig 3a-3i show the circuit of the static designs used while 3j-3r show the circuit of the dynamic designs.



3 (a)-Static 2-input NAND Schematic

3 (j)- Dynamic 2-input NAND Schematic

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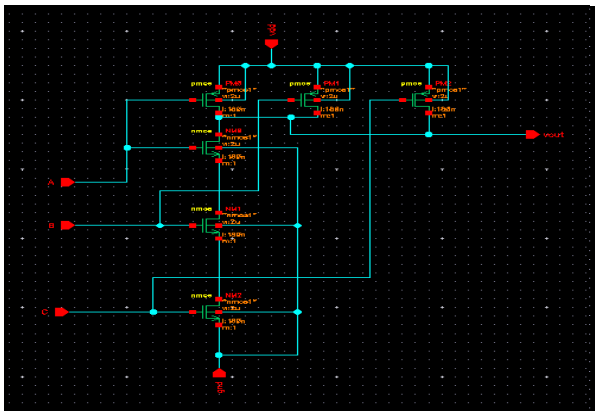
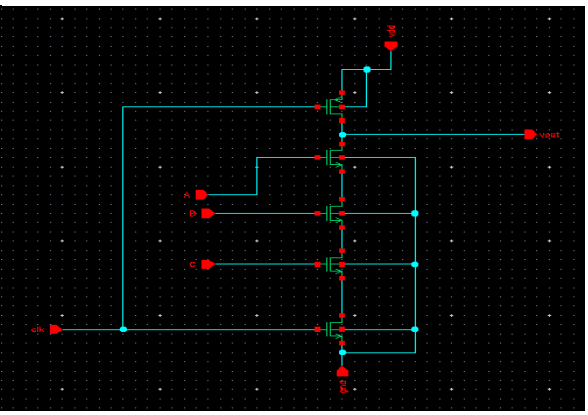
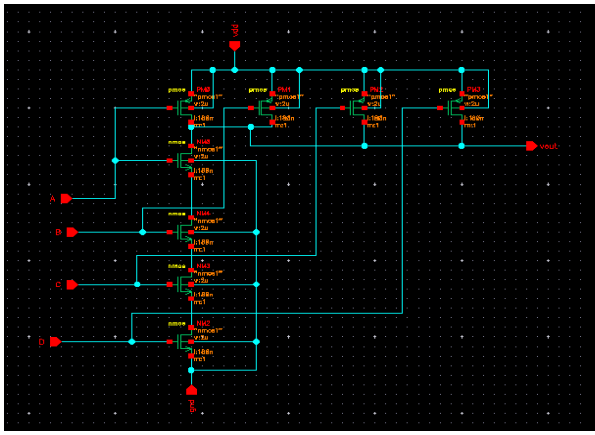


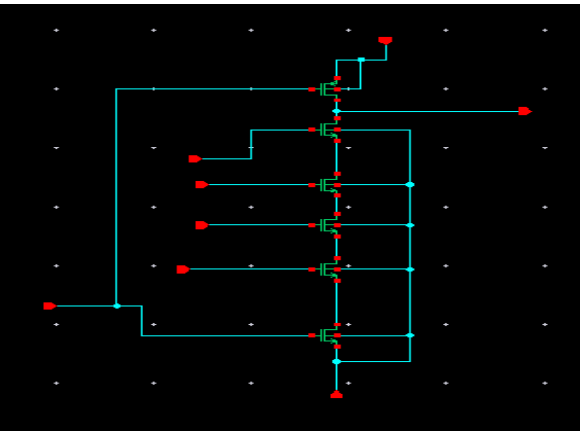
3 (b)- Static 3-input NAND Schematic



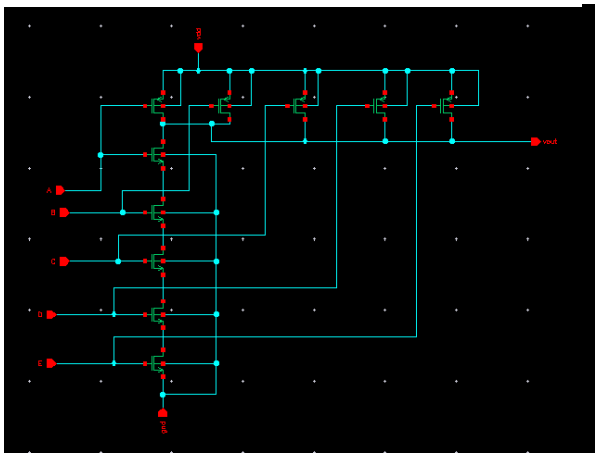
3 (k)- Dynamic 3-input NAND Schematic



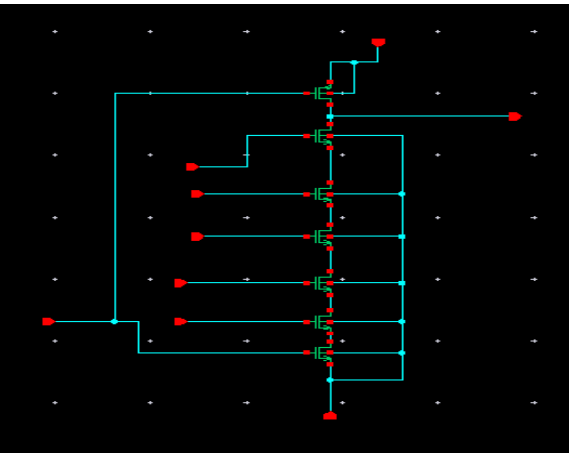
3 (c) Static 4-input NAND Schematic



3 (l)- Dynamic 4-input NAND Schematic



3 (d) Static 5-input NAND Schematic



3 (m)- Dynamic 5-input NAND Schematic

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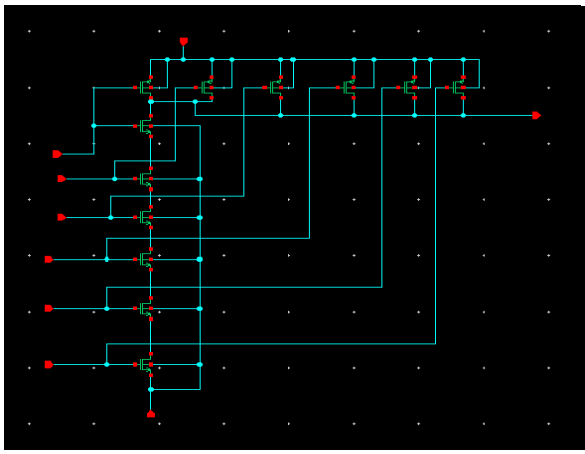
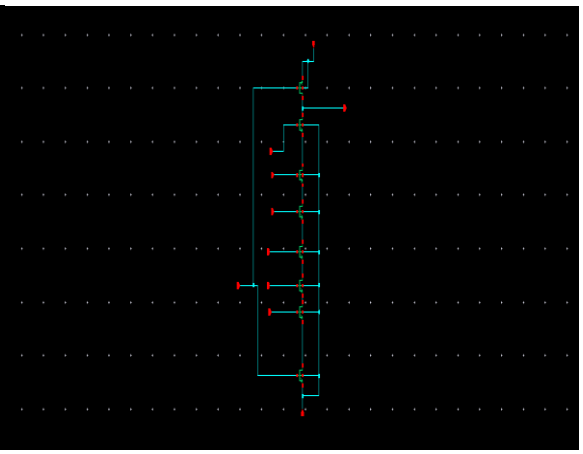
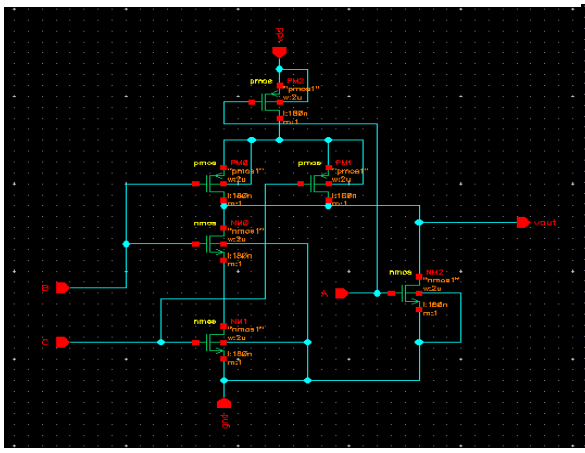


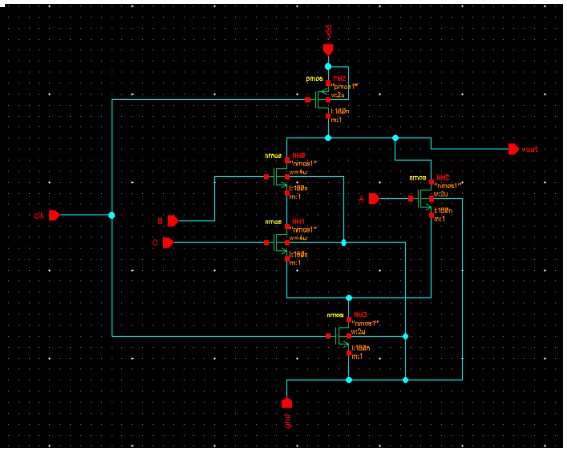
3 (e)- Static 6-input NAND Schematic



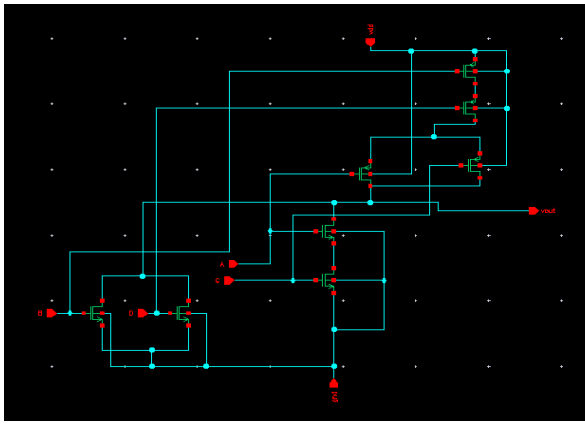
3 (n)- Dynamic 6-input NAND Schematic



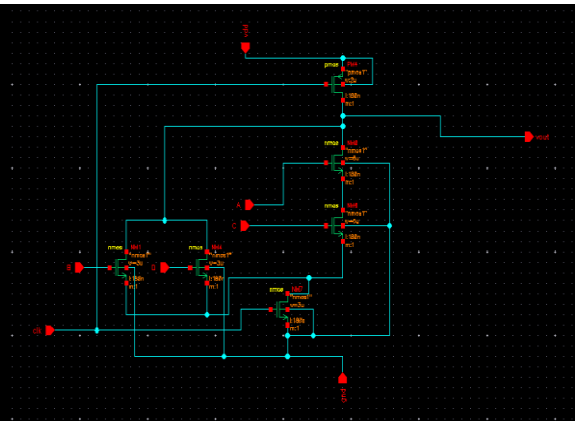
3 (f)- Static (A+BC)' Schematic



3 (o)- Dynamic (A+BC)' Schematic



3 (g)- Static (AC.(B+D))' Schematic



3 (p)- Dynamic (AC.(B+D))' Schematic

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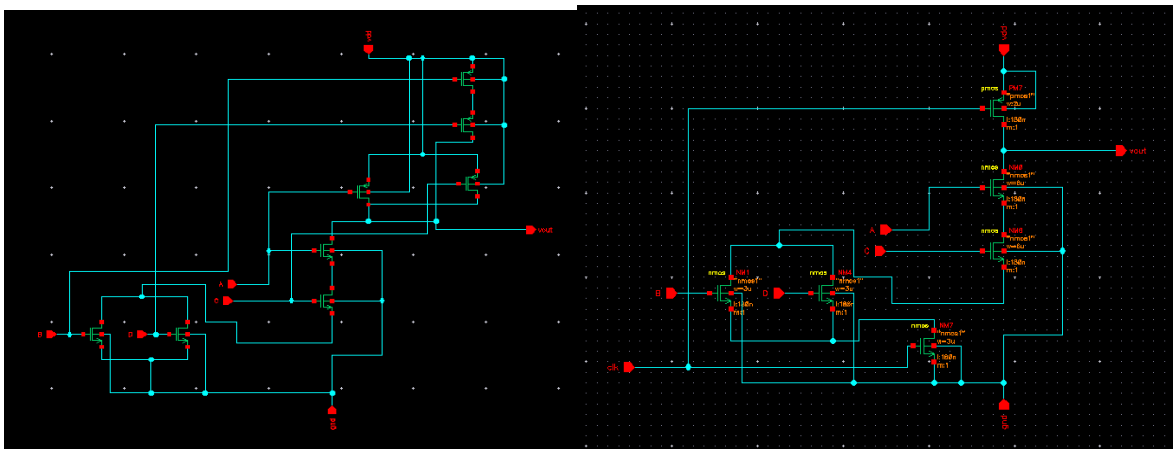
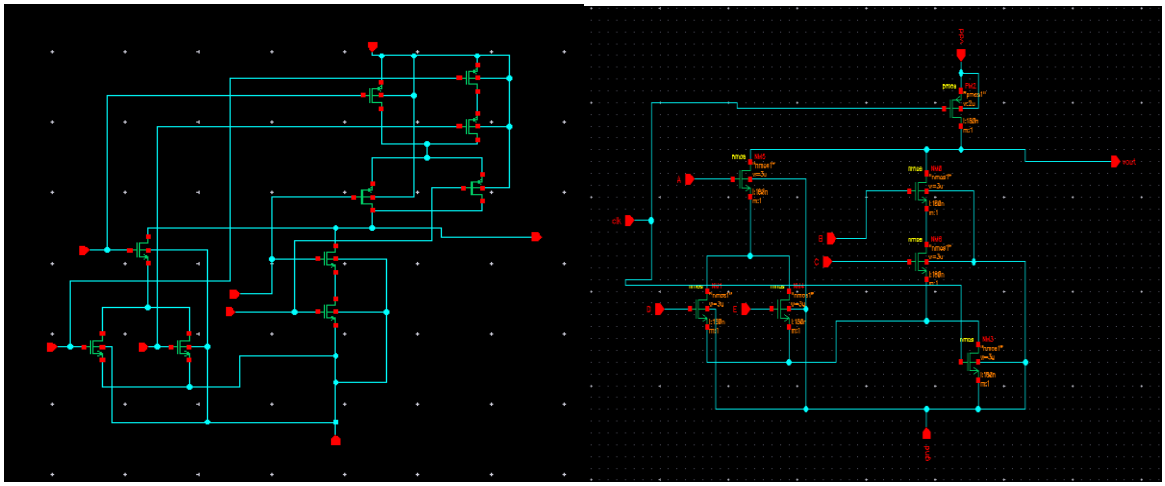


3 (h)- Static (AC+(B+D))' Schematic

3 (q)-Dynamic (AC+(B+D))' Schematic



3 (i)- Static (A.(D+E)+BC)' Schematic

3 (r)-Dynamic (A.(D+E)+BC)' Schematic

V.ANALYSIS AND RESULTS

The analysis was carried out using three technology files 180nm, 90nm and 45 nm. Fig 4a-4i show the analysis of the static designs while 4j-4r show the analysis of the dynamic designs.

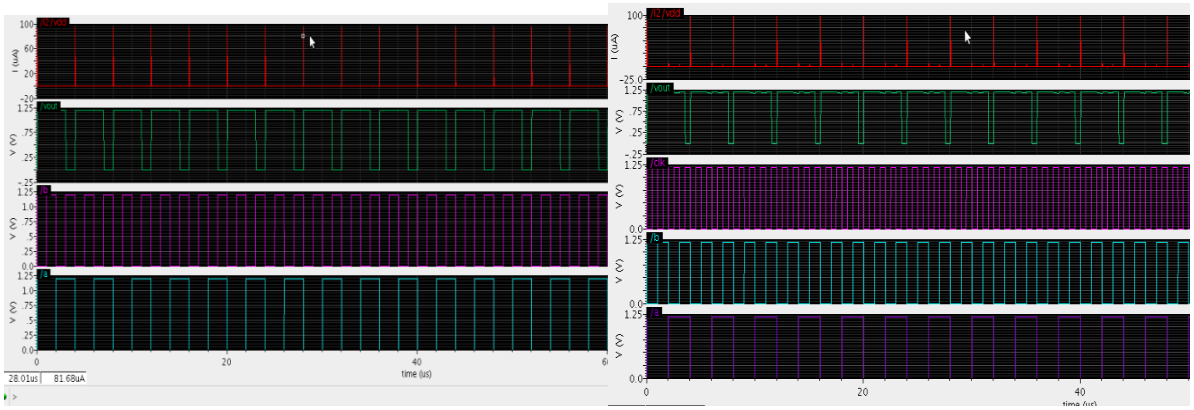


Fig 4a:Static 2 input NANDAnalysisFig 4j: Dynamic 2 input NANDAnalysis

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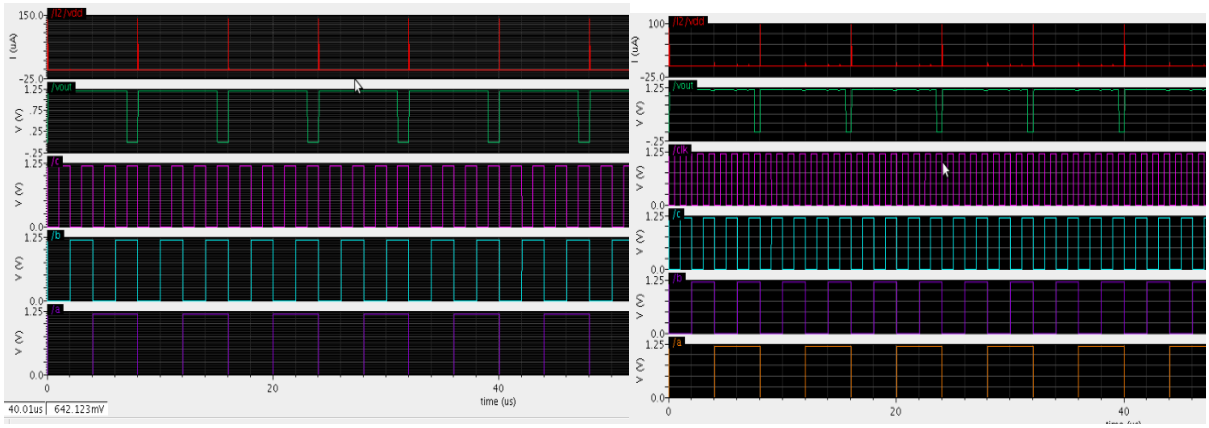

Fig 4b:Static 3 input NAND Analysis Fig 4k:Dynamic 3 input NANDAnalysis

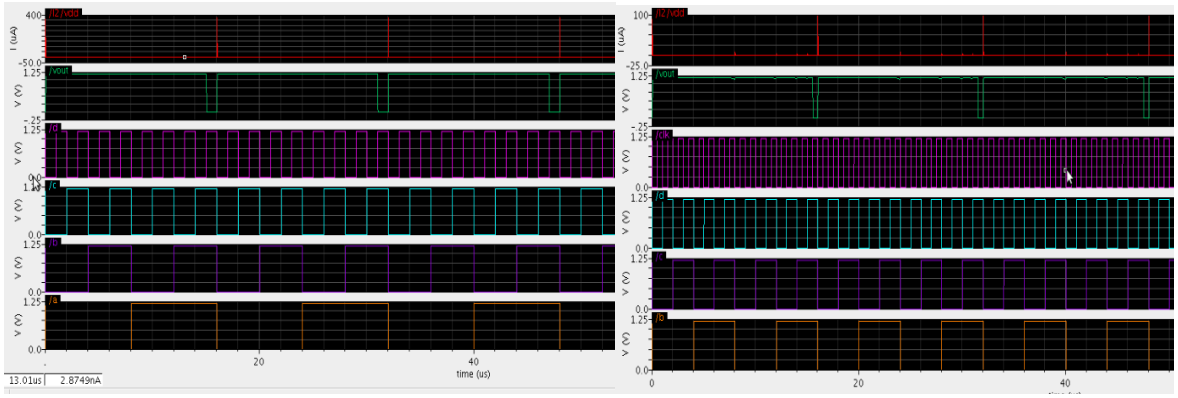

Fig 4c:Static 4 input NANDAnalysis Fig 4l: Dynamic 4 input NANDAnalysis

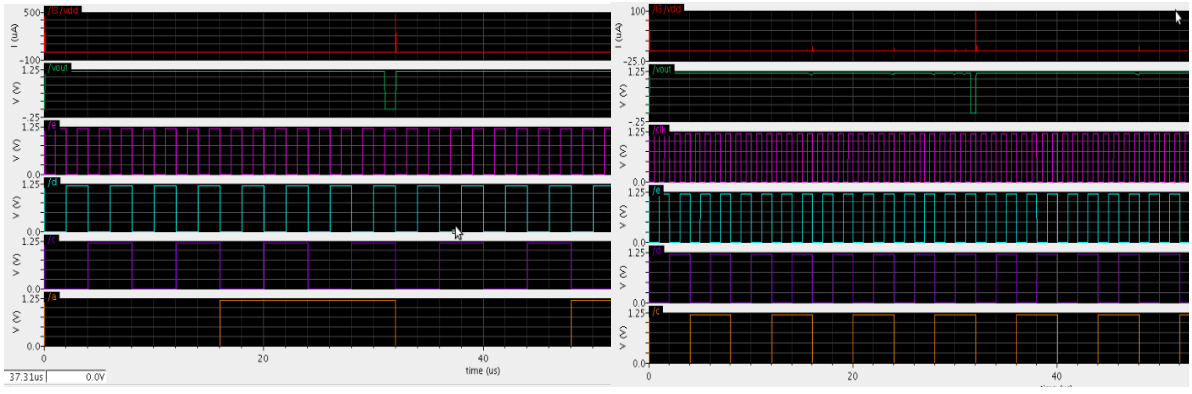

Fig 4d: Static 5 input NAND Analysis Fig 4m: Dynamic 5 input NANDAnalysis

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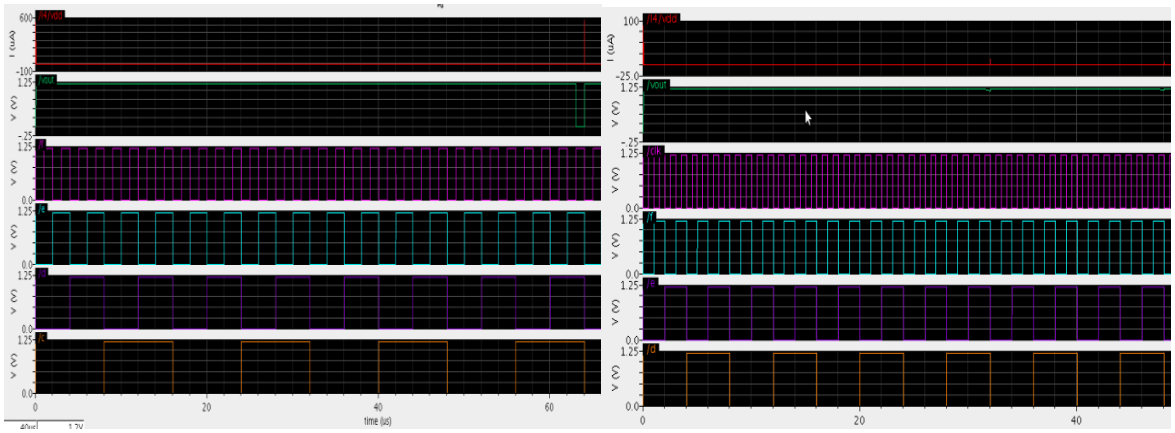

Fig 4e: Static 6 input NANDAnalysis Fig 4n: Dynamic 6 input NANDAnalysis

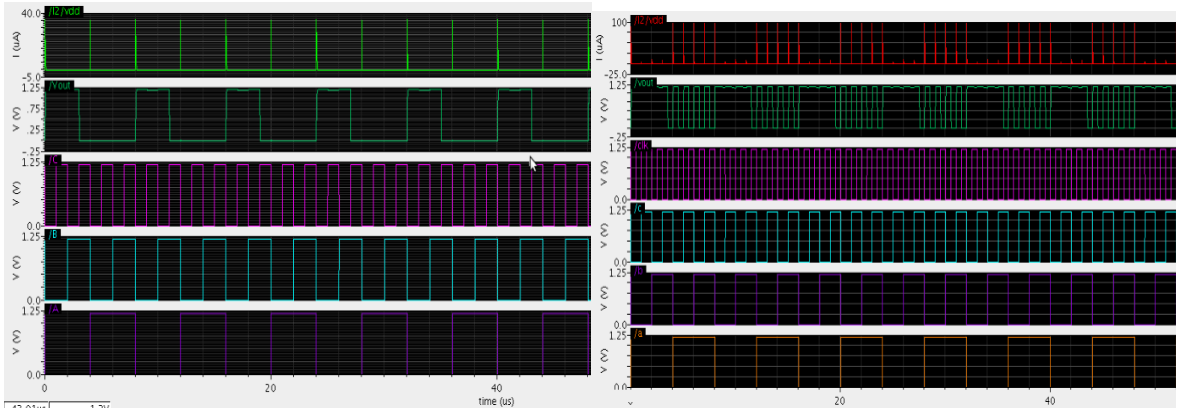

Fig 4f: Static (A+BC)'Analysis Fig 4o: Dynamic (A+BC)' Analysis

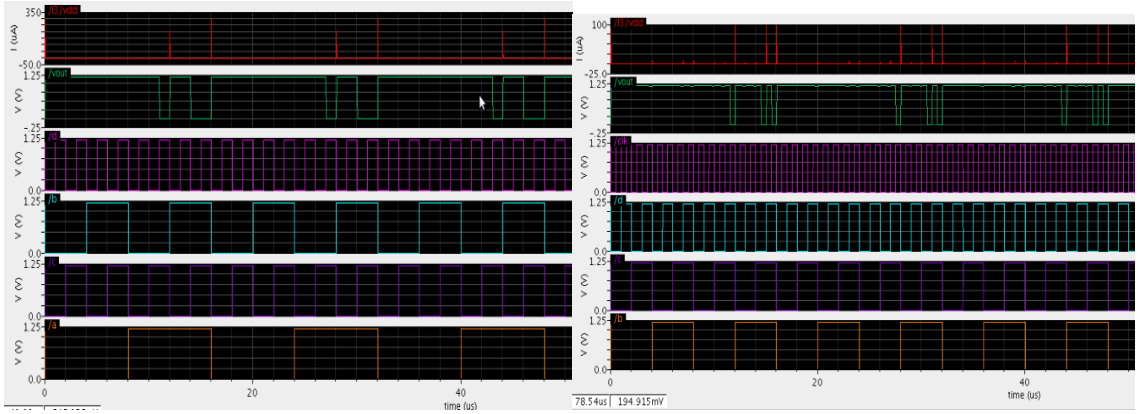

Fig 4g:Static (AC.(B+D))'Analysis Fig 4p: Dynamic (AC.(B+D))'Analysis

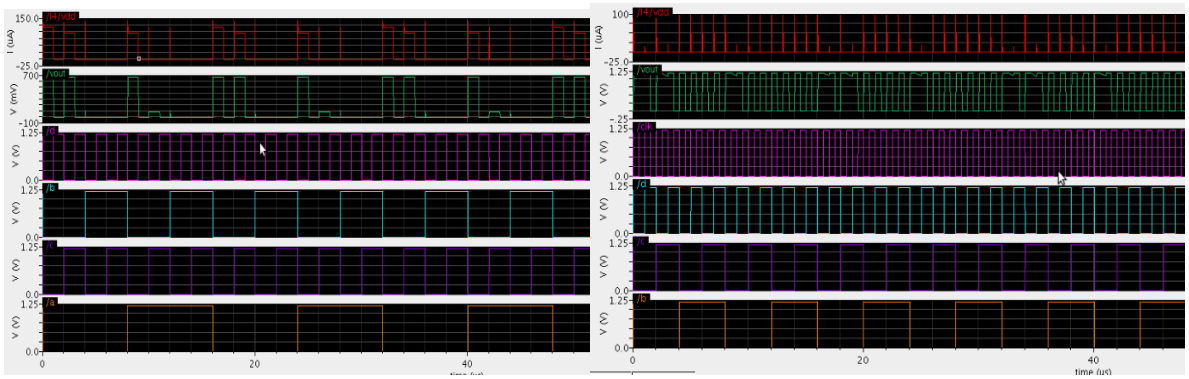

Fig 4h:Static (AC+(B+D))'Analysis Fig 4q: Dynamic (AC+(B+D))'Analysis

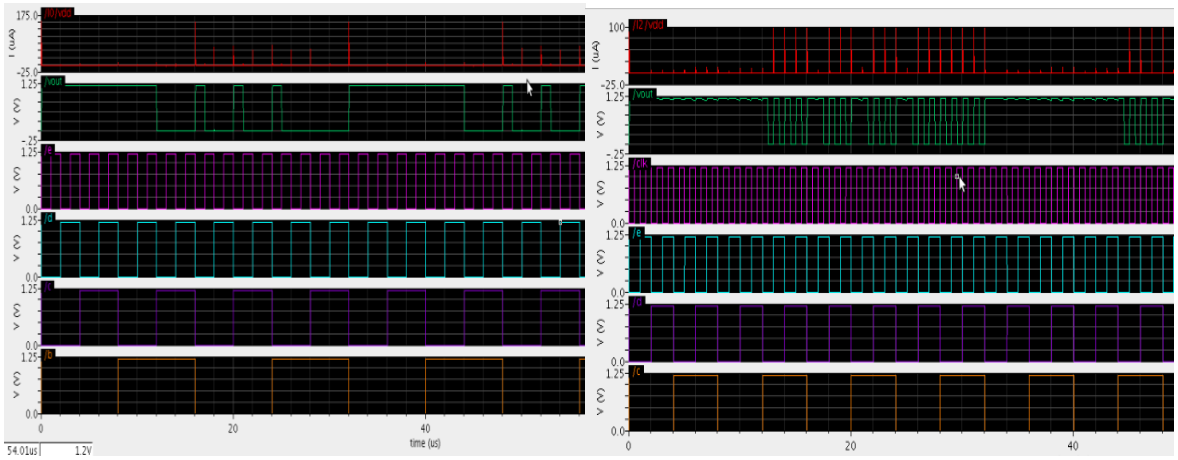

Fig 4i:Static (A.(D+E)+BC)'Analysis Fig 4r:Dynamic (A.(D+E)+BC)'Analysis

Circuit delay, power and the PDP are calculated after the simulation using the analysis waveforms for all the designs using 180, 90 and 45nm technology files. Table 4a shows the results for 180nm, Table 4b for 90nm and table 4c shows the results for 45nm.

Circuit	Area in number of transistors		Delay in secs		Power in Watts		Power Delay Product	
	Static	***Dynamic***	***Static***	***Dynamic***	***Static***	***Dynamic***	***Static***	***Dynamic***
2 i/p NAND	4	4	21.0E-6	31.5E-6	825.6E-9	829.9E-9	17.34E-12	26.14E-12
3 i/p NAND	6	5	33.0E-6	38.5E-6	418.3E-9	414.3E-9	13.7E-12	15.95E-12
4 i/p NAND	8	6	42.0E-6	43.0E-6	209.2E-9	214.2E-9	8.786E-12	9.639E-12
5 i/p NAND	10	7	45.0E-6	46.5E-6	125.4E-9	129.6E-9	5.643E-12	6.026E-12
6 i/p NAND	12	8	62.0E-6	63.0E-6	86.89E-9	87.44E-9	5.387E-12	5.509E-12
(A+BC)'	6	5	29.0E-6	16.5E-6	468.3E-9	2.08E-6	13.58E-12	34.4E-12
(AC.(B+D))'	8	6	34.5E-6	38.36E-6	426.2E-9	641E-9	14.7E-12	24.61E-12

(AC+(B+D))'	8	6	21.29E-6	8.47E-6	742.8E-9	2.736E-6	15.81E-12	23.17E-12
(A.(D+E)+BC)'	10	7	29.75E-6	23.35E-6	399.1E-9	1.606E-6	11.8E-12	37.5E-12

Table 4a : 180nm results

Circuit	Area in number of transistors		Delay in secs		Power in Watts		Power Delay Product	
	Static	***Dynamic***	***Static***	***Dynamic***	***Static***	***Dynamic***	***Static***	***Dynamic***
2 i/p NAND	4	4	21.0E-6	31.5E-6	385.6E-9	381.5E-9	8.098E-12	12.02E-12
3 i/p NAND	6	5	33.0E-6	38.5E-6	201.8E-9	196.5E-9	6.659E-12	7.565E-12
4 i/p NAND	8	6	42.0E-6	45.0E-6	1076E-9	101.8E-9	4.519E-12	4.581E-12
5 i/p NAND	10	7	45.0E-6	46.5E-6	66.33E-9	60.67E-9	2.985E-12	2.821E-12
6 i/p NAND	12	8	62.0E-6	63.0E-6	44.2E-9	40.48E-9	2.74E-12	2.55E-12
(A+BC)'	6	5	29.0E-6	16.5E-6	217.9E-9	927.4E-9	6.299E-12	15.3E-12
(AC.(B+D))'	8	6	34.5E-6	38.36E-6	210.8E-9	292.3E-9	7.24E-12	11.21E-12
(AC+(B+D))'	8	6	21.39E-6	8.47E-6	23.41E-6	1.214E-6	500.7E-12	10.28E-12
(A.(D+E)+BC)'	10	7	29.75E-6	23.35E-6	211.6E-9	720.6E-9	6.22E-12	16.83E-12

Table 4b : 90nm results

Circuit	Area in number of transistors		Delay in secs		Power in Watts		Power Delay Product	
	Static	***Dynamic***	***Static***	***Dynamic***	***Static***	***Dynamic***	***Static***	***Dynamic***
2 i/p NAND	4	4	4.019E-6	6.50E-6	252.E-9	72.958E-6	1015E-15	19.3E-12
3 i/p NAND	6	5	6.021E-6	7.023E-6	126.9E-9	127.1E-9	764E-15	0.89E-12
4 i/p NAND	8	6	7.02E-6	7.032E-9	985.9E-9	1.031E-6	16.9E-12	7.25E-12
5 i/p NAND	10	7	34.42E-9	30.22E-9	1.713E-6	1.231E-6	58.9E-15	37.1E-15
6 i/p NAND	12	8	34.42E-9	29.84E-9	2.642E-6	1.637E-6	90.9E-15	48.8E-15
(A+BC)'	6	5	6.528E-6	7.752E-6	126.4E-9	9.534E-6	825E-15	73.87E-12
(AC.(B+D))'	8	6	9.264E-6	11.27E-6	125.1E-9	175.1E-9	1158E-15	1972E-15
(AC+(B+D))'	8	6	4.819E-6	2.587E-6	201.1E-9	350.4E-9	968.6E-15	906E-15
(A.(D+E)+BC)'	10	7	7.208E-6	1.248E-6	137.9E-9	582.0E-9	993E-15	735E-15

Table 4c : 45nm results

VI.CONCLUSIONS

The analysis and results show that the performance drastically changes from one technology to another. By comparing table 4a and 4b we can conclude that there is 50% increase in the performance. Table 4c shows

further reduction in PDP for static logic and high fan in, complex dynamic circuits. Hence the tradeoff between area, delay, power and the logic have to be analyzed properly before implementing any circuit to get optimum results.

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