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Design and Implementation of Flash Analog to Digital Converter for High Speed and Low Power Applications

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ABSTRACT

The DSP (Digital Signal Processing) has many advantages over the analog processing. Therefore, with the recent advent of technology most of the signal processing tasks have been transferred from the analog to the digital domain. The ADCs (Analog to Digital Converter) provide a line between the real world analog signals and the digital processors. Therefore, ADCs become an elementary part of almost all modern electronic systems. Flash analog to digital converters also known as parallel ADC's fastest way to convert analog signal to digital signal. This paper describes the design and implementation of a Low Power flash Analog to Digital converter (ADC).

KEYWORDS:ADC, DAC, Signal Processing, Flash Memory

I.INTRODUCTION

The Flash ADC is the fastest ADC among a wide range of accessible ADC architectures. A N-Bit Flash ADC utilizes the 2N-1 comparators for information change. Applications such as wireless communications and digital audio and video have created need for cost-effective data converters that will achieve higher speed and resolution. The needs required by digital signal processors continually challenge analog designers to improve and develop new ADC and DAC architectures. There are many different types of architectures, each with unique characteristics and different limitations. Flash analog-to-digital converters are the fastest way to convert an analog signal to a digital signal due to their parallel operation. Flash ADCs are suitable for applications requiring very large bandwidths, like receivers and high density disk drivers, but they consume more power than other ADC architectures and are generally limited to 8-bit resolution. This paper presents the systematic design of a 4-bit 2GHz flash ADC implemented in 70-nm CMOS technology. This work includes the design of a high speed flash ADC, introduction of a clocked comparator.

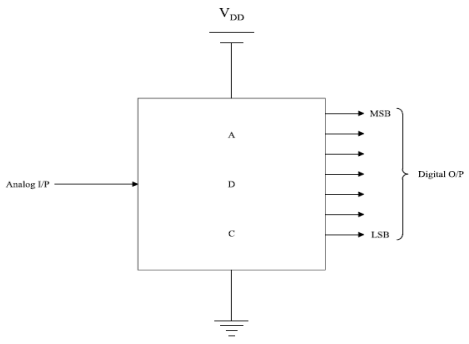

Figure 1. Block diagram of analog to digital converter

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II.FLASH ADC

Figure 2 shows the general block diagram of ADC [1] Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. A typical flash ADC block diagram. For an "N" bit converter, the circuit employs 2N-1 comparators. A resistive divider with 2N resistors ladder provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a "1" when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is "0".

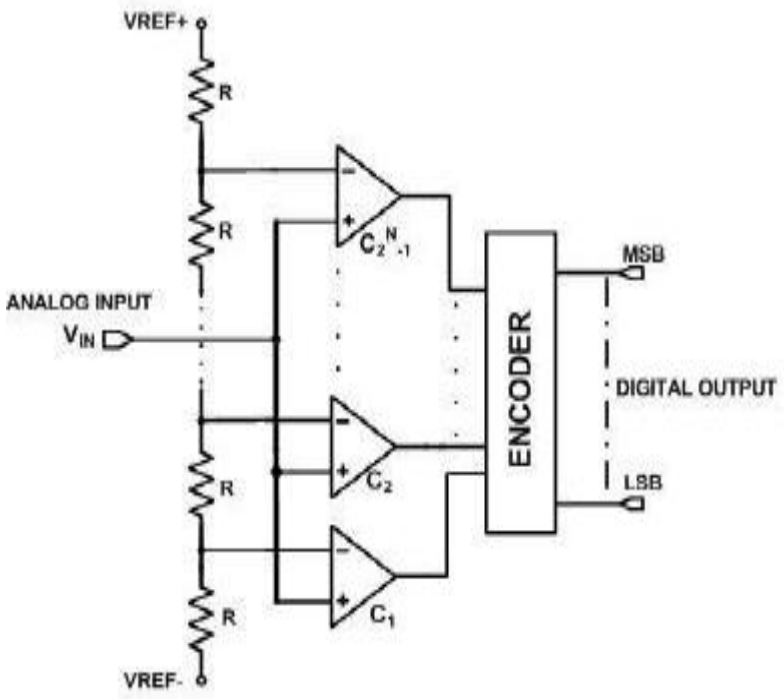

Figure. 2. Flash ADC architecture

As shown in figure 2, the flash ADC is composed of three major components: resistors ladder, comparators and encoder. "The comparators are typically a cascade of wideband and low gain stages. They are low gain because at high frequencies it's difficult to obtain both wide bandwidth and high gain. They are designed for low voltage offset, such that the input offset of each comparator is smaller than a LSB of the ADC. Otherwise, the comparator's offset could falsely trip the comparator, resulting in a digital output code not representative of a thermo meter code."

A D-latch at each comparator is used to stores the Output result. So that the end state is forced to either a "1" or a " 0"'. The analog input voltage is concurrently compared to the reference voltage levels generated from resistors ladder and the speed of A/D conversion is therefore maximized. The outputs of comparators form a thermometer code (TC) which is a combination of a series of zeros and a series of ones, e.g., 0000…0101…1111. Because binary code is usually needed for digital signal processing, a thermometer code is then transformed to a binary code through a (2n-1)-to-n TC-to-BC encoder, where n is the resolution (bits) of

ADCs. The cost of such a traditional encoder increases exponentially with the resolution. Optimizations on area cost, circuit latencies power consumptions are greatly expected. In this paper we have low used power Comparator in the design throughout.

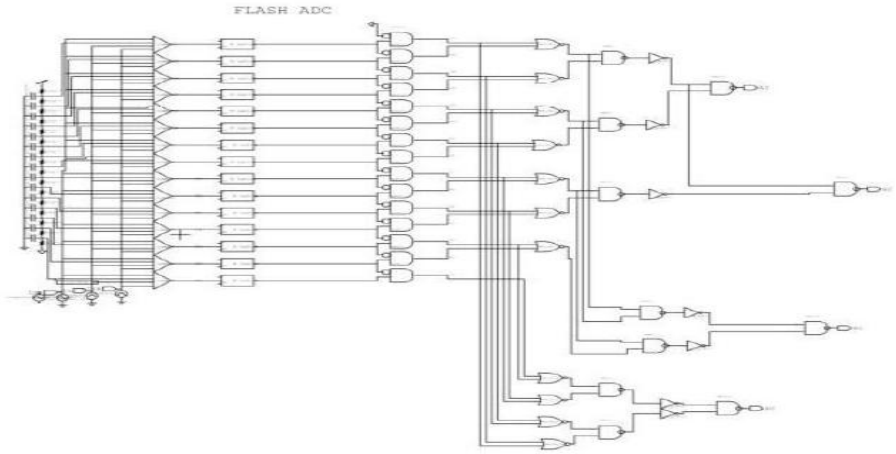

Fig 3. 4-Bit Flash ADC architecture

III. PROPOSED ARCHITECTURE

Flash ADCs utilize massive parallelism in its architectures and hence the name parallel ADC. The results of the conversion are available at the end of one clock cycle. Due to the parallel structural design it is the fastest ADC among all the other types and is appropriate for large bandwidth applications such as radar processing data acquisition, high density disk drives, satellite communication, data communications and real time oscilloscopes.

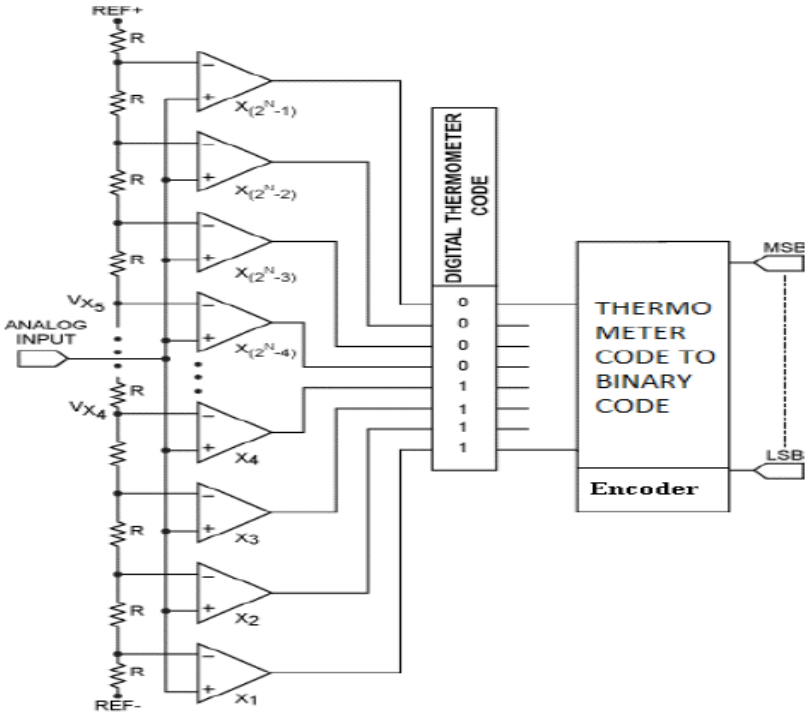

Figure 4. Generic block diagram of flash ADC

It is also highly used in other types of ADCs such as pipeline ADCs and multi bit sigma delta ADCs. Flash ADC is limited to a resolution of six to eight bits because the numbers of comparators utilized in these ADCs are doubled if the resolution is enhanced by one bit. Due to this, it consumes a lot of power and becomes costly, as the resolution increases [3]. The speed and power of an encoder play an important role in the design of flash ADC. The proposed encoder utilizes the properties of logic style implementation and wallace tree implementation. In order to reduce the power dissipation, the logic implementation is done with the use of dynamic logic [4].

Fig. 4 shows the generic flash ADC block diagram. From the figure, it is clear that 2N -1 comparators are needed for N bit flash ADC. Each comparator is connected with one input to an analog input and another to a reference voltage. The reference voltage for the comparator is generated with the help of a resistor ladder. The resistor ladder consists of 2N resistors. The reference voltages are uniformly spaced by least significant voltage between the smallest reference voltage and the largest reference voltage. When the input voltage is less than the reference voltage of comparator it produces logic low otherwise, the comparator output is logic high. The outputs of the comparators are coming in a specific fashion which is known as thermometer code. It‟ s named because it is like a mercury thermometer, where the mercury column always rises to the suitable temperature and no mercury is available beyond that temperature. This thermometer code is further translated into a binary data with the assist of a thermometer to binary code converter. Flash ADC requires a huge number of comparators when the resolution increases. For example, a 6-bit flash ADC requires 63 comparators, but 1023 comparators are required for a 10-bit flash ADC. This exponential increase of comparators needs a large die size which leads to huge amount of power consumption.

IV. DESIGN OF PROPOSED SYSTEM

A. Design of Single-Ended Comparator:

In the traditional flash ADC, comparators need lots of transistor number and power consumption. We design a single-ended comparator to improve the traditional flash ADC. The single-ended comparator consists of a CMOS inverter as shown in Fig. 5. The threshold voltage (*Vth*) of NMOS can be expressed as

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right)$$

Vth0 is threshold voltage when source and bulk is connected together, γ is body effect parameter and Φf is semiconductor parameter. VSB is set to 0 to avoid the body effect. The MOS operating mechanism is depended on the relationship of VGS and Vth. By assigning different resistors between the sources of two NMOS transistors, we can change the source voltages of the NMOS transistors. If VGS＜Vth, NMOS is at the “cut-off” region, and the comparator will output a negative logic “0”. If

VGS＞Vth, NMOS is at the “saturation” region, and the comparator will output a negative logic “1”.

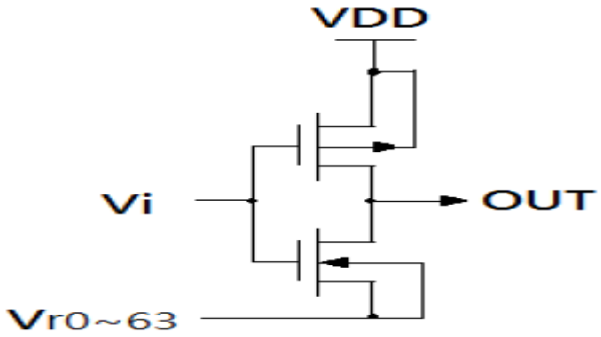

Fig 5. The presented single-ended comparator

B. Design of Encoder

Error handling capability and power dissipation are two vital parameters in the design of thermometer to binary code conversion. Offset voltage in the comparator creates bubble error in the thermometer code. There are mainly two methods to minimize the effect of bubble errors. The first method is to convert the thermometer code to gray code (intermediate step) and then convert to binary code [7]. But the accuracy of the gray code decreases steadily as more number of bubble errors is present in the thermometer code. The second method is the use of wallace tree encoder for the implementation. This technique offers a high robustness to bubble error and stuck at fault error because of its inherent global bubble error correction/suppression capability [6]. The disadvantage of this method is the large delay of the encoder. With the purpose of maintaining medium speed and low power dissipation with small amount of bubble error, the first stage of encoder is designed using dynamic logic [3] and the last stage is designed by wallace tree encoder style. In the first stage, conversion of thermometer code into two different four bit binary codes is done. With the help of four full adders and two different four bit binary codes, the final binary code is designed. The design equations are shown below.

$$b_3 = T_8$$

$$b_2 = T_4 \bullet \overline{T_8} + T_{12}$$

$$b_1 = T_2 \bullet \overline{T_4} + T_6 \bullet \overline{T_8} + T_{10} \bullet \overline{T_{12}} + T_{14}$$

$$b_0 = T_1 \bullet \overline{T_2} + T_3 \bullet \overline{T_4} + T_5 \bullet \overline{T_6} + T_7 \bullet \overline{T_8} + T_9 \bullet \overline{T_{10}} + T_{11} \bullet \overline{T_{12}} + T_{13} \bullet \overline{T_{14}} + T_{15}$$

$$a_3 = T_{24}$$

$$a_2 = T_{20} \bullet \overline{T_{24}} + T_{28}$$

$$a_1 = T_{16} \bullet \overline{T_{20}} + T_{22} \bullet \overline{T_{24}} + T_{26} \bullet \overline{T_{28}} + T_{30}$$

$$a_0 = T_{17} \bullet \overline{T_{18}} + T_{19} \bullet \overline{T_{20}} + T_{21} \bullet \overline{T_{22}} + T_{23} \bullet \overline{T_{24}} + T_{25} \bullet \overline{T_{26}} + T_{27} \bullet \overline{T_{28}} + T_{29} \bullet \overline{T_{30}} + T_{31}$$

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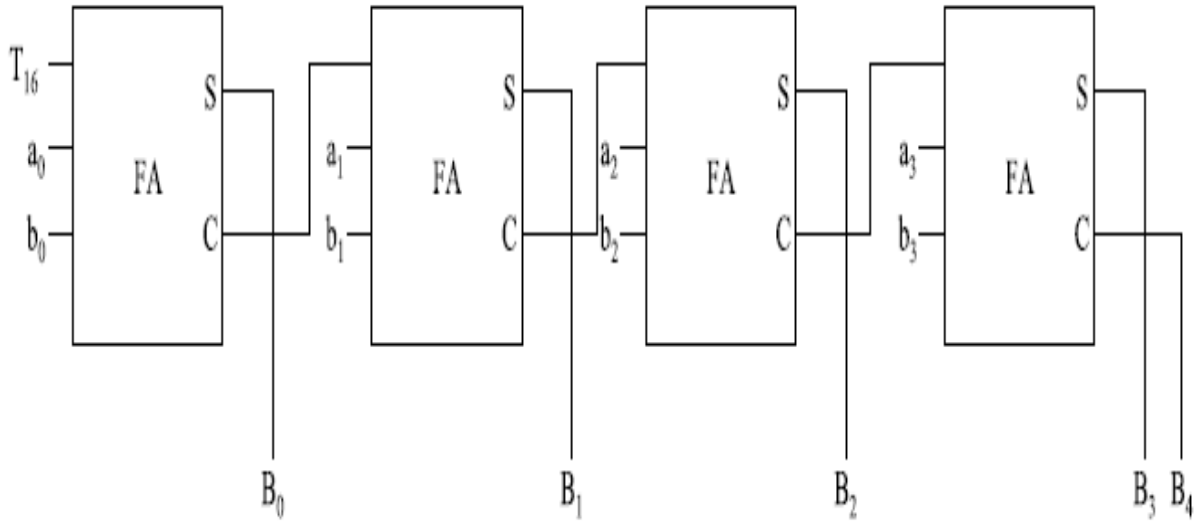

Fig 6. Final Stage Implementation using Full Adders

B4	B3	B2	B1	B0	Thermometer Code
0	0	0	0	0	00000000000000000000000000000000
0	0	0	0	1	00000000000000000000000000000001
0	0	0	1	0	00000000000000000000000000000011
0	0	0	1	1	00000000000000000000000000000111
0	0	1	0	0	00000000000000000000000000001111
0	0	1	0	1	00000000000000000000000000011111
0	0	1	1	0	00000000000000000000000000111111
0	0	1	1	1	00000000000000000000000001111111
0	1	0	0	0	00000000000000000000000011111111
0	1	0	0	1	00000000000000000000000111111111
0	1	0	1	0	00000000000000000000001111111111
0	1	0	1	1	00000000000000000000011111111111
0	1	1	0	0	00000000000000000000111111111111
0	1	1	0	1	00000000000000000001111111111111
0	1	1	1	0	00000000000000000011111111111111
0	1	1	1	1	00000000000000000111111111111111
1	0	0	0	0	00000000000000001111111111111111
1	0	0	0	1	00000000000000011111111111111111
1	0	0	1	0	00000000000000111111111111111111
1	0	0	1	1	00000000000001111111111111111111
1	0	1	0	0	00000000000011111111111111111111
1	0	1	0	1	00000000000111111111111111111111
1	0	1	1	0	00000000001111111111111111111111

1	0	1	1	1	00000000111111111111111111111111
1	1	0	0	0	00000001111111111111111111111111
1	1	0	0	1	00000011111111111111111111111111
1	1	0	1	0	00000111111111111111111111111111
1	1	0	1	1	00001111111111111111111111111111
1	1	1	0	0	00011111111111111111111111111111
1	1	1	0	1	00111111111111111111111111111111
1	1	1	1	0	01111111111111111111111111111111
1	1	1	1	1	11111111111111111111111111111111

Table 1. Five bit binary Encoder truth table

V.SIMULATION RESULTS

To analyze the behaviour of flash ADC, first discuss the results of basic design of comparator. Comparator operates at 2.5V power supply in 180nm CMOS technology. Here results are computed between characteristics such as gain, phase margin of op-amp which is used as comparator and 16bit DAC, sample and hold circuit and flash logic. The comparator is designed in 180nm technology and obtained a gain of 53.6db with a phase margin of 179 degrees in ac analysis with a start frequency from 100Hz and stop frequency of 1000 MHz where the operating point is 1.49V resulted from dc analysis.

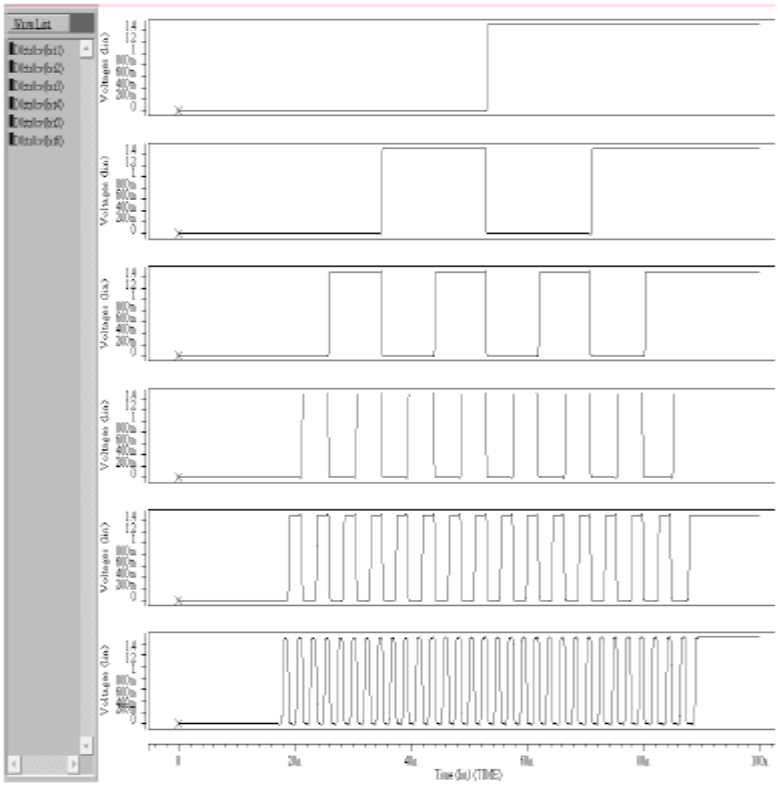

Fig 6. ADC Binary Output

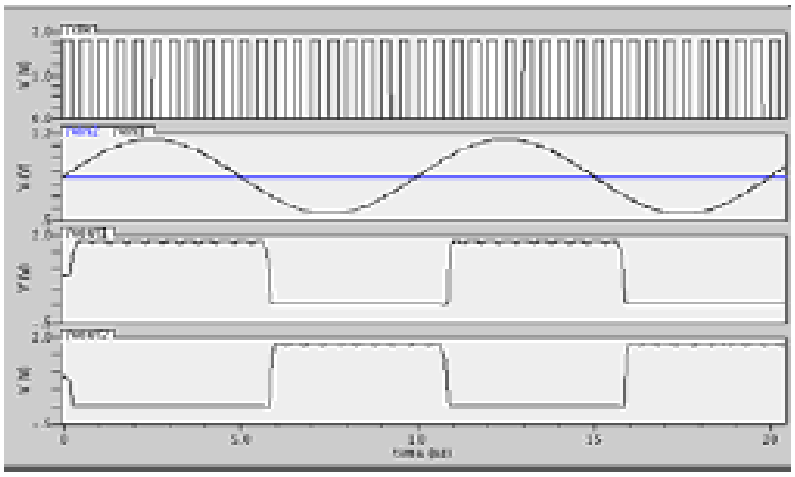

Fig 7. Logic Simulation of Comparator

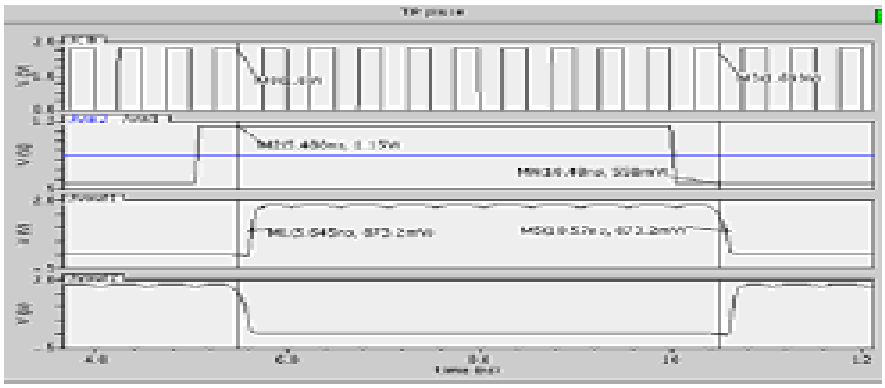

Fig 8. Transmission delay of comparator

VI.CONCLUSION

With the advancement of technology, digital signal processing has progressed significantly in recent years. However, the development of technology has not provided same level of benefit for the analog integrated circuit design. In order to extract the advantages of digital signal processing, there is a trend of shifting signal processing from analog to more capable digital domain and interacting with the analog signals only in the input as well as output stages. For a system to work efficiently, all blocks of that system should be fast. It can be seen that the analog interfaces are main bottleneck in the whole system in terms of speed and power. This fact has led researchers to develop and implement high speed analog-to- digital converters (ADCs) with low power consumption.

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