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A Novel approach for design of Real Time Traffic Control System using Verilog HDL

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ABSTRACT

In this project we projected a design of traffic light control system (TLC) to manage the road traffic and clear the way for the ambulance. The steps that are followed in this project are proposing the idea, writing code, simulate, synthesis and finally the system has been successfully verified. The controller is designed by using Verilog Hardware Descriptive Language, Simulated using XILINX ISE tool and synthesized on Spartan 3 FPGA family .

Keywords: FSM, Simulation, Traffic Light Control System (TLC), Verilog, Xilinx ISE Simulator, FPGA, Spartan 3.

I. INTRODUCTION

Traffic lights are the signaling devices used to manage traffic on multi-way road. These are positioned to control the competing flow of the traffic at the road intersections to avoid collisions. By displaying lights (red, yellow and green), they alternate the way of multi -road users. The implementation of traffic Light Controller can be through a Microcontroller, Field Programmable Gate Array or Application Specific Integrated Circuit. FPGA implementation is advantageous over ASIC and microcontroller; number of IO ports and performance compared to microcontroller and implementation with FPGA is less expensive compared to ASIC design. Now a days Traffic jamming is a serious predicament in many of the cities and towns throughout the globe. To travel within the cities to the place of work or restoration has become an issue to the commutates all along. Because of this public lose time, money and mostly energy resources will be drained due to frequent use of automobiles. In the past many ideas have come up to reduce the complexity of the traffic congestion. Generally the time allotment is unchanging for east and west side, in the same way for north and south side in a traffic light controller near cross roads. To crack these traffic related issues we are emerging a system which reduces the traffic jam The traffic light arrangement works on the particular switching of Red, Green and Yellow light in a sequence and whenever an ambulance is in the traffic it is detected using a sensor and the light automatically switches to green and all other roads are blocked.

II. PROPOSED METHODOLOGY

In this paper we are going to design a time based traffic light control system for a junction of having four ways. We are internally designing a decrement counter which is used to display the signal time in a decrement order and also to change the signal from on path to another sequentially. In the conventional traffic light controller we were not able to change the signals during emergencies like when an ambulance enters in any path and also we there was not able to change the signal time during peak and non-peak hours. So we are overcoming these problems in this paper. In addition to the time based traffic controlling, we are placing siren sensors in all four paths. When an ambulance enters in a particular path, the siren sensor senses the arrival of the ambulance in that path. The present signals and the present time will be paused; traffic signal for that particular path will be made green so that the ambulance passes smoothly. As soon as the ambulance leaves, the previous signals and also the time will be resumed. In this paper we have an input signal called peak. During non-peak hours this signal will be low and the signal time will be for sixty seconds. In peak hours there will be more vehicles. So the signal time should also be increased. During peak hours the peak signal will be made high. When the peak signal made high, the signal will stay for one hundred and twenty seconds for the smooth movement of the vehicles.

At first the North traffic will be allowed to move and then traffic in the East, South and West direction will be allowed to move in sequence. The advantage of writing Traffic Light Controller program is that in a program, modifications as per requirements can be done easily i.e., suppose the traffic on main road should be allowed for more time and for side roads the traffic should be allowed for less time; then the clock is divided in such a way that for main road the clock period will be more and for side roads the clock period will be less, this is because the main road traffic is heavy when compared to the side road traffic [5]. In general TLC System will be having three lights (red, green and yellow) in each direction where red light stands for traffic to be stopped, green light stands for traffic to be allowed and yellow light stands for traffic is going to be stopped in few seconds. But in this paper, yellowlight is split into two phases and are included in the signaling lights along with red and green lights in order to indicate that in the first phase of yellow light, pedestrian wille OFF and in the second phase, pedestrian will be ON. Traffic congestion has been causing many critical problems and challenges in most cities of modern countries. To a commuter or traveler, congestion means lost time, missed opportunities, and frustration. To an employer, congestion means lost worker productivity; trade opportunities, delivery delays, and increased costs. To solve congestion problems is feasible not only by physically constructing new facilities and policies but also by building information technology transportation management systems.

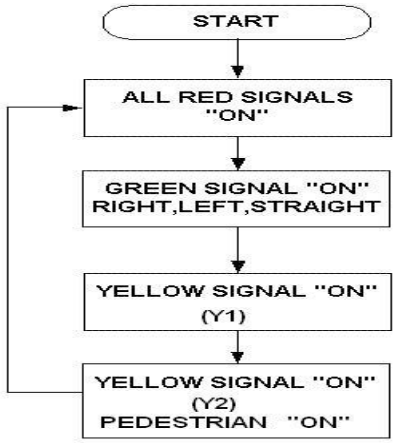

Fig. 1 TLC Flow Chart

The sequential order of the flow chart helps the programmer in the design regarding the flow of the program. North/ south-bound traffic will start with a green signal light while all the other lanes being red, the traffic will be stopped. After a predetermined time, the north/south traffic light turns yellow and then to red, allowing the east/west signal light to be green and the same sequence as the north/south-bound traffic is followed. The system will continue to be in this loop until an indication of a vehicle in a left turn lane occurs. When the signal light turns yellow, the controller scans the inputs. If high, then the program will jump to a subroutine which has a different light sequence. This sequence controls the main lights along with the left turn lights. After completion of the subroutine sequence, the program returns to the main loop. The flow chart can be applied to any number of road structures. In this paper, a four road structure is considered in which the four directions labeled with four labels namely North, South, East and West. Each traffic lane has set of three traffic light signals, “Red, Yellow, and Green”, which operates similar to general signaling lights i.e., it changes from red to green and then to yellow and after that back to red signal.

III. STRUCTURE OF ROAD

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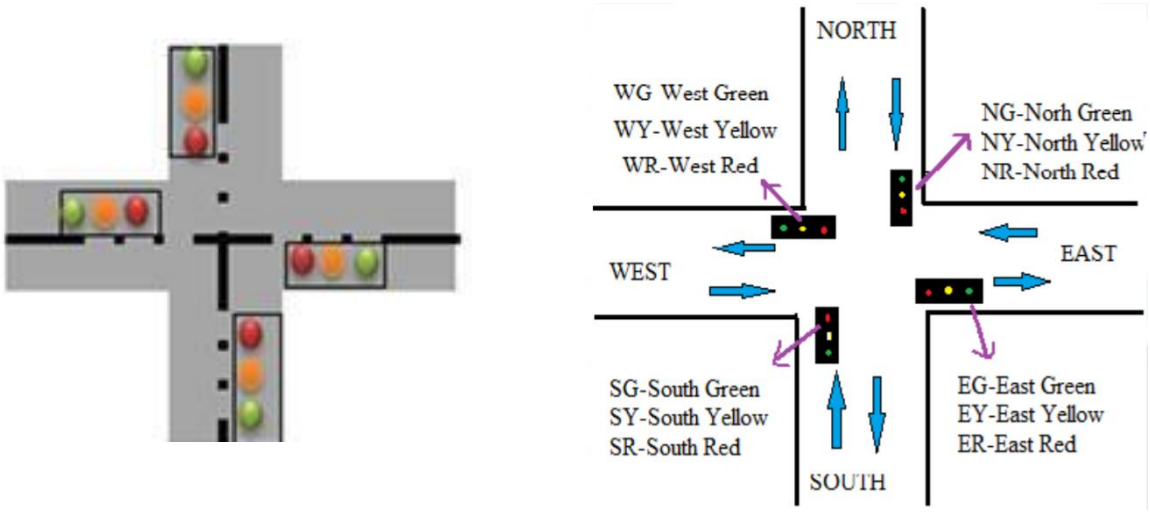

Fig. 2 A Single junction of Four Roads

In the conventional traffic light system there are four LEDs used on each sides in order to reduce the power consumption we use sensors. The sequence of traffic is as shown in Figure 2 fist North rode allow to move the traffic after that East rode allow traffic to reach their place . After east South rode allow moving the traffic on rode and then West rode allow to move the vehicles. The advantage of this particular Traffic Light Controller program is that modification can be done easily as per the requirements. Every lane has their own separate traffic light system which is having regular as usual red, yellow and green lights. the north side lane has north green ,north red, and north yellow light which is presented by NG,NR,NY respectively. Similarly east side also having EG, ER, EY respectively. And the lights of south side are presented by SG, SR, SY. Similarly the west side lights also presented as WG, WR, WY. The system will continue to be in this loop until an indication of a vehicle in a left turn lane occurs. When the signal light turns yellow, the controller scans the inputs. If high, then the program will jump to a subroutine which has a different light sequence. This sequence controls the main lights along with the left turn lights. After completion of the subroutine sequence, the program returns to the main loop. The flow chart can be applied to any number of road structures. In this paper, a four road structure is considered in which the four directions labeled with four labels namely North, South, East and West. Each traffic lane has set of three traffic light signals, “Red, Yellow, and Green”, which operates similar to genera signaling lights i.e., it changes from red to green and then to yellow and after that back to red signal .

Traffic Light Controller can be designed by starting with certain assumptions. Initially Red signal is ON in North, East, West and South direction. The TLC program will allow to do modification as per requirements i.e. the clock is divided in such a way that the clock period can be increased or decreased as per the load of traffic on the road. The road with heavy traffic will be allowed a more clock period than a road with a low traffic[8]. The conventional TLC System will be using three LED‟ s (red,green,yellow) in each direction where Red LED stands for traffic to be stopped, Green LED stands for traffic to be allowed and Yellow LED stands for traffic is

going to stopped in few seconds. But this paper contain a motor which will rotate after the yellow signaling. North bound traffic will start with a green signal light while all others being red ,the traffic will be stopped. After a predetermined time, the north light will become yellow and then motor rotates it will turns red, allowing the east to be green and same sequence as north bound traffic is followed. The system will continue in this loop.

IV STATE MACHINE, STATE TABLE AND HARDWARE DESCRIPTION:

The TLC state diagram shown in Fig. 3 illustrates that whenever cnt=00 and dir=00,then green light in north direction will be ON for few seconds and red signal light in all other directions namely west, south and east will be ON. When cnt=01 and dir=00 then yellow light (y1) will be ON for few seconds and when cnt=01 yellow light (y2) and pedestrian north will be ON and then dir is incremented by one and cnt is assigned to zero. So when cnt=00 and dir=01, the green light in east direction will be ON for few seconds and all red lights in other directions be ON.

A finite state machine (FSM) is a mathematical model of computation used to design the sequential logic circuits. The machine is in only one state at a time, the state it is in at any given time is called the current state. It can change from onestate to another when initiated by a triggering event or condition, this is called transition.The output is produced by the system in order to the response of the input signal frominput handling module [9-10].

In this design, PTLC uses a standard two process finite state machine where one process is used to change states of every clock cycle while the other process is used to combinatorial calculate what the next state should be based on the current inputs and the current state.

South	West
GS= green south RS= right south Y1S=yellow light1south Y2S= yellow light 2 south PDS=pedestrain south	GW = green west RW = right west Y1W = yellow light 2 west Y2W = yellow light 2 west PDW = pedestrain west
North	**East**
GN = green north RN = red north Y1N = yelow light 1 east Y2N = yellow light 2 north PDN = pedestrain north	GE = green east RE = red east Y1E = yellow light 2 east Y2E = yellow light 2 east PDE = pedestrain east

Table I. Terms used in State Diagram

cnt=01 yellow light (y2) and pedestrian east will be ON and then dir is incremented by one and cnt is assigned to zero. So whenever cnt=00 and dir=10, the green light in south direction will be ON for few seconds and all red lights in other directions will be ON. Whenever cnt=01 and dir=10 then yellow light (y1) will be ON for few seconds and when cnt=01 yellow light (y2) and pedestrian south will be ON and then dir is incremented by one and cnt is assigned to zero. So whenever cnt=00 and dir=11, the green light in west direction will be ON for few seconds Whenever cnt=01 and dir=01 then yellow light (y1) will be ON for few seconds and when and all red lights in other directions will be ON. Whenever cnt=01 and dir=11 then yellow light (y1) will be ON for few seconds and when cnt=01 yellow light (y2) and pedestrian west will be ON and then dir is assigned to 00 and cnt is assigned to zero. This sequence repeats and the traffic flow will be controlled by assigning time periods in all the four directions. Table I specifies the abbreviations used in TLC state diagram. Labeling for each lane is done by assigning the direction label in order to distinguish the outputs from each other with their states. In the traffic light controller program there will be two inputs namely clock and reset. When the two variables are „1" then the TLC will start working. Initially that is when reset is „0" then the red signal lights in all the directions will be ON and when reset is „1" , then the traffic light controller system will be on assigning cnt and dir variables to 00 where cnt and dir respectively represent the states and the four directions in the state machine.

V. RESULTS

5.1 RTL SCHEMATIC

The simulation is performed by Xilinx 12.4. The RTL schematic shown below. It consists of two input signals, clock signal, reset signal and stages.

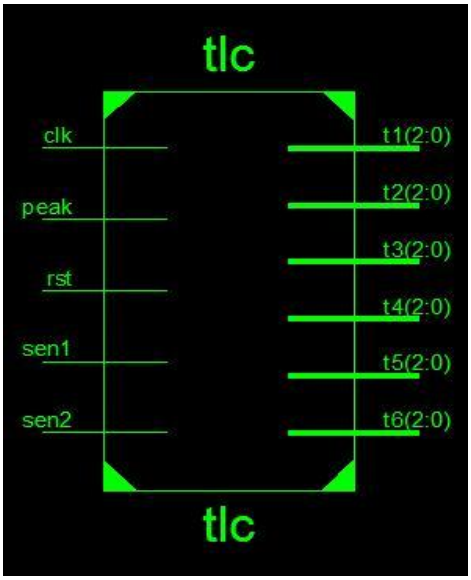

Fig. 3 RTL Schematic

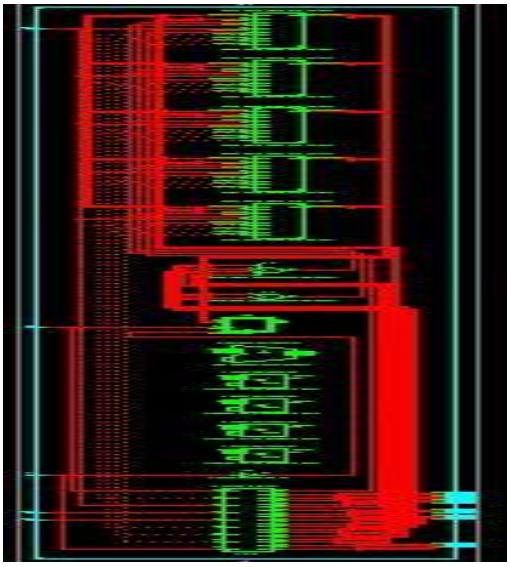

Fig. 4 RTL Schematics

5.2 SIMULATION RESULTS

Fig.5: Sensor1=0, Sensor2=0

The simualtion results are carried out by using ISE Xilinx. Here two inputs are indicated with Sensor1=0, Sensor2=0. and output is indicated with R. When the clock signal is"1" and reset signal is „0" the output will be displayed.

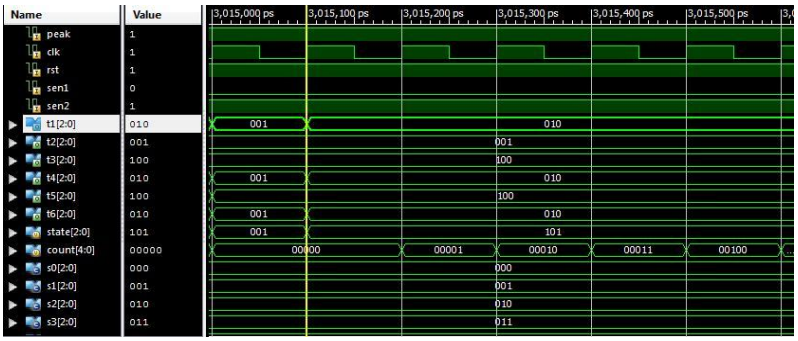

Fig. 6 Sensor1=0, Sensor2=1

The simualtion results are carried out by using ISE Xilinx . Here two inputs are indicated with Sensor1=0, Sensor2=1. And output is indicated with R. When the clock signal is"1" and reset signal is „0" the output will be displayed.

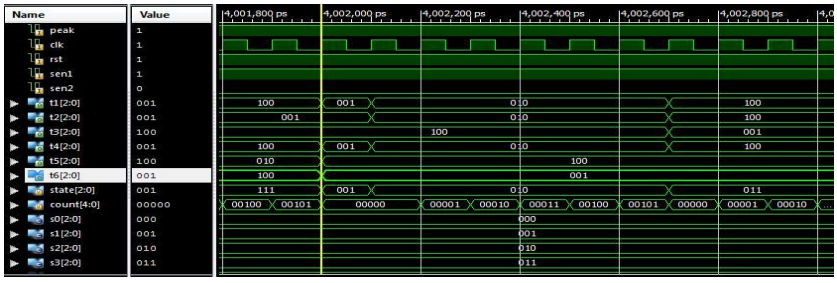

Fig. 7 Sensor1=1, Sensor2=0

The simualtion results are carried out by using ISE xilinx . Here two inputs are indicated with Sensor1=1, Sensor2=1 and output is indicated with R. When the clock signal is"1" and reset signal is „0" the output will be displayed.

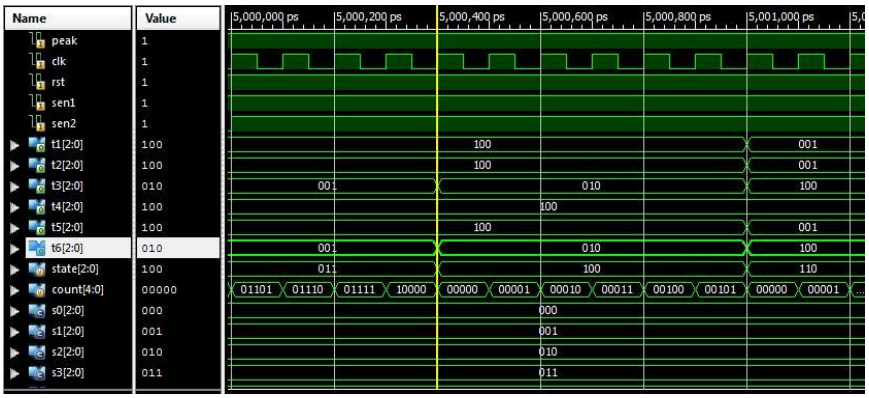

Fig. 8 Sensor1=1, Sensor2=1

The simualtion results are carried out by using ISE xilinx . Here two inputs are indicated with Sensor1=1, Sensor2=1. andout put is indicated with R. When the clock signal is"1" and reset signal is „0" the output will be displayed.

5.3 Synthesis results: The sysnthesis is performed in FPGA Spartan 3 prototype board and the images are shown below:

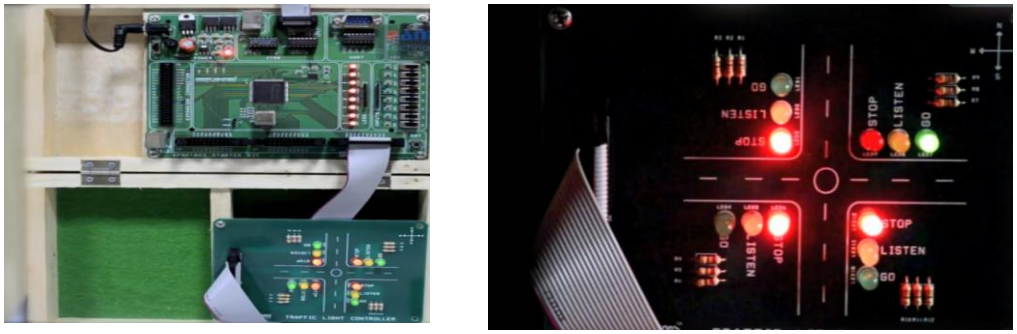

Fig.9 Synthesis on FPGA Spartan 3 family

VI .CONCLUSION AND FUTURE SCOPE

The simulated and synthesis results are shown above and this project can be implemented in real time. This work can be further extended to further FPGA families to implement speed grade and with aurdino processors and raspberry pi for improvement of parameters like speed for better performance.

VII ACKNOWLEDGEMENTS

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