Volume No.07, Special Issue No. (03), January 2018 www.ijarse.com



# DESIGN AND SIMULATION OF 4-BIT ADDERS USING LT-SPICE

## Kumari Amrita<sup>1</sup>, Avantika Kumari<sup>2</sup>

1,2B.Tech-M.Tech Student VLSI, Department of Electronics and Communication,
Jayoti Vidyapeeth Women's University, Jaipur (Raj.) (India)

#### **ABSTRACT**

Addition is the very fundamental arithmetic operation, which is implemented commonly. An adder is a circuit that sums the amplitudes of two input signal. These days the main domains of research are to reducing of size and a high-speed path logic system. Here in this paper, there is a similitude between various types of adders such as Ripple Carry Adder (RCA), Carry Look Ahead (CLA) and Full Adder (FA). As the technology develops we offer the low power expenditure, high tempo, and compact design. So, here between these adders, Researchers rationalize that Full adder is fast in speed but is massive in the area; Ripple Carry adder is compact in the area but is interminable in speed on the other hand in Carry Look-ahead Adder, it is in between of the extreme point of the time and the area complexity too. In this paper 4-bit adders are simulated on LT-spice XVII and AC Analysis concluded.

Keywords: RCA, CLA, FA.

#### **I.INTRODUCTION**

This paper consists of three types of an adder which are going to be explaining in this paper viz. Full Adder (FA), Ripple Carry Adder (RCA), Carry Look-Ahead Adder (CLA) [1]. These all three sort of adder are used for addition. In this paper, all three of the adders are outlined for the 4-bit operation. This paper is systematized into four segments. Firstly a brief study of given different types of adders with their architecture and working, which will be discussed in section II. In section III, the results obtained by spacious simulation on LT Spice of different adders. Consequence drew after comparing results and subsequent work proposed will be examined in section IV and in section V conclusion is discussed.

#### II. ARCHITECTURE OF ADDERS

#### 2.1FULL ADDER

A full adder made to overpower the drawback of the Half Adder. As the half adder cannot be chained together to add multi-bit numbers. It adds two input operand bits plus a Carry in a bit and outputs as Carryout bit and a sum bit [2]. The Sum out (Sout) of a full adder is the XOR of input operand bits A, B and the Carry in (Cin) bit Full adders can be cascaded to procreate any number of bits. Hence, raising the performance of the adder would

## Volume No.07, Special Issue No. (03), January 2018 www.ijarse.com

IJARSE ISSN: 2319-8354

vastly outbid the execution of binary operations. Basic 4-bit Full Adder architecture is depicted in fig. 1(a) and the input-output relation is shown in fig. 1(b). In this section, we will review the architecture of RCA and CLA.

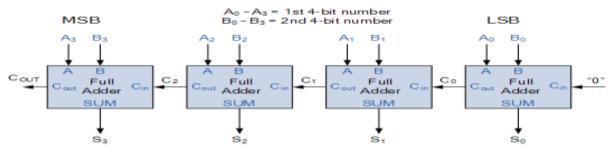


Fig.1:- Architecture of 4-bit Full Adder

#### 2.2RIPPLE CARRY ADDER

A full adder is the basic unit of ripple carry adder. It is known as a logic circuit in which the carry-out of each full adder is the carry in of the thrive next most prominent full adder. In a ripple carry adder the sum and carry out bits is not valid as long as the carry in of that stage occurs at any half adder stage. Interconnection of four full adders (FA) circuits is shown in figure 2 to provide a 4-bit ripple carry adder [1]. In this the input is from the right side because the first cell regularly signifies the least significant bit (LSB). Bits and in the figure represent the least significant bits of the numbers to be added. The sum output is characterized by the bits [2].

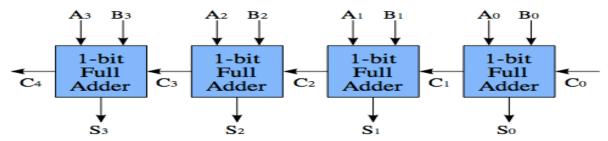


Fig.2:- Architecture of 4-bit Ripple Carry Adder

#### 2.3 CARRY LOOK AHEAD ADDER

Carry look-ahead adder is designed to dislodge the ripple carry delay and to vanquish the delay proposed by the rippling effect of the carry bits. This method based on the carry generating and the carry propagating functions of the full adder [3]. This adder is depending on the tenet of looking at the lower bits of the augends and added if a higher order is originated. This added detracts the carry delay by reducing the number of gates through which a carry signal must propagate. As seen in the ripple-carry adder, its limiting factor is the time it takes to propagate the carry [1]. Fig 3 shows that the carry look-ahead adder solves this problem by evaluating the carry signals in advance that are based on the input signals. The result is a diminish carry propagation time [3]. The carry look-ahead adder using the concept of propagating and generating the carry bit. It calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits[4].

Volume No.07, Special Issue No. (03), January 2018 www.ijarse.com



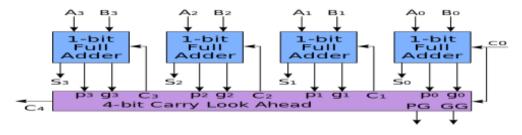


Fig.3:-Block diagram of 4-bit Carry Look Ahead Adder.

#### **III.TABLES**

**TABLE 1.Truth Table OF 4-bit Full Adder** 

TABLE 2.Truth table of 4-bit Ripple Carry Adder

INPUT			OUTPUT		
A	В	C-IN	C-OUT	S	
0	0	0	0	0	
0	0	1	0	1	
0	1	0	0	1	
0	1	1	1	0	
1	0	0	0	1	
1	0	1	1	0	
1	1	0	1	0	
1	1	1	1	1	

Input Data A			Input Data B			Addition						
A4	A3	A2	A1	B4	В3	B2	B1	С	S4	S3	S2	S1
1	0	0	0	0	0	1	0	0	1	0	1	0
1	0	0	0	1	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1	0	1	0
0	0	0	1	0	1	1	1	0	1	0	0	0
1	0	1	0	1	0	1	1	1	0	0	1	0
1	1	1	0	1	1	1	1	1	1	0	1	0
1	0	1	0	1	1	0	1	1	0	1	1	1

#### IV. SIMULATED RESULTS OF ADDERS ON LT-spice

#### 4.1.4-Bit FULLADDER

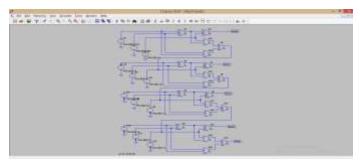


Fig.4:- 4-Bit full adder on LT-spice

## Volume No.07, Special Issue No. (03), January 2018

#### www.ijarse.com

IJARSE ISSN: 2319-8354

```
Circuit: * C:\Users\Amrita\Documents\LTspiceXVII\dbitFulladr.log

Circuit: * C:\Users\Amrita\Documents\LTspiceXVII\dbitFulladr.asc

WARNING: Less than two connections to node SUMI. This node is used by A5.
WARNING: Less than two connections to node SUMI. This node is used by A7.
WARNING: Less than two connections to node SUMI. This node is used by A7.
WARNING: Less than two connections to node COUT. This node is used by A7.
WARNING: Less than two connections to node COUT. This node is used by A12.
WARNING: Less than two connections to node COUT. This node is used by A12.
No AC stimulus found:

Set the value of a current or voltage source to "AC 1."

to make it behave as a signal generator for AC analysis.

Direct Newton itsesation for .op point succeeded.

Date: Tue Feb 29 10:34:12 2017
Total elapsed time: 0.109 seconds.

tnom = 27
temp = 27
temp = 27
method = trap
totaler = 0
tranpoints = 0
accept = 0
rejected = 0
matrix size = 41
fillins = 0
natrix size = 41
fillins = 0
natrix size = 41
fillins = 0
accept = 0
rejected = 0
matrix size = 41
fillins = 0
accept = 0
accept = 0
rejected = 0
matrix compiler: 1.72 in object code size
```

Fig.5:-Simulation Window of 4-Bit full adder on LT-spice

#### **4.2RIPPLE CARRY ADDER**

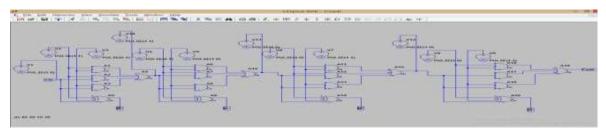


Fig.6:- 4-Bit Ripple Carry Adder on LTspice

```
Complete XVII read

The The Complete XVII read

A Complete XVII re
```

Fig7:- Simulation Window of 4-Bit Ripple Carry Adder on LT-spice.

#### 4.3 CARRY LOOK AHEAD ADDER



Fig8:- 4-Bit carry look ahead adder on LTspice

## Volume No.07, Special Issue No. (03), January 2018 www.ijarse.com



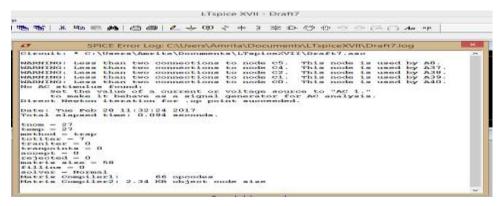


Fig9:- Simulation Window of 4-Bit carry look ahead adder on LT-spice.

#### V. COMPARED RESULTS OF ADDERS

	4-bit FA	4-bit RCA	4-bit CLA
Total elapsed time	0.109 sec	0.203 sec	0.094sec
_			
Tnom	27	27	27
Temp	27	27	27
Method	trap	trap	trap
Totiter	6	5	7
Traniter	0	0	0
Tranpoints	0	0	0
Accepts	0	0	0
Rejected	0	0	0
Matrix size	41	41	58
Fillins	0	0	0
Solver	normal	normal	normal

#### VI. CONCLUSION

In this paper three 4-bit adders Full Adder, Ripple Carry Adder and Carry Look Ahead Adders respectively simulated on LT-spice XVII and analyzed all the three adders have different elapsed time and other characteristics that are shown in comparison table. By analyzing comparison table it seems that 4- bit Carry Look Ahead has less total elapsed time when its contains more matrix size as compared to 4-bit full adder and 4- bit ripple carry adder. Due to it Carry Look Ahead Adder is better than bothadders.

Volume No.07, Special Issue No. (03), January 2018 www.ijarse.com

IJARSE ISSN: 2319-8354

#### **REFERENCES**

- [1] "DESIGN OF EXTENDED 4-BIT FULL ADDER CIRCUIT USING HYBRID-CMOS LOGIC",ISSN 2394-739X Vol.03, Issue 3,Pages: 38-44.(S.Varalakshmi, March Volume 3, Issue3)
- [2] "Analysis of Various Full-Adder Circuitsin Cadance." International Journal of Computer Applications (0975-8887), NCPSIA 2015. (Manjunath K M)
- [3] "Design and Implementation of Ripple CarryAdder using area efficient full adder cell in 180nm CMOSTechnology." International Journal of Science, Engineering and Technology Research (IJSETR), Vol. 3, Issue 5, May 2014, Pages: 14-19 (2016).
- [4] "(Amita, Mar-Apr, 2014)." *IOCR Journal of Electronics and Communication Engineering (IOSR-JECE)*.e-IISN: 2278-8735. Volume 0, Issue 2, Ver. VII (Mar-Apr 2014), pp92-95.