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Multi Level Inverters with Its Detailed Depiction and Elimination of Higher Order Harmonics With Switching Losses Calculations Using MATLAB

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ABSTRACT

The emerging trends in the field of power electronics have made many advancements in the power sector in which the multilevel inverters are the pre-dominating one. We have used the two level inverters to convert DC to AC in the hoary days but now the multilevel inverters have replaced them and paved a path for the evolution of power sector. The detailed description of multi level inverters with their working, advancements, advantages has been described herein. The MATLAB model for the multilevel inverters has been developed and the elimination of the higher order harmonics have been performed by PWM and filters. This paper also calculates the switching losses in the multilevel inverter.

Keywords: Multilevel-Inverter, MATLAB, PWM, Filters, harmonics, switching losses.

I.INTRODUCTION

The renewable energy sources has been tremendously increasing its production out of all those renewable energy sources solar is popular and it needs an inverter for the conversion. The multilevel inverters are the advancement in power electronics.

II.STRUCTURES OF THE MULTI LEVEL INVERTERS

The multi level inverters can be classified as three major types on the basis of the switch connectivity and type of switch used. They are flying capacitor inverter, diode clamped inverter and the cascaded H-bridge inverter.

2.1Flying Capacitors

The figure 1 shows the structure of a flying-capacitor type converter. In this type of inverters we are going to use the capacitors and diodes along with the DC voltage source. This has an advantage that filter is unnecessary and the control of active and reactive power flow is possible. It also has drawback as the number of capacitors is very high, the control of system becomes difficult with the increase of diode legs.

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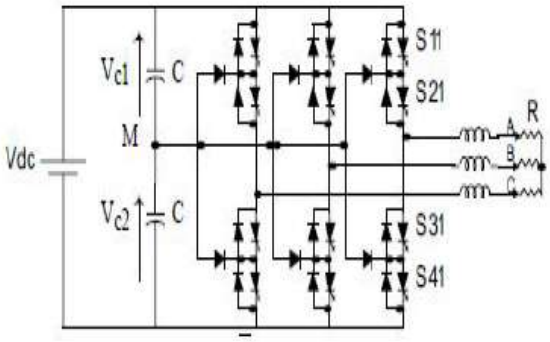

Fig 1topology Of Three Level Inverter

2.2Cascaded-Type Multilevel Inverter

Figure 2 represents the structure of a three-phase cascaded-type converter with separate dc sources. This type of converter does not need any transformer clamping diodes, or flying capacitors. Each bridge converter generates three levels of voltages and can be
in star or delta.

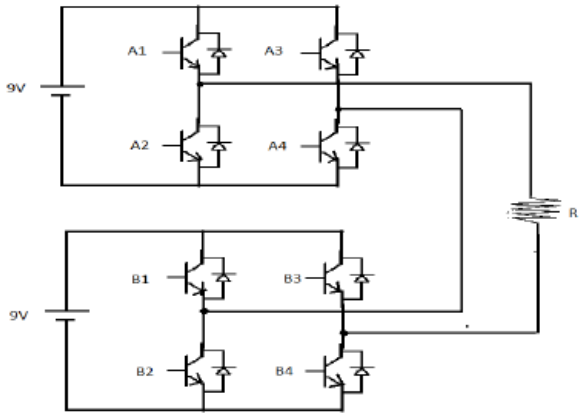

Fig 2. Schematic diagram of a 5 –level cascaded type converter

It has the following advantages:

- It uses fewer components than the other types.
- It has a simple control, since the converters present the same structure.

However, the main drawback is that it . needs separate dc sources for the conversion of the active power, which limits its use.

2.3Diode-Clamped Multilevel Inverter

This is used in static VAR compensation, variable speed motor drives, and high-voltage system interconnections. A three phase six-level diode clamped inverter is shown in Figure. An m level inverter leg requires 2(m-1) switching devices and (m-
1)(m-2) clamping diodes. For a three-level inverter, m=3, so it needs four switching devices and two clamping diodes per leg as shown in Figure 3,

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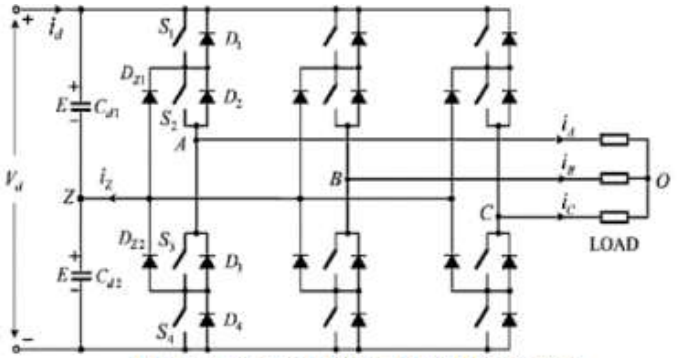

Fig 3. A 3- level diode clamped inverter

III.CIRCUIT OPERATION

3.1Overview of Circuit

A five level cascaded multilevel inverter is chosen for simulation. For a five level cascaded multilevel inverter, two H – bridges are modeled in simulink. According to the expected waveform, MOSFETs are grouped into categories. Each group is triggered with a pulse generator.

Model of a 5 – Level Cascaded Multilevel Inverter (CMI)

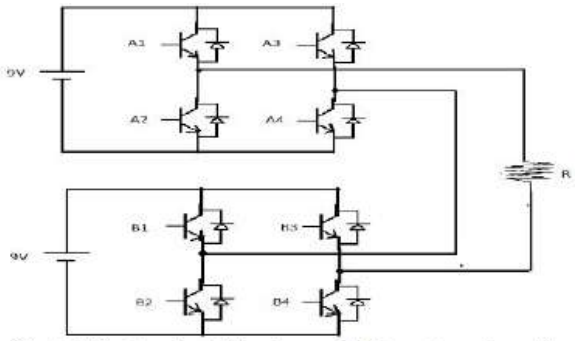

Fig 4 A five level multilevel cascaded inverter schematic

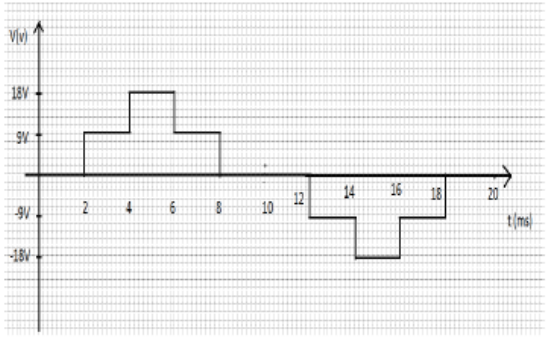

Fig 5 Output of the multilevel inverter

The table 1 gives information about the operation of the MOSFET'S in the groups to give the desired output. In this the two H-Bridges are grouped with the 8 MOSFET's and those are switched ON for certain period of time. Total number of groups that are used here are in number 4 and they are classified as group1, 2, 3, and 4. In each

the groups some/all MOSFET's function (be in ON state) for a certain period. This can be used for successful estimation of the waveform. The voltage levels may not be same for each group and they may change from increment or a decrement fashion.

Table-1: Group of switches with respect to voltage levels

Group	Voltage level	Conducting switches
1	9v	B1 B4A4
2	18v	B1A1 B4A4
3	9v	A3 A2B2
4	18v	A3B3 A2B2

The numbers of switches i.e. MOSFET's to be in ON position depends on the group that we have chosen and that indirectly depends on the desired waveform.

3.2OPERATION

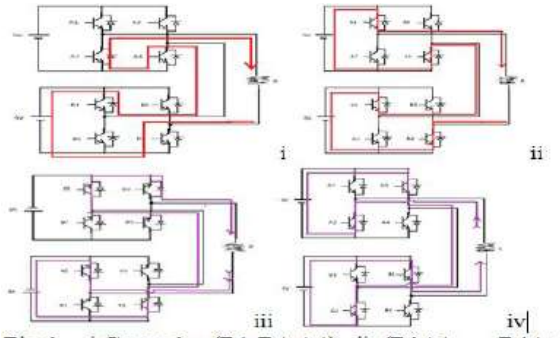

Fig 6. i.Group1 – (B1-B4-A4) ii. (B1A1 B4A4 iii. (A3 A2B2) iv.(A3B3 A2B2)

IV. SWITCHING LOSSES AND HARMONICS INVESTIGATIONS

Waveforms of practical inverters are non-sinusoidal and contain certain harmonics. Harmonic contents present in the output of a dc-ac inverter can be eliminated either by using a filter circuit or by employing Switching losses become a dominant part of the total inverter losses at higher switching frequencies. Therefore, optimization of the switching frequency is necessary to reduce both THD and switching losses in the power devices.

4.1Multilevel Inverters

The cascaded inverter uses a large number of separate dc sources for each of the bridges. However, in the diode clamped topology, all devices are switched at the fundamental frequency resulting in low switching losses and high efficiency. Other main features of this topology are controlled reactive power flow between source and load, much better dynamic voltage sharing

among switching devices and simple topological structure. Therefore, diode clamped inverter topology is considered here for study. The control logic is simple, especially for back-to-back inter-tie connections of two

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systems. However, it requires a large number of clamping diodes for a large number of output voltage levels. To produce an m-level output phase voltage, (m-1) switches are required for each half phase leg, a total of (m-1) dc link capacitors for energy storage and (m-1)*(m-2) clamping diodes for each phase leg.

***4.2* Switching Losses Calculations:**

Consider a single MOSFET switch connected across a dc voltage of value Vdc . Current through switch during 'on' time is considered as Idc . Figure 6.1 shows the waveforms of the voltage across current through and the the switch when it is operated at a switching frequency of Fs = 1/Ts , where T s is the switching period. To simplify the expressions, the switching waveforms are represented by linear approximations. In the figure 7, v M and i M are the voltage across and the current through the MOSFET.

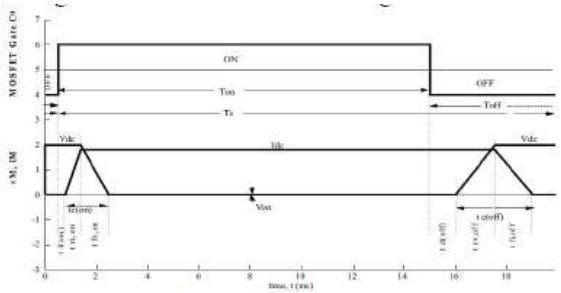

Fig 7 : The waveforms of the voltage across and the current through the switch

Switching losses can be calculated from the turn-on and turn-off characteristics of the devices. Instantaneous voltage and current during turn on time tc(on)

$$v(t) = V_{dc} - (V_{dc} - V_{on})*(t/t_{c(on)}); \qquad 0 < t \leq t_{c(on)} \qquad (1)$$

$$i(t) = I_{dc} * (t/ t_{c(on)}); \qquad 0 < t \leq t_{c(on)} \qquad (2)$$

Instantaneous power during the interval tc(on) is

$$p(t) = v(t)*i(t)$$

$$=\{V_{dc} - (V_{dc} - V_{on})*(t/t_{c(on)})\}* \{I_{dc} * (t/ t_{c(on)})\}$$

$$=\{V_{dc} *I_{dc} * (t/ t_{c(on)}) \} - (V_{dc} - V_{on})*(t^2/t_{c(on)}^2) \qquad (3)$$

and energy dissipated during this interval is t c(on) ,

$$E_{c,on} = \int[\{V_{dc} *I_{dc} *(t/ t_{c(on)})\}- (V_{dc} - V_{on})*(t^2/t_{c(on)}^2)]\, dt \;\; 0 \text{ to } t_{c(on)}$$

$$E_{c,on} = (V_{dc} *I_{dc} * t_{c(on)})/2 - (V_{dc} - V_{on})* I_{dc} * t_{c(on)}/3$$

$$= (V_{dc} *I_{dc} * t_{c(on)})/6 - (V_{on} * I_{dc} * t_{c(on)})/3 \qquad (4)$$

and during turn-off transition, of t c(off) , the current falls from I dc to zero and Vdc rises lineary to Vdc. The instantaneous voltage and current during this period are

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$$v(t) = V_{on} + (V_{dc} - V_{on})/t_{c(off)} \quad (5)$$

$$i(t) = I_{dc} - I_{dc}/t_{c(off)} \quad (6)$$

The instantaneous power dissipated during the interval tc(off) is

$$p(t) = v(t)*i(t)$$
$$= \{V_{on} + (V_{dc} - V_{on})*(t/t_{c(off)})\}* \{I_{odc} - I_{dc} * (t/ t_{c(off)})\}$$
$$= V_{on}*I_{dc} + (V_{dc}-V_{on})*I_{dc}*(t/t_{c(off)}) - V_{on}*I_{dc}*(t/t_{c(off)}) -$$
$$(V_{dc} - V_{on})*I_{dc}*(t^2/t_{c(off)}^2) \quad (7)$$

Hence, the energy dissipated can be found as tc(off)

$$E_{c,off} = \int[V_{on}*I_{dc} + (V_{dc} - V_{on})*I_{dc}*(t/t_{c(off)}) - V_{on}*I_{dc}$$
$$*(t/t_{c(off)}) - (V_{dc} - V_{on})*I_{dc}*(t^2/t_{c(off)}^2)]\,dt \qquad 0t_{c(on)}$$
$$= (V_{dc}*I_{dc}*t_{c(off)})/6 - (V_{on}*I_{dc}*t_{c(off)})/3 \quad (8)$$

Therefore, with the devices having short switching times, it is possible to operate them at a higher switching frequency thus avoiding excessive switching power losses in the device.

V. SIMULATION RESULTS

5.1Circuit implementation in MATLAB

The MATLAB simulated circuit for the Switching Losses and Harmonics Investigations in Cascaded Multilevel Inverter is shown in the figure 8 and this figure consists of two MOSFET H-bridges with two separate DC supplies which are fed to the two bridges, This also consists of an R-load.

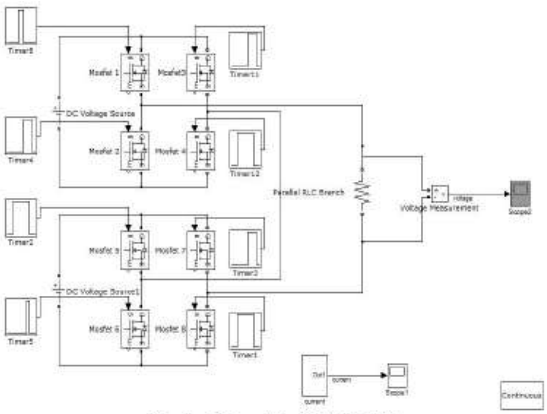

Fig 8 : Circuit in MATLAB

Each MOSFET is triggered at certain intervals of time and those intervals of time is given in the below table 2.

The results of the above circuit are shown and that is as in here.

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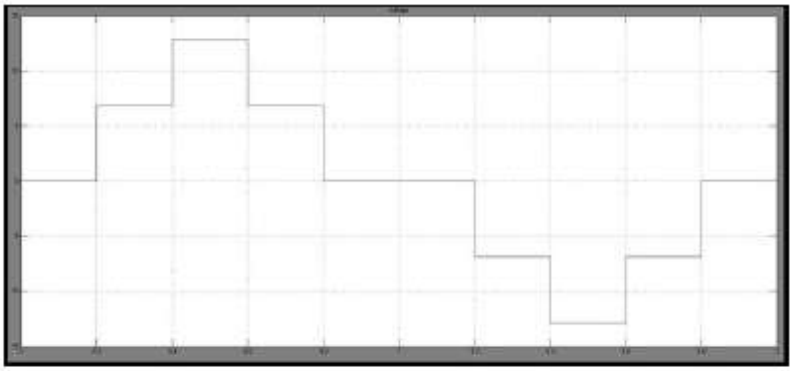


Fig 9 : Staircase output obtained at the load

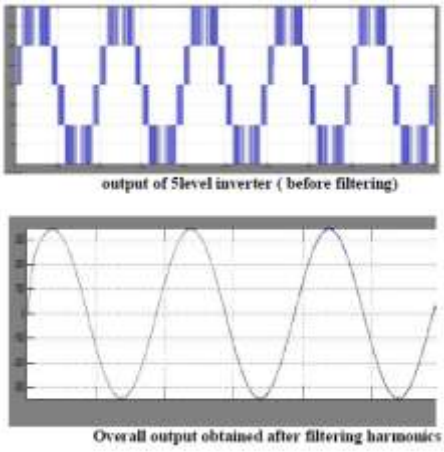
The level of DC-supply that is maintained is 9V while the load here is 1ohm. The switching losses depend on the time for which the MOSFET has been ON. The switch that is ON for more time may suffer more switching losses while the switch that is On for the less time suffers with the less switching losses. All the switches are calculated with the ON and OFF time taken from their timers. They are as follows

Table 2: Switching losses

S no	Switch name	Losses (in mJ)		Average Losses (mJ)
		ton	toff	
1	A1	1.35	12.15	6.75
2	A2	4.05	18.90	11.48
3	A3	4.05	18.90	
4	A4	4.05	18.90	
5	B1	4.05	18.90	
6	B2	4.05	18.90	
7	B3	1.35	12.15	6.75
8	B4	4.05	18.90	11.48
			Total losses	9.115

The above denotes that the switches A1,B3 are the switches that suffer with the low losses while the other switches are suffering with the high losses and thus these switches can be given the rating in order to overcome the losses. The harmonics are calculated or estimated by using the diode clamped inverter.

VI. RESULTS



VII.CONCLUSION

The multi level inverter is designed by taking two H-MOSFET bridges with number of levels as five. The switching losses of the multi level inverter is calculated and the harmonics are investigated and then the higher order harmonics which are of greater than 500 Hz are eliminated by using the low pass filter and then better sinusoidal signal is obtained. Thus this made the difference between an ordinary inverter and the multilevel inverter by cascading the H-bridges made of MOSFET's.

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