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Low Power Dynamic Logic Resistive Keeper Circuit Using N-Channel FinFET

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ABSTRACT

Dynamic logic is most area effective technique for designing VLSI circuit. However, due to lower noise margin of dynamic logic performance is not auspicious. This research proposes a N-FinFET based resistive keeper circuit using 45nm PTM FinFET model which reduces the contention between pull down network and keeper device using the special feature of four terminal FinFET (capacitance merging among both gates of four terminal FinFET). Proposed resistive gate voltage can control the strength of keeper device which reduces the leakage power and time delay. Extensive simulation results using LTSpice tools demonstrate the validity and superiority of the introduced circuit.

***Keywords*—Dynamic logic; N-FinFET; Resistive keeper; Leakage power;**

I. INTRODUCTION

In VLSI design, better speed, high noise margin and low power logic circuits design is more discretion work. Dynamic logic has most comparative logic where the half number of transistor being used compared to traditional logic circuits [1- 2]. Dynamic logic circuits contain a pull down network, a keeper device and a footer device. A clock pulse is used for the operation of dynamic logic. However, a parasitic capacitance has situated just before the output of circuits and it stores the voltage of output to control the output states [3-4]. There are two phases in dynamic logic precharge and evaluation phase. When the Clock is high of the logic circuit is called evaluation phase and low clock is called precharge phase. The performance of dynamic logic is not so good because of dynamic node is not always connected to VDD [5]. A keeper device (PMOS) has been employed to reduce the leakage power through pull-down network. If any input of the PDN is high, stored voltage of the capacitor will be removed and will enroll the keeper device ON. However, the ON stage of keeper device remains ON until the voltage of output goes to minimum voltage and this time difference generates a contention between pull down network and keeper transistor where it demotes the performance of power consumption, time delay and noise margin. Double gate FET has been used to reduce the short channel effects and drain induced barrier lowering (DIBL) where both gates are combined electrically [6-7]. FinFET is the most expected candidate which is reliable to generation for good performance comparing to the other double gate

devices [8]. This device can reduce the short channel effects by controlling both gates, doping concentration and thicker oxide.

Independently biased of four terminals FinFET and combined of two gates three terminal FinFET are shown in Fig. 1. The composition of FinFET can be optimized from,

$$W = 2 \times n \times H \qquad (1)$$

Width of the FinFET is calculated by the number of the fins (n) and height of the fin (H). n and H these parameters are used to control the FinFET gate and to improve the noise margin. A PMOS keeper device has been used in the dynamic logic circuits to reduce the leakage power, charge distributing. So, we need to design a keeper device for increasing the noise margin of the dynamic logic. However, proper keeper sizing of FinFET based domino logic design is difficult for increasing the noise margin of dynamic logic circuits. This work design a N-FinFET based resistive gate keeper circuit which uses the special feature of (capacitance merging among both gates of four terminal FinFET) FinFET to attain lower power consumption and high performance.

A. Dynamic Logic Circuits

The clocking of dynamic circuits1 can be classified into two categories: non blocking and blocking. With non blocking dynamic circuits, the evaluation clock arrives before critical path data transitions. The advantages of using non blocking evaluation clocks are that the flow of critical data is not blocked by the arrival of evaluation clocks and that some amount of clock skew may be tolerated [1]. The lower bound on the critical path delay is the time it takes for every gate along the critical path to evaluate. In order to use non blocking clocks, inputs to each dynamic gate must be monotonically rising. Domino logic [2] guarantees this constraint by pairing inverting static gates with each dynamic gate such that all inputs to dynamic gates precharge low. Enforcing monotonically rising inputs to dynamic gates may require logic duplication.

In contrast to non blocking dynamic circuits, the evaluation clock of a blocking dynamic gate rises after the latest input has settled. The delayed clock into each dynamic gate can be generated by using a delay matching circuit or a “speed-independent” self-timed circuit [3]. Blocking dynamic circuits have been used in memory designs [4]–[6], control logic [7]–[11], and data paths [12]–[16]. Logic duplication is not necessary since all inputs to a dynamic gate are guaranteed not to change during evaluation. The area and power savings from not duplicating logic is diminished by the number of delayed clock generation circuits needed. In general, each dynamic gate can receive a custom-tuned clock depending on the worst case input arrival time to that gate. To save area at the expense of overall delay, all dynamic gates in a logic level can receive the same delayed clock, whose delay is set by the latest input data arrival time to that level. For a blocking dynamic logic pipeline, the lower bound on the worst case delay is the sum of the evaluation time of each gate along the critical path. It is worth noting that the evaluation time is not necessarily the time it takes to make a full transition. Instead, all that is required is for each dynamic gate to sample its inputs correctly. In this paper, we investigate the clocking of blocking dynamic circuits and explore its impact on the delay versus margin tradeoff for each gate in a logic network.

B. FinFET Basics

With advanced geometry planar FET technologies, such as 20nm, the source and the drain intrude into the channel, making it easier for leakage current to flow between them and making it very difficult to turn the transistor off completely. FinFETs are named so because they are 3d structures that projects out of the substrate and resemble a fin. The 'fins' form the source and drain, effectively providing more volume for the same area than a planar transistor (see Figure 1. comparing planar FET and FinFET). The gate wraps around the fin, providing better control of the channel and allowing very little current to leak through the body when the device is in the 'off' state. This, in turn, enables the use of lower threshold voltages and results in better performance and power.

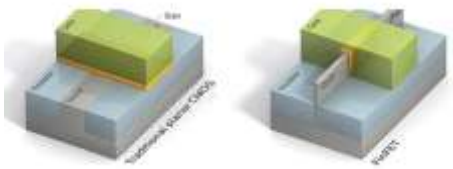

Fig. 1 Planar CMOS and FinFET

The industry's experience with 20nm has paved the way for an easier transition to FinFET processes. Many of the tool improvements can still be applied, but the handling of FinFETs does require a few more changes; for example, SPICE BSIM-CMG models had to be created to add the 3D effects. It is also true that, with 3D transistors, capacitance becomes a primary concern. EDA tools must build in high resistance interconnect optimization in order to mitigate these capacitive effects. Layer awareness is also essential to provide optimal metal layer assignment during routing of the design. Another interesting trend to note is the cost variation as the size decreases. As the size decrease lower than 28nm, there is a price increase unlike the gradual price decrease with the size reduction up to 28nm. Multi-gate or tri-gate architectures, also known as FinFET technology is a promising technology that lead to creation of even smaller and efficient microprocessors and memory cells. This improves performance and battery life of computing devices. The technology came into existence as a result of relentless increase in the levels of Si process manufacturing and integration. This has resulted in change in many design parameters. Fundamentally the feature sizes have reduced to enable more devices to be fabricated within a given area. However, other figures such as power dissipation and line voltages have also reduced along with increased frequency performance. The taxonomy is presented in the form of a 2D matrix with manufacturing processes on one axis and design parameters on the other axis. The taxonomy focuses on the impact of various manufacturing processes on the design parameters. The categorization of patents/patent applications, related to FinFET technology was done on the basis of manufacturing processes and the affected design parameters. The set considered for the analysis comprised of 12,769 patents/patent applications.

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II.EXISTING SYSTEM

A. *Selecting a Template (Heading 2)*

Both gates are tied together is denoted by three terminal FinFET. Traditional three terminal FinFET based domino logic is shown in Fig. 2. PFET keeper device, a precharge device, an inverter contains in dynamic logic. When the clock is Low, dynamic node keeps the high state and isolates all states from domino node. Foot switch turns ON in evaluation phase where domino node is discharged and it depends on the input values. Both phases are shown in Fig. 3.

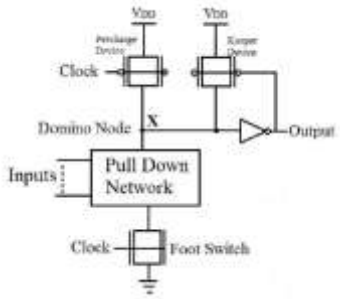

Fig. 2 The existing domino logic using traditional three terminals FinFET

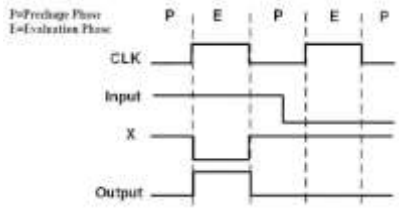

Fig. 3 The Wave shapes for traditional domino logic circuits using three terminals FinFET.

Until output voltage reaches minimum voltage to turn off the keeper device, a contention occurs between keepers and pulls down network. This contention provides a poor noise margin. Resulting lower time delay and high power consumption. The reducing of this contention is more challenging in sub-100nm model due to leakage power is continuously increasing and needs large keeper transistors. However, keeper design with FinFET device is reliable for continuous scaling and high performance. Presented by some researchers which could not implement for wide-fan-in logic operation.

III. PROPOSED DESIGN

Basically, this work designed a resistive gate with four terminals N-FinFET which is shown in Fig. 4. In FinFET based domino logic, variability of fin and oxide thickness is very important. The peak value of back gate of P increases when oxide thickness and fin thickness increase. Due to low sensitivity of peak value, designing keeper will be easy. Thinner fin thickness of P increases the peak value and time constant of differential

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waveform. This differential voltage pulse decreases the drive current of N-type resistive gate, which is needed at the beginning of the evaluation phase. It reduces the contention between pull down network and keeper.

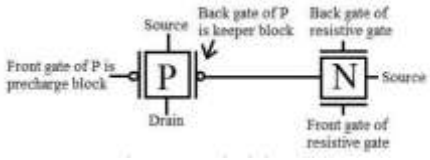

Fig. 4 Structure of proposed resistive keeper circuit.

The input capacitance of three terminals FinFET is higher than the four terminals FinFET. For that, four terminal FinFET decreases power as a substitute of three terminals FinFET. The structure of the proposed domino logic made by four terminal FinFET where P and N are used as P-FinFET and N-FinFET which is shown in Fig. 5. FG1 of P performs as precharge gate and BG1 of P performs as keeper device. The resistive gate of this design is N and it forms a four terminal FinFET with P.

There are two gates of N as FG2 and BG2. FG2 is linked with domino node and BG2 linked with output node. Low clock called precharge phase and that time dynamic node charged to VDD which is shown in Fig. 6. At this time, the four-terminal resistive gate of N acts as single gate mode due to BG2 is Low and FG2 High state. The feedback of N is connected to the BG1 of P. Both gates of N acts as double gate mode where both gates are prejudiced Low. The dynamic node turns high to Low state through PDN in evaluation phase and BG2 of N is charged and linked the BG1 of P immediately.

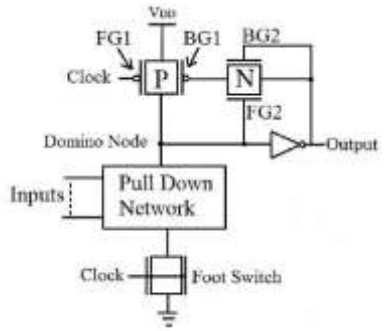

Fig. 5 Structure of proposed domino logic based resistive keeper circuit.

When the clock turns Low to high various types of waveform is made in BG1, which decreases the gate to source voltage of BG1. Resulting to weaken P branch than the pull-down network. However, it minimizes the controlling corrosion of P by decreasing and increasing the threshold voltage and presented design induces its benefits.

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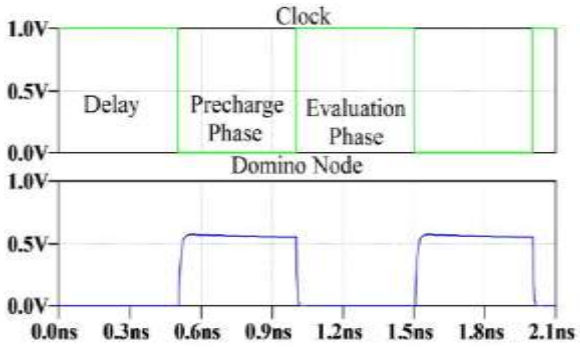

Fig. 6 Wave shapes of clock versus domino node

Simulation results are presented using LTspice simulation tool by employing 45nm FinFET from Arizona State University Predictive Technologies Model (ASU-PTM) PTM model. FinFET parameters contain 45nm channel length; 1.5nm oxide thickness and 8nm fin thickness were applied in this design. Also, 3nm high fin (HFIN) and 2×1016eV channel doping were used in this work. The simulation result presents power consumption, noise margin, and delay for the proposed circuit as well as standard domino logic circuits with respect to several existing models for the same noise margin and VDD is 1V. Table. 1 shows the proposed model demonstration of the power saving and high performance.

IV.RESULT AND DISCUSSION

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In this newly created file, highlight all of the contents and import your prepared text file. You are now ready to style your paper; use the scroll down window on the left of the MS Word Formatting toolbar.

This research presented a new model of dynamic logic using four terminal FinFET. N-FinFET is used as resistive gate that forms with precharge device. Gate -source voltage of keeper device is low at the initial time of evaluation phase. The dynamic logic is designed with different logic gates with different nano meter technologies. The dynamic logic based resistive keeper circuit is used to reduce static power dissipation. The simulation results are performed in LTSpice EDA tool.

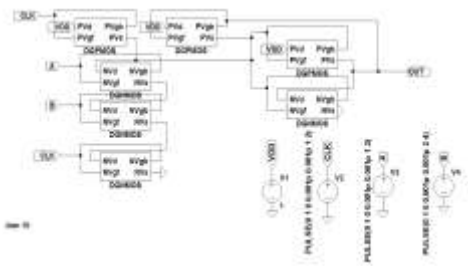

Fig. 7 Schematic diagram of Traditional domino logic using three terminal FinFET

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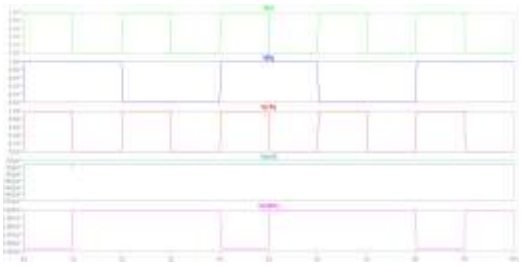

Fig. 8 Output waveform of Traditional domino logic using three terminal FinFET

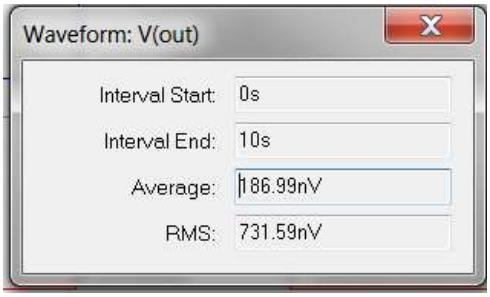

Fig. 9 Average and RMS voltage of Traditional domino logic using three terminal FinFET

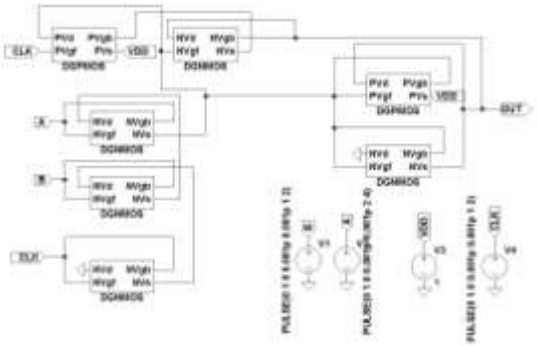

Fig. 10 Schematic diagram of proposed domino logic and FinFET based resistive keeper circuit

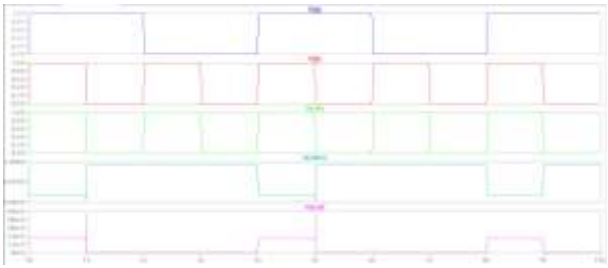

Fig. 11 Output waveform for proposed domino logic and FinFET based resistive keeper circuit

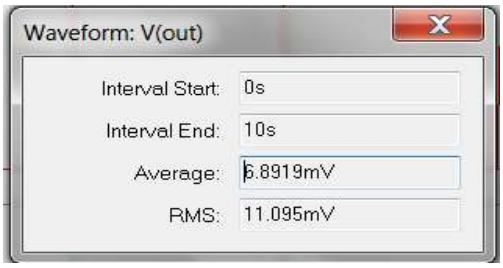

Fig. 12 Average and RMS voltage of proposed domino logic

TABLE I. COMPARISON OF THREE AND FOUR TERMINAL FINFET

	Comparison of three and four terminal FinFET	
	Average Output Voltage	***Output RMS Voltage***
Three Terminal FinFET	186.99nV	731.59nV
Four Terminal FinFET	6.891mV	11.095mV

V.CONCLUSION

This research presented a new model of dynamic logic using four terminal FinFET. N-FinFET is used as resistive gate that forms with precharge device. Gate -source voltage of keeper device is low at the initial time of evaluation phase. The dynamic logic is designed with different logic gates with different nano meter technologies. The dynamic logic based resistive keeper circuit is used to reduce static power dissipation. The simulation results are performed in LTSpice EDA tool.

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