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Perturbation On-Time (POT) Technique to improve Power Factor Correction and Low THD

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ABSTRACT

The input line current is basically shaped by the power factor correction (PFC) controller to be the replica of the input line voltage and exactly in phase with it. The proposed perturbation on-time technique reduces total harmonic distortion (THD) and improves the power factor in the power factor correction (PFC) controller. The boundary conditions in the PFC controller are changed in order to get the better power factor and reduced total harmonic distortion and besides,the adaptive controls of the minimum off time by the proposed inhibit time control improves efficiency even at low ac input voltage. The Power factor of 0.989 with high efficiency of 95% is obtained. This process have achieved a low Total harmonic distortion of 6%

Index Terms—Inhibit time (IT) control, perturbation on time (POT),power factor correction (PFC), ultra high voltage (UHV),Spike-free circuit.

I. INTRODUCTION

During the past two decades, power electronics research has focused on the development of new families of hard- and soft-switching converter topologies used in the design of dc–dc and ac–dc converters with active power factor corrections (PFC's). The goal is to design high-efficiency and high-power density converters with improved power factor and low electromagnetic interference (EMI). In recent years, as the new standards such as IEC 1000-3-2 became compulsory regarding limiting the total harmonic distortion (THD) and input power factor in power electronic circuits, researchers are actively seeking ways to shape the line current waveform to achieve THD and power factor that comply with international standards. Active PFC circuits that use pulse width modulation (PWM) switch-mode topologies such as the boost, buck–boost, and their derived ones have been used dominantly.

The steady-state analyses for a large number of such topologies are well documented, and their various dc control characteristics are well known. In addition to the steady-state behavior, the dynamic behavior is equally important and critical when it comes to the design of a robust control system for such converters. Control theory is applied to improve the performance of power electronics circuits such as the transient response, control accuracy, regulation capability and to reduce the effects of parameter variations as well as other disturbances. Over the last two decades, several control schemes have been presenting various modeling techniques for the power stage.

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With the increasing demand for power from the ac line and more stringent limits for power quality, power factor correction has gained great attention in recent years.Power Factor Correction (PFC) technique continues to be attractive research topic with several effective regulations being reported. Conventional cascade of two stage topology can achieve good performance such as high power factor and low voltage stress, but it usually suffers from high cost and increased circuit complexity. Many single-stage PFC AC/DC converters have been proposed that can be applied cost-effectively. However, it's well known that in single stage topologies, the voltage across the bulk capacitor can not be controlled well due to the fact that only one switch and control loop are used. Moreover, the storage capacitor voltage varies widely with the input voltage and load variation, especially when the PFC operates in

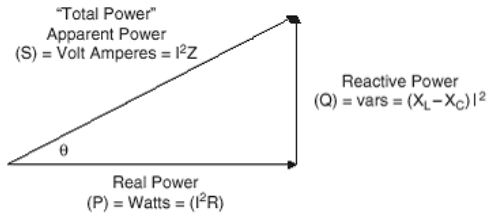

Fig.1 Power Factor Triangle (Lagging)

DCM mode while DC/DC stage operates in CCM mode. Finally, the storage capacitor voltage will increase to be unbearable under light load condition.

Power Factor Correction (PFC) converter is necessary for many electronic types of equipment to meet harmonic regulations and standards, such as IEC 1000-3-2. For low power applications, single-stage PFC converter is a better choice considering cost and performance. In single switch topologies, a PFC cell is integrated with a DC/DC conversion cell and both cells share active switches and controller. But those topologies suffer from high voltage and high current stresses. But most of those methods will bring high distortion to line current waveform, resulting in reduced power factor.

The conventional PFC as depicted in Fig. 2 uses the boost topology with the boundary conduction mode (BCM) technique [1]–[5] to guarantee high PF value due to the in-phase line voltage and inductor currents. The conventional BCM technique can simplify circuit complexity but have high root-mean square (rms) current in the inductor. In the conventional BCM technique, the error amplifier (EA) can set up the output power level through the error signal *V*EAO. The comparator compares the saw-tooth signal with *V*EAO to determine the on-time period.

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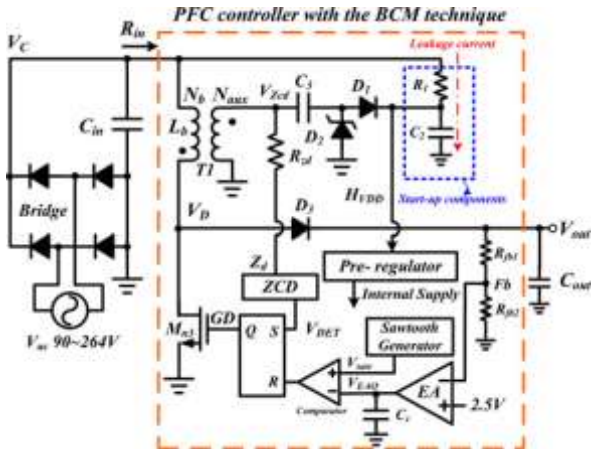

Fig 2: Conventional PFC with BCM Technique

On the other hand, the off-time period is determined by the detection of the zero inductor current. That is, the power N-type MOSFET is inherently turned ON with a zero current switching (ZCS) mechanism. The switching loss is effectively decreased because the diode reverse recovery is eliminated. Therefore, an accurate zero current detection (ZCD) circuit is needed in the ZCS operation for high efficiency.

Here, the energy in the auxiliary windings can be used to find the zero current condition by the ZCD circuit in order to avoid facing ultrahigh voltage (UHV). The ZCD circuit will detect the zero inductor current from the auxiliary windings through the signal *V*DET to trigger the set-reset (SR) latch high to restart the next switching cycle. Thus, the auxiliary windings with the number of *N*aux turns are used to detect the zero inductor current if primary windings with the number of *Nb* turns have an equivalent inductor value of *Lb*. Once the power N-type MOSFET is turned ON, the inductor current *i*Lb is equal to the line current *i*ac which is proportional to the product of the line voltage *V*ac and the on-time value.

$$i_{L_b} = i_{\text{ac}} = \frac{V_c}{L_b} \cdot t_{\text{on}} \text{ where } V_c = |V_m \sin \omega t|$$

Vc is the voltage across the input capacitor *C*in and *Vm* is the peak value of the input ac source. Therefore, if the values of *Vm*, *Lb*, and *t*on are constant, the line current will be in phasewith the line voltage) with a constant *M*

$$i_{\text{ac}} = M \cdot \sin \omega t \text{ where } M = \frac{V_m \cdot t_{on}}{L_b}$$

Through the control of the inductor current *i*Lb, the in-phase characteristic between line voltage and line current can be guaranteed to achieve high PF value. As a result, the fix on-time control is adopted by the conventional PFC controller to modulate the input resistance seen at the ac source nearly equal to a constant value PF value is

not only determined by the value of cosθ, which is decided by the angle between linevoltage and current, but also by the value of cosΦ, which is affected by the total harmonic distortion (THD) value

$$\mathrm{PF} = \cos\theta\cos\Phi = \frac{P}{A} \text{ and } \mathrm{THD} = \frac{D}{F} = \tan\Phi$$

P is the active power, *A* is the total apparent power, *D* is distortionpower, and *F* is the fundamental power. In conventionalactive PFC controller design, the target of in-phase line voltageand current simply ensures the value cosθ is equal to 1. Thatis, the reactive power can be reduced to zero by controlling the line current and ensure it is in phase with the line voltage. However,the THD value will still deteriorate the PF value owing to the existence of distortion power. The reduction in THD becomes more important if high PF is demanded in a high-quality power delivery system. Specifically, minimized THD results in a small angle of Φ and a low distortion power. Therefore, in this paper, the proposed active PFC controller not only reduces the value of θ through the in-phase line voltage and current, but also reduces the valueof THD through the perturbation on-time (POT) technique. Besides,the minimum off time is also adaptively adjusted by the proposed inhibit time (IT) control for high efficiency to reduce power consumption effectively even at low ac input voltage.

II.PROPOSED PFC CONTROLLER

The two controls are used in the Power factor controller circuit i) POT technique to modulate the on time behavior and ii) IT control to setup the minimum off time value

2.1.POT Technique

The conventional BCM architecture is as shown in Fig. 2.The expressions of on time *t*on and off time *t*off are shown as follows:

$$t_{on} = \frac{V_{EAO}}{V_{saw}} T_S \text{and} t_{off} = \frac{V_C}{V_{out}-V_c} t_{on}$$

where $T_S = t_{on} + t_{off}$.

The dc output voltage shows that on time is nearly constant for high Power factor. It is known that THD will deteriorate the Power factor. And THD is defined as the ratio of sum of the powers of all harmonic components to the power of the fundamental frequency, where I_1 is the fundamental signal of i_{ac} and $I_2 - I_n$ indicate the harmonic signal of i_{ac}.

$$\text{THD} = \frac{\sqrt{I_2^2 + I_3^2 \ldots + I_n^2}}{I_1}.$$

THD gradually increases output loading decreases as shown in the above figure, because fundamental energy is decreased and thus power factor is seriously affected. Therefore the Power factor can be expressed as

$$PF = \frac{P_{in}}{P_{line}} = \frac{\left(\frac{1}{2\pi}\right)\int_0^{2\pi} i_{ac}(\theta)v_{ac}(\theta)d\theta}{I_{rms}\,V_{rms}}$$

P_{in} is the input power and P_{line} is the line power.$I_{rms}$and V_{rms} are the rms value of the line current and voltage, respectively. The Voltage drop across the diodes and the resonant effect in the bridge leads to the crossover distortion thus THD is deteriorated. Therefore the crossover distortion angle ϕ is caused due to harmonic distortion and the line current is expressed as given below by taking I_m is the peak value of line current.

$$i_{ac}(\theta) = \frac{I_m}{1-\sin\phi}\ (\sin\theta - sin2\phi) \text{ and } v_{ac}(\theta) = V_m \sin\theta$$

Therefore the $P_{in}(\theta)$ can be derived with the effect of THD expressed as

$$P_{in}(\theta) = \frac{V_m I_m}{\pi(1-\sin\phi)}\ \left(\frac{\pi}{2} - \phi - \frac{1}{2}\ sin2\phi\right).$$

If the cross over distortion angle is smaller than ϕ, line current is zero. Therefore the distortion angle is expressed as from ϕ to $\pi - \phi$ with P_{in} is given by

$$I_{rms} = \sqrt{\left(\frac{1}{2\pi}\right)\int_0^{2\pi} i_{ac}^2\ (\theta)d\theta} = \sqrt{\frac{I_m^2}{\pi(1-\sin\phi)^2}\left[\frac{\pi}{2} - \phi - \frac{3}{2}\ sin2\phi\ + (\pi - 2\phi)\sin^2\phi\right.}$$

Therefore, the PF and THD can be obtained as follows

$$\text{PF}(\phi) = \frac{P_i}{V_{rms} \cdot I_{rms}} = \frac{\pi - 2\phi - sin2\phi}{\sqrt{\pi[(\pi-2\phi)(2-2\cos 2\phi) - (3sin2\phi).}}$$

$$\text{THD}(\phi)\ \% = 100\sqrt{\frac{\pi[(\pi-2\phi)(2-2\cos 2\phi) - (3sin2\phi)}{(\pi - 2\phi - sin2\phi)^2} - 1}$$

Therefore THD is decreased by increasing the value of ϕ thus PF is improved. By reducing ϕ value greatly, it is simplified as

$$\text{PF}(\phi) = \frac{\pi - 2\phi}{\sqrt{\pi(\pi-2\phi).}}$$

$$\text{THD}(\phi)\ \% = 100\sqrt{\frac{\pi}{\pi-2\phi} - 1.}$$

Fig. 3 shows the proposed PFC architecture with POT and IT controls for reduced THD and high PF at the same time. The POT technique modifies the conventional fix on-time mechanism through the addition of input current information to conditions. In other words, the POT technique shapes the on time by the input current and the

output voltage loop, rather than simply by the output voltage loop.the functionality of the proposed POT techniqueto verify the distortion angle Φ is effectively decreased.

Input current information through the current sensing signal *V*CS is injected into the control loop. *V*CS can also compare with the predefined value *V*limit to decide whether the overcurrent (OC) situation happens or not. On-time value is drastically increased in case of low input line current to reduce the distortion angle by further discharging *C*in. Simultaneously, efficiency can be raised due to the decreasing switching frequency because switching loss on the charging/discharging of the gate capacitanceis greatly reduced. Therefore, the perturbation of on-time value is based on the input ac voltage, which can decrease THD and thus increase PF.

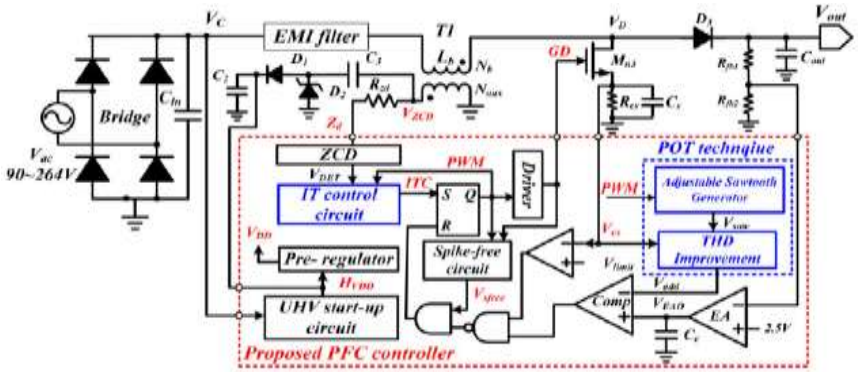

Fig 3: Proposed POT and IT controls in PFC Controller

2.2 IT CONTROL

To further increase the efficiency and reduce the EMI problem, the proposed IT control can set up the minimum off-time value as shown in Fig. 10. The converter contains at least one minimum off time to deliver the energy to the output. Before exceeding the minimum off time, the converter will not trigger the next switching again. In other words, the switching frequency will not be increased infinitely to cause a serious EMI problem.

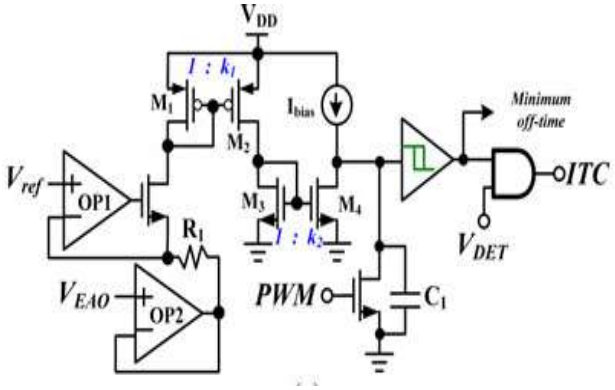

Fig 4: Schematic of POT Circuit

At low input line voltage, the minimum off time is extended. As a result, the resultant reduction in switching frequency can enhance the efficiency.

III. DESIGN CONSIDERATION

The POT technique circuit contains three blocks, namely, the adjustable saw-tooth generator, the THD improvement, and the max-on-time limiter. Accuracy of the adjustable saw-tooth generator can be improved by the timing adjustment circuit to ensure adequate power delivery. The timing adjustment circuit can adjust the minimum operation frequency higher than 35 kHz. The max-on-time limiter is also used to limit the maximum on-time value for avoiding overloading through the comparison of a higher voltage level.

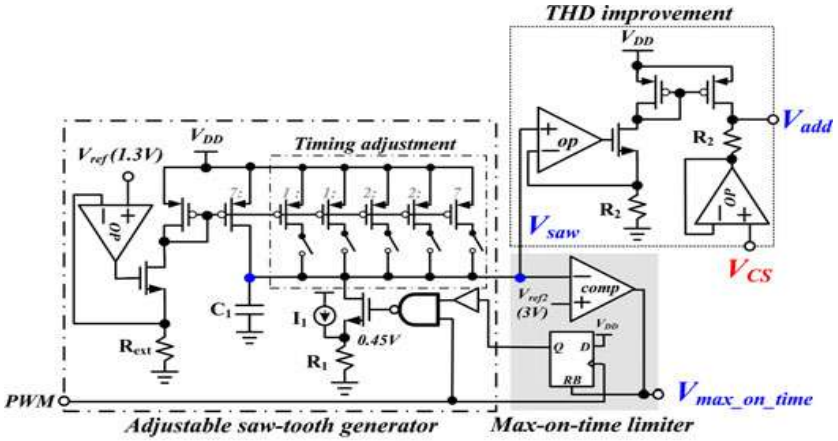

Fig 5: Schematic of IT Control circuit

On-time value can be determined by the comparison of *V*EAO and *V*add. The adjustment of on-time value can optimize the crossover distortion angle Φ. The POT techniquecan demonstrate the improvement contributed by the POT technique, that is, the decrease in Φ can be expressed as ΦPOT, which is effectively controlled by the POT technique.

The IT control circuit in Fig. 5 can improve the EMI performance by reducing high switching loss at light loads andaround low voltage level of the input line voltage. The IT control circuit adjusts the minimum off-time value according the loading indication signal *V*EAO, which is generated by the EA .

The voltage across the resistor *R*1 definesthe current flowing through the transistor *M*4 . Specifically, lowering the value of *V*EAO leads to a higher value of the current flowing through the *M*4 . Consequently, the charging current for the capacitor *C*1 is drastically decreased to generate a longer minimum off time.

IV. SIMULATION RESULTS

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The proposed system is implemented in the MATLAB environment and the obtained results are as depicted. The simulation is obtained for the output voltage of 90V, for the output power of 10 the efficiency is 93%. As the power level increases to 90, the obtained efficiency level is 95%.

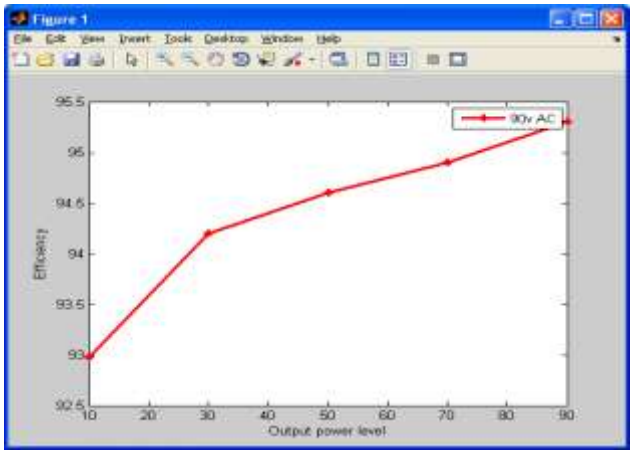

Fig 6: Output power level Vs Efficiency for the proposed system

Figure 7 shows the increased efficiency of 96% when the voltage is raised to 220V when compared to the previous voltage level of 90V. The increased efficiency results in the conservation of energy and the cost.

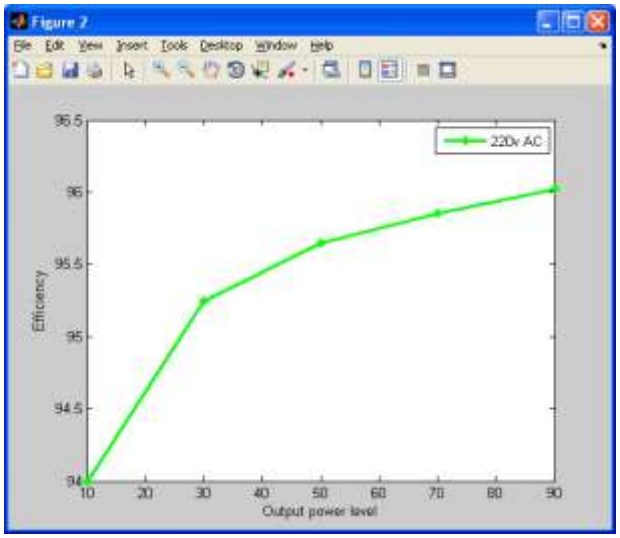

Fig 7: Output power level Vs Efficiency for the proposed system for the supply of 220V

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Figure 8 shows the graph between the Power factor and K value for the voltage level of 220V supply. The value of k range in between 0.1 and 0.6. The power factor varies in between 0.982 and 0.989. The increase in power factor reduces the line currents. The reduced line currents results in the reduction of losses.

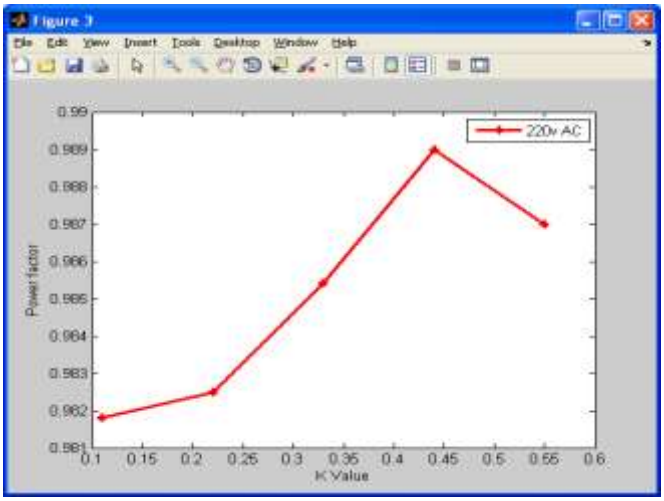

Fig 8: Power factor Vs K Value

Figure 9 depicts the plot between the % Threshold and K Value. As the k value increases the threshold value reaches the minimum value of 7. The voltage level is kept at constant value of 220V

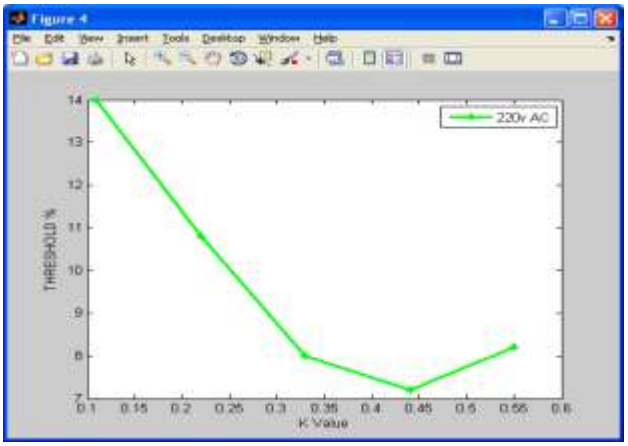

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Fig 9: Threshold percent Vs K Value

Figure 10 shows the plot between the % threshold and line voltage. As line voltage increases the % Threshold reaches the maximum value of 13. The line voltage is varied in between 80 V and 280V.

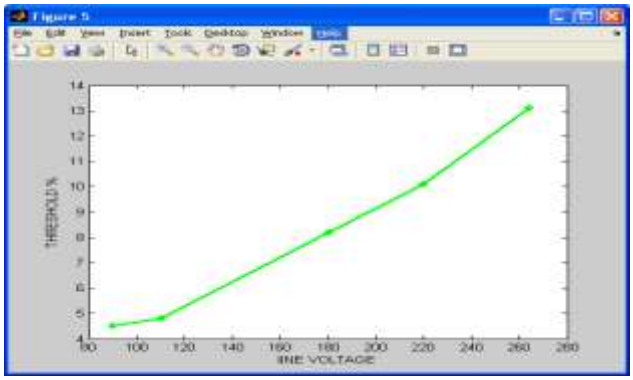

Fig 10. Threshold percent Vs K Value

V. CONCLUSION

It is observed from the obtained results the input line current is basically shaped by the power factor correction (PFC) controller to be the replica of the input line voltage and exactly in phase with it. If the value of the power factor (PF) is not 100%, it results in power losses, harmonics that travel down the neutral line, and disruption of other devices connected to the line. A high efficiency of 95% can be ensured at the output power of 90W through the proposed POT and IT controls. The PFC controller can have low THD of 5% and high PF of 0.998 at 90 Vac, and high PF of 0.985 at 220 Vac because the on-time value is perturbed by the input voltage information for reducing the distortion angle. The adaptive minimum off-time adjustment by the IT controller can also reduce the switching power loss to guarantee high efficiency. In addition, due to the UHV device, the startup mechanism can minimize the current leakage at the ac input and remove the need of external startup components.

REFERENCES

[1.] R. W. Erickson and D. Maksimovic, *Fundamentals of PowerElectronics*,2nd ed. Norwell, MA: Kluwer Academic Publishers, 2001.

[2.] J. W. Kim, S. M. Choi, and K. T. Kim, "Variable on-timecontrol ofthe critical conduction mode boost power factor correction converter toimprove zero-crossing distortion," *Power Electron. Drives Syst.*, vol.2,pp. 1542–1546, Nov. 2005.

[3.] Y.-S. Roh, Y.-J.Moon, J.-C. Gong, and C. Yoo,"Active power factorcorrection (PFC) circuit with resistor-free zero-current detection," *IEEE Trans. Power Electron.*, vol. 26, no.2, pp. 630– 637, Feb. 2011.

[4.] Y. Wang, Y. Zhang, Q. Mo, M. Chen, and Z. Qian, "An improved controlstrategy based on multiplier for CRMflyback PFC to reduce line currentpeak distortion," in *Proc. IEEE Energy Convers.Congr.Expo.*, Sep. 2010,pp. 901–905.

[5.] "Design of Power Factor Correction Circuit Using FAN7527B" Fairchildapplication note AN4121.

[6.] J.-S. Lai and D. Chen, "Design consideration for power factor correctionboost converter operating at the boundary of continuous conduction modeand discontinuous conduction mode," in *IEEE Appl. Power Electron.Conf.*, Mar. 1993, pp.267–273.

[7.] K. Yao, X. Ruan, X. Mao, and Z. Ye, "Variable-duty-cycle control toachieve high input power factor for DCM boost PFC converter," *IEEETrans. Ind. Electron.*, vol. 58, no. 5, pp. 1856–1865, May 2011.

[8.] *Power Factor Correction Handbook*, ON Semiconductor,Phoenix, AZSep. 2007.

[9.] P. Preller, "A controller family for switch mode power supplies supportinglow power standby and power factor correction," Infineon Technol. AG,Munich, Germany, Appl.Note AN-TDA 1684X, Jun. 2000.

[10.] J. Sebastian, J. A. Cobos, J. M. Lopera, and J.Uceda, "The determinationof the boundaries between continuous and discontinuous modes in PWMdc-to-dc converters used as power factor preregulators," *IEEE Trans.Power Electron.*, vol. 10, no. 5, pp. 574–582, Sep. 1995.

[11.] D. S. L. Simonetti, J. L. F. Vieira, and G. C. D.Sousa,"Modeling ofthe high-power factor discontinuous boost rectifier," *IEEE Trans. Ind.Electron.*, vol. 46, no. 4, pp. 788–795, Aug. 1999.

[12.] A. Abramovitz, "Effect of the ripple current on power factor of CRMboost APFC," in *Proc. CES/IEEE Int. Power Electron. Motion Control Conf.*, Aug. 2006, pp. 1412–1415.

[13.] M. M. Jovanovi´candY. Jang, "State-of-the-art, single-phase, active powerfactor-correction techniques for high-power applications—An overview,"*IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 701–708, Jun. 2005.

[14.] J. Zhang, J. Shao, F. C. Lee, and M. M. Jovanovi´c, "Evaluation of inputcurrent in the critical mode boost PFC converter for distributed powersystems," in *Proc. IEEE ApplPower Electron. Conf.*, Feb., 2001, pp. 130–136.

[15.] K. De Gusseme, D. M. Van de Sype, A. P. M.Van Den Bossche, and J.A. Melkebeek, "Input- current distortion of CCM boost PFC converters operated in DCM," *IEEE TransInd. Electron.*, vol. 54, no. 2, pp. 858–865, Apr. 2007.

[16.] K. H. Liu and Y. L. Lin, "Current waveform distortion in power factor correction circuits employing discontinuous-mode boost converters," in*Proc. IEEE Power Electron. Spec. Conf.*, Jun. 1989, pp. 825–829.

[17.] C. Y. Bernd, R. Liang, "Power factor correction with reduced total harmonicdistortion," United States Patent 6 128 205, Oct. 3, 2000.

[18.] D. Dai, S. N. Li, X. K. Ma, and C. K. Tse. "Slow-Scale Instability of Single-Stage Power-Factor-Correction Power Supplies."*IEEE Trans. On Circuits and Systems I: Regular Papers*, vol.54, pp.1724-1735, Aug2007.

[19.] B. R. Lin, C. L. Huang, and M. Y. Li. "Novel zero voltage switching dual-switch forward converter with ripple current cancellation." *Electric Power Applications, IET*, vol.1, pp.799-807, Sep 2007.

[20.] R. T. Chen and Y. Y. Chen, "Single-stage push–pull boost converter with integrated magnetics and input current shaping technique," *IEEE Trans.Power Electron.*, vol. 21, no. 5, pp. 1193–1203, Sep. 2006.

[21.] A. Fernandez, J. Sebastian, F. F. Linera, and A.Ferreres, "Single-stage AC-to-DC converter with self-driven synchronous rectification that complies with EN61000-3-2 regulations," *IEEE Trans. Ind. Electron.*, vol. 50,no. 5, pp. 1062–1064, Oct. 2003.

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