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Efficient signal processing in clock domain crossing

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ABSTRACT

Ever shrinking device sizes and the innovative circuit design techniques have made it possible to have a multimillion-transistor systems running with multiple asynchronous clocks. Digital Design is becoming increasingly sophisticated day by day. As a result, circuits with multiple clocks must have reliable communication with each other for optimizing power and to increase the speed and accuracy. When a signal in a multiple clocked digital circuit traverse from one clock domain into another, this is known as clock domain crossing. Due to either differing clock latency or a different clock source, different clock domains have clocks which have a different frequency, a different phase or both. Either way the relationship between the clock edges in the two domains cannot be relied upon. Therefore, clock domain crossing signals pose issues and challenges during verification. Although the existing simulation techniques are adequate to verify clock domain crossings but they are time consuming and provide partial verification only. The asynchronous clocks used in circuits may lead to setup or hold time violations of flip flops. These violations can lead the signal to a metastable state, because of these the receiver will recognize the logic level to be at the different value and hence generate erroneous signals. This paper addresses metastability in clock domain crossing and proposes a methodology to remove this metastable state.

***Keywords*: Clock domain crossing, metastable, setup and hold time violations**

I. INTRODUCTION

In todays era, only elementary digital circuits use a single clock. Most data-movement applications, including disk-drive controllers, mobile phone chips, modems, network interfaces and network processors have a multitude of components working with different clock-domains running at varying speeds[1-3]. These applications bear inherent challenges related to signal stability while moving data across multiple clock domains. When signals travel from one clock domain to another, the signal appears to be asynchronous in the new clock domain[4-6].

System-on-a-chip advanced architectures support asynchronous clock domains in the circuit.The part of the design driven by single clocks or clocks with the constant phase relationships is called as clock domain. The system is often composed of various such domain where in each system runs on its own clock.The link through which these domains communicate is known as clock domain crossing. Signals that cross the clock domain boundary are of two types (i) Synchronous and (ii) Asynchronous. Synchronous crossings are defined as those in which the sending and the receiving domain have a phase relationship and frequency relationship which can either be same or different. Static timing analysis can guarantee that data does not change within clock setup and hold times within synchronous clock domain. On the other hand asynchronous crossings are those which do not have any phase or frequency relationship between the sending and receiving domains[7-11]. When signals in circuits with asynchronous clock domain are passed, the time analysis cannot guarantee about the data change ,thereby leading to metastability state.

In any design every flipflop has a specified setup and hold time violations, or the time period in which the data is not allowed to change before and after the clock edge. If the setup and hold time variations are met then the correct output will appear at the valid output level (and) with the maximum clock to output delay of the flip flop. However, if these setup and hold time variations are not met then the output of the flip flop will take much longer delay as compared to clock to output delay to reach at a valid logic level. This unstable behavior of output is known as metastability. This unstable value may or may not converge to a stable value either 0 or 1 before the sampling clock edge for some duration of time at some point during normal operation of a design. The duration of the metastable condition cannot be determined as it is a nondeterministic phenomenon, and therefore we cannot determine the maximum possible time[12-18].

When a data signal is being sampled with a clock, the outcome is determined by the order of the events. The smaller the time difference between two events, the longer time it will take to analyze which event occur first. When two events occur very close together, then either the decision process will take longer than the time allotted or the synchronization failure occurs. In a multi-clock design, metastability cannot be avoided but the detrimental effects of metastability can be neutralized. To address clock domain problems due to metastability several types of synchronization techniques are employed worldwide.

Remainder of the paper proceed as follows. Section 2 introduces synchronization techniques and its working principle has been explained. In section 3, a proposed synchronization technique is given and results are given in section 4. Section 5 concludes the paper.

II. SYNCHRONIZATION TECHNIQUES

In Fig.1, multiple clocks come from different sources. The sections of logic elements driven by these clocks are called clock domains, and the signals that interface between these asynchronous clock domains are called the clock domain crossing paths. The output signal D_A of flip flop A is considered an asynchronous signal into the clock domain as there is no constant phase and time relationship between Clk_A and Clk_B.

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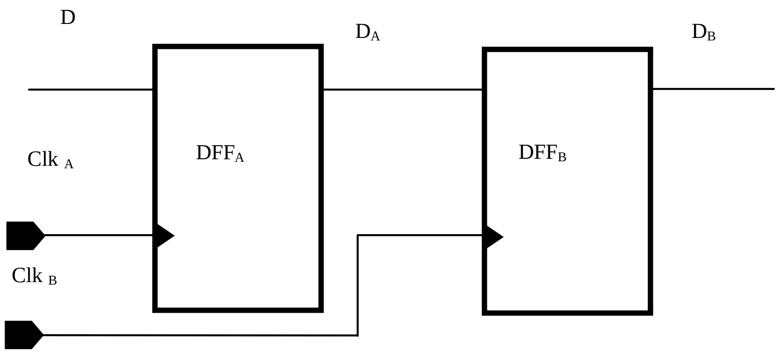

Fig.1: Synchronizer circuit

Synchronizer is a circuit-level term that refers to a device that converts an asynchronous signal and outputs a version of the signal that has transitions synchronized to a local or sample clock. It is used to resolve the clock domain issues due to metastability and data sampling. However, the sole introduction of the synchronizers does not guarantee prevention of the metastability. The proble of metastability should be resolved within a synchronization period (a period of the destination clock) so that the sampling of the output of the flip-flop in the destination clock domain becomes a simpler task. The main job of the synchronizer is to provide sufficient time to the metastable state to settle down to a stable state in the destination clock domain, thereby making it an essential component in most clock domain crossing interfaces. There are two scenarios possible when signals are passed across the cross domain crossing boundaries, and hence it is important to determine which scenario is true for proposed design.

1. Between clock domain every passed signal should be sampled.
2. It is allowed to miss samples between clock domains

The time elapsed between the two consecutive failures of a synchronizer is called as the mean time between failure (MTBF). By using MTBF, the occurrence of metastability can be predicted easily using following relationship.

$$\mathrm{MTBF} = \frac{e^{C_2 \cdot t_m}}{C_1 \cdot f_{clk} \cdot f} \qquad (1)$$

Where C_1 and C_2 are the constants used during the flip flop generation and t_{met} is the duration of the metastable output. The term f_{data} represents the frequency of asynchronous input, and f_{clk} is the frequency of synchronous clock. The exponential term in the equation is used to describe the time duration for which, a given metastable condition will last i.e t_{met}. As the time delay is increased, the number of failures decreases dramatically. When calculating MTBF for the circuits, it is preferable to use larger ones over the smaller ones. It indicates large time gap between two potential failures, while the small MTBF signifies that the metastable state generates frequently causing failures in the circuit.

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III. PROPOSED CIRCUIT

The circuit implementation of proposed synchronizer is shown in Fig.2 shows the working principle of simplest and the most common type of synchronizer.

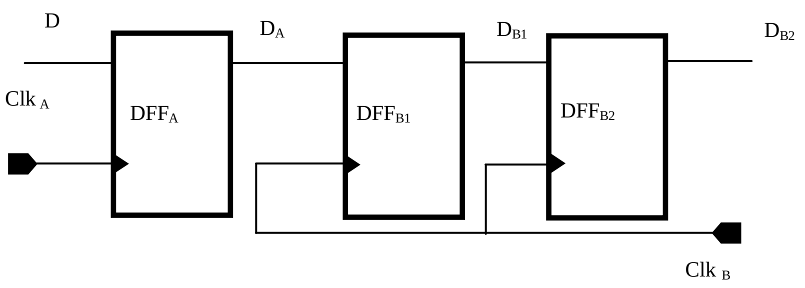

Fig.2: Proposed synchronizer circuit

It consists of three flip flops A, B1 and B2. The flip flop B1 and the flip flop B2 are used as synchronizers in the proposed circuit. The flip flop A samples the input signal D_A into the new clock domain and waits for any metastable state on the signal D_{B1}, then again the signal D_{B1} is sampled by the clock B again. DB2 is now a valid and stable signal synchronized and ready for further use in the circuit. For most of the circuits using asynchronous clocks, the two flip flop synchronizer is sufficient to remove all the metastable state. By using few guidelines and verification and synchronization techniques these errors can be avoided. For higher speed designs, the MTBF of two flip flop synchronizer is too small and therefore a third flip flop is added in the proposed synchronizer to increase the MTBF.

IV.SIMULATION RESULTS

The proposed circuit has been simulated using SPICE. Fig.3 shows the output signals and metastability occurring when the two clocks are changing very close to each other. The metastable state is more clearly visible in Fig.4. This metastable state cause failures. Fig.5 shows metastable state in proposed circuit. From the results it is seen that the proposed synchronizer removes the metastable state.

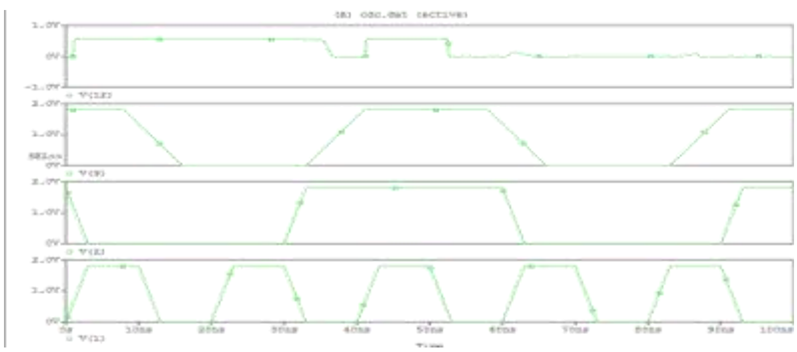

Fig.3: Waveforms of synchronizer circuit

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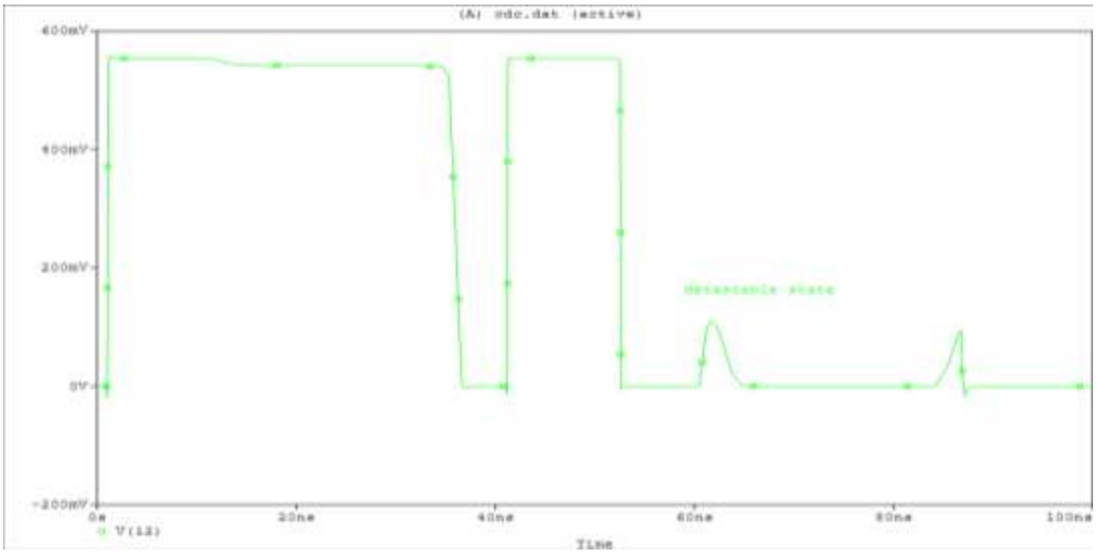

Fig.4: Metastable state synchronizer circuit

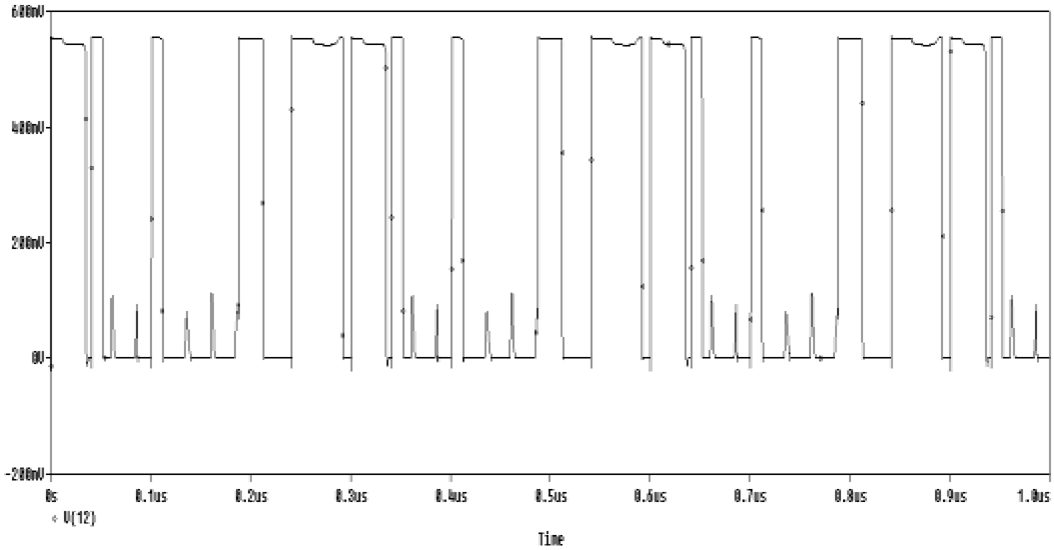

Fig.5: Metastable state proposed synchronizer circuit

V.CONCLUSION

The error generated by clock domain clocking signal can cause serious design failures. The issues such as metastability cannot be detected using the simulation and static-timing analysis, as a result, these issues often end up as pressure on the silicon chip. These failures can be very expensive as again whole the process has to be repeated to remove the errors. By using few guidelines and verification and synchronization techniques these errors can be avoided. In this work, a new synchronizer has been proposed as for higher speed designs, the

MTBF of two flip flop synchronizer is too small. The addition of third flip flop is in the proposed synchronizer increases the MTBF.

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