International Journal of Advance Research in Science and Engineering
Volume No.06, Issue No. 11, November 2017
www.ijarse.com
IJARSE
ISSN: 2319-8354

ADIABATIC LOGIC FOR ULTRA LOW POWER APPLICATION

Kirti Gupta

Dept. of Electronics and Communication,

Bharati Vidyapeeth's College of Engineering, Delhi, (India)

ABSTRACT

This paper attempts to merge the advantages offered by the adiabatic logic family and subthreshold operation to design ultra low power digital circuits. Adiabatic circuits when operated within the sub-threshold region can reduce both dynamic as well as static power thus greatly reducing the overall power dissipation. Two different adiabatic logic families have been discussed and successfully operated within the sub-threshold region. Their functionality has been verified by means of their inverters, and have been compared based on their power dissipation and propagation delays at different input frequencies. All simulations have been carried out using TANNER EDA software using 180nm technology.

Keywords: Adiabatic logic, low power, subthreshold region, Digital circuits, ECRL, IECRL

I. INTRODUCTION

Ever-growing demand for portability and increased performance has resulted in increased levels of dissipated power in digital circuits. This poses a threat to the rate of advancement of the electronics industry. Use of adiabatic technology is one key solution to curb the growing power needs. Adiabatic circuits significantly reduce the dynamic power dissipation of a circuit, thus reducing the overall power [1-2].

Operating digital circuits in the sub-threshold region is another way to reduce dissipated power to sufficiently low levels. Circuits operating in the sub-threshold region use leakage currents for realizing the logic. Thus dissipated power dominantly comprises of the leakage power [3-7]. Both these techniques have great potential yet to be exploited.This paper attempts to combine the advantages offered by the adiabatic logic family and subthreshold operation to design ultra low power digital circuits. Adiabatic circuits when operated within the sub-threshold region can reduce both dynamic as well as static power thus greatly reducing the overall power dissipation. Two different adiabatic logic families have been discussed and successfully operated within the sub-threshold region.

The paper first presents an overview of the CMOS operating in subthreshold region in section 2. Then, the adiabatic logic style in subthreshold is discussed in section 3. The subsequent section 4 presents the simulation results. In the last, the conclusion are drawn in Section 5.

II. SUBTHRESHOLD REGIME

The conventional CMOS devices which maintains long channel and operate on high supply voltages remained more or less unaffected by the leakage currents. This is due to the extremely low values of leakage currents as compared to the operational currents. However, with the scaling of the CMOS devices an increase in the leakage currents is observed which could no longer be ignored as compared to the operational current.Leakage currents are present even when the MOS is in the OFF state hence it is a necessary evil.

Over the past decades V_{DD} has decreased from typical 5 V down to typical 1V in present state-of-the-art processes. As the dynamic power consumption quadratically depends on the supply voltage. A result of this has been a dramatic reduction in the dynamic power consumption. While the dynamic power consumption has decreased, the static leakage currents have simultaneous increased, due to thinner gate-channel isolation layer and lowered threshold voltage [8-13].

Operation in Sub-threshold region is achieved by applying a low voltage at the gate terminal. As a result, the majority carriers between the drain and the source region are repelled away from the surface, leaving a depletion charge of fixed atoms. The density of minority carriers is increased with respect to the distant bulk, but it is still negligible in the overall charge balance. However, these minority carriers are the only mobile charge available at the surface. Hence, as soon as some voltage is applied between the source and the drain of a MOS transistor structure, they move by diffusion, thereby producing a drain current also called the sub-threshold current.

Sub-threshold region can be of weak inversion or moderate inversion depending upon the applied gate voltage. If the voltage applied at the gate terminal is sufficiently below the threshold voltage Vt then the MOS device is said to be in the weak inversion region characterized by the flow of diffusion current only. However, when the gate voltage is around the threshold voltage Vt then the device is in moderate inversion region. The drain current in moderate inversion region is a combination of drift and diffusion currents.

By operating the circuit's transistors in their sub-threshold region, transistors are never fully turned on. Instead they are varying between being turned off and partially turned on, starting to conduct sub-threshold leakage current to a greater degree. While the dynamic power consumption increases quadratically with the supply voltage, the maximum clock frequency increases only linearly with the supply voltage [17]. The static power consumption contribution exceeds the dynamic when operating at very low supply voltage [16]. When transistors are operated in the sub-threshold region, power consumption is dramatically reduced without the need for major design changes of the circuit.

III. ADIABATIC LOGIC FAMILIES

In conventional CMOS logic significant power loss occurs specially during the switching operation. The various power losses can be reduced by using several techniques. But however, these techniques are

accompanied by its advantages and disadvantages. Also in all these techniques the energy drawn from the power supply is used only once before being dissipated. To increase the energy efficiency of the logic circuits, other measures can be introduced for recycling the energy drawn from the power supply. A novel class of logic circuits called adiabatic logic offers the possibility of further reducing the energy dissipated during the switching events, and the possibility of recycling, or reusing, some of the energy drawn from the power supply. To accomplish this goal, the circuit topology and the operation principles have to be modified, sometimes drastically.

Adiabatic Logic is a logic family which means to operate without or absolutely no losses, also a yet another term maned as "Quasi-Adiabatic Logic" is describes a logic style whichworks with lower power than static CMOS logic, but which still has some minimum non-adiabatic losses. Overall, both the logic types represents that these systems consume substantially less power than the traditional static CMOS circuits. This logic style is also known as: "Charge recovery logic", "Charge recycling logic", "Clock-powered logic", "Energy recovery logic" and "Energy recycling logic" in the existing literature.Adiabatic circuits follow some common principles which are as follows:A transistor should never be turned on a transistor if there is a voltage potential between the source and drain and transistor should not be turned off when current is flowing through it.Changes in the voltage must be done gradually, and current should not be passed through a diode [1, 2].

In this paper, the concepts of both the adiabatic logic and circuits operating in the sub-threshold region are merged for the conservation of dissipated power. Adiabatic logic circuits operating in the sub-threshold region of operation is characterized by a supply voltage lower than the threshold voltage for the circuit. When circuits operate in the sub-threshold region or weak inversion region the depletion layer so formed lacks minority carriers for effective conduction. Thus this region is characterized by diffusion current rather than drift current. The drain current is formed mainly by leakage currents which become significant in this region. Thus in this region leakage power forms a major portion of the total power. As leakage currents are used for charging of the output nodes the overall power is significantly reduced.Both these techniques can be combined in a way so that the dissipated power can be further reduced. The performance of the ECRL: Efficient Charge Recovery Logic and IECRL: Improved Efficient Charge Recovery Logichave been studied in subthreshold region in the paper.

3.1 ECRL: EFFICIENT CHARGE RECOVERY LOGIC

ECRL family consist of a pair of cross-coupled PMOS transistors[14]. The NMOS network forms the functional unit and cross coupled PMOS acts as a load. ECRL uses dual rail inputs and provides dual rail outputs as shown in Fig. 1. This family uses four phase trapezoidal power clock for its working.ECRL uses a method in which pre-charge and evaluation occur simultaneously which eliminates the need of pre-charging diode and hence reduces energy dissipation. One disadvantage of ECRL is that once the charge from the previous stage has been recovered from the gate of the NMOS devices, there is no pull-down path to ground. This has implications for noise susceptibility. Also it has the coupling effects, because the two outputs are

connected by the PMOS latch and the two complementary outputs can interfere with each other. The circuit diagram for a ECRL inverter is shown in Fig. 2.

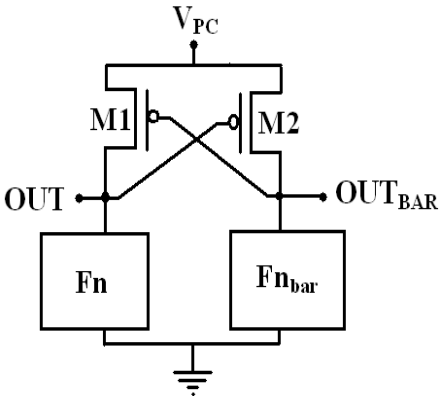


Fig. 1 Generalized ECRL structure

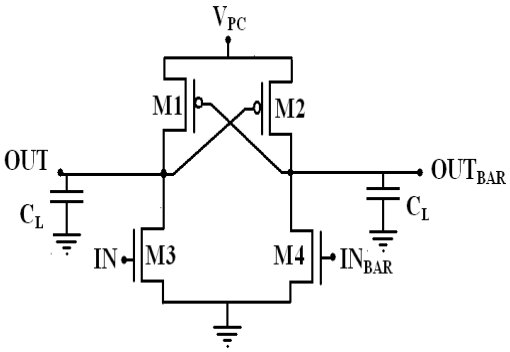


Fig. 2. ECRL Inverter

When the clock is in evaluation phase and M3 is given high input, and correspondingly INBAR is low, the output node connected to M3 will be provided a path to ground and hence output will be low. The drain of M3 is connected to drain of M1 which comes in operation as its gate is given low input. M1 makes the OUTBAR node follow the power clock. In the hold phase, the circuit holds its state and stabilizes all the outputs. In the recharging phase, the circuit regains the energy it supplied in the evaluation phase. The capacitance connected to OUTBAR node which is charged during the evaluation phase, discharges itself and the charge flows back to the power supply. During the wait stage, the input switches its value and the circuit waits to evaluate new input values. Similarly when IN is low and INBAR is high then OUTBAR gets connected to ground via M2. In this case PMOS connected to output node gets active and output node follows the power clock.

3.2 IECRL: IMROVED EFFICIENT CHARGE RECOVERY LOGIC

This family uses cross coupled network of CMOS inverters to realize any function [15]. This family also uses dual rail coded signals, i.e., both true and complement values of inputs and outputs are present as shown in Fig. 3. In comparison to ECRL this family uses NMOS transistor in parallel with the function to be implemented so as to provide better connection to ground when inputs have had their charge recovered. It is also called 2N-2N2P adiabatic family. The two cross-coupled NMOS which provide a better path to ground even after the inputs has recovered their charge. They are used in standard SRAM cell. The circuit diagram for a IECRL inverter is shown in Fig. 4.

International Journal of Advance Research in Science and Engineering
Volume No.06, Issue No. 11, November 2017
www.ijarse.com
IJARSE
ISSN: 2319-8354

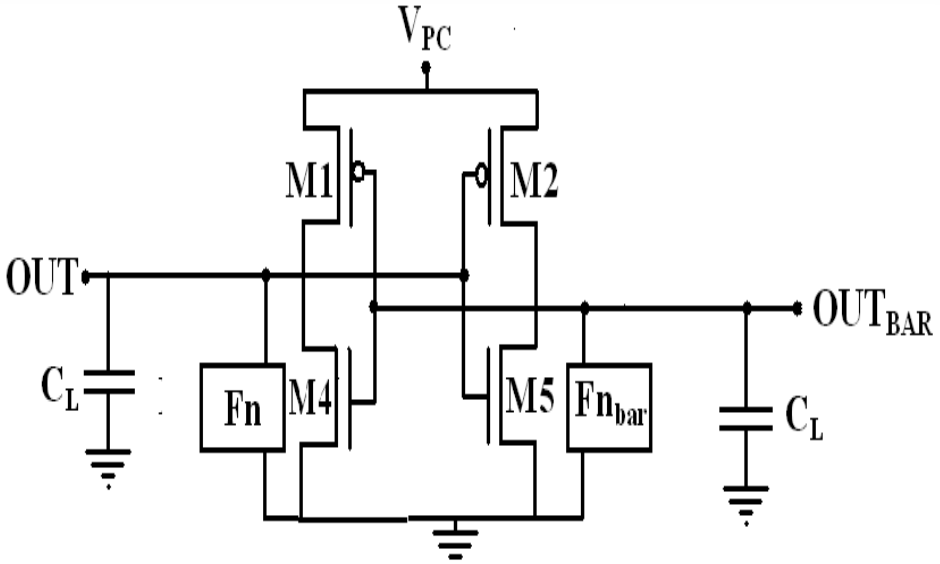


Fig. 3 IECRL generalized structure

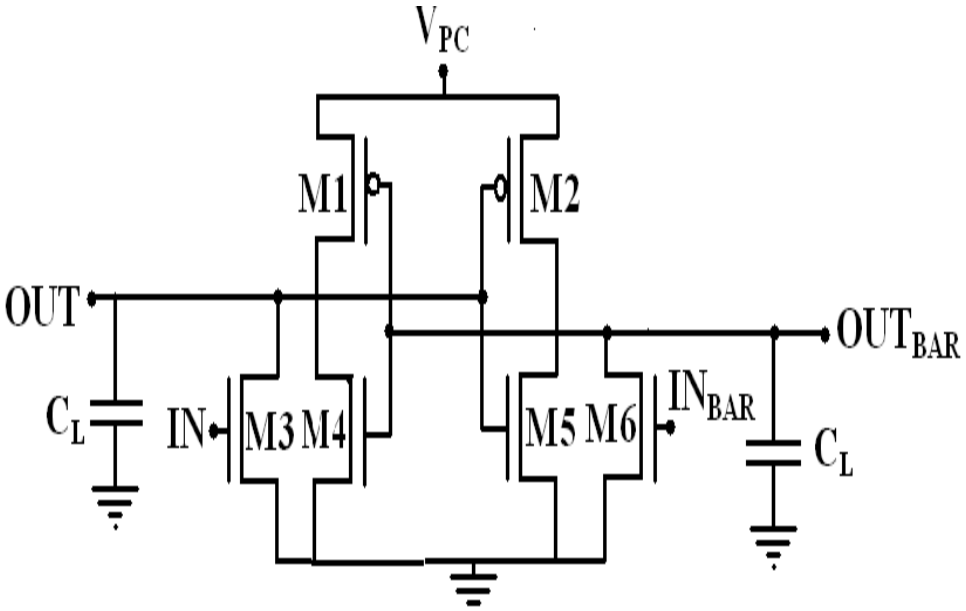
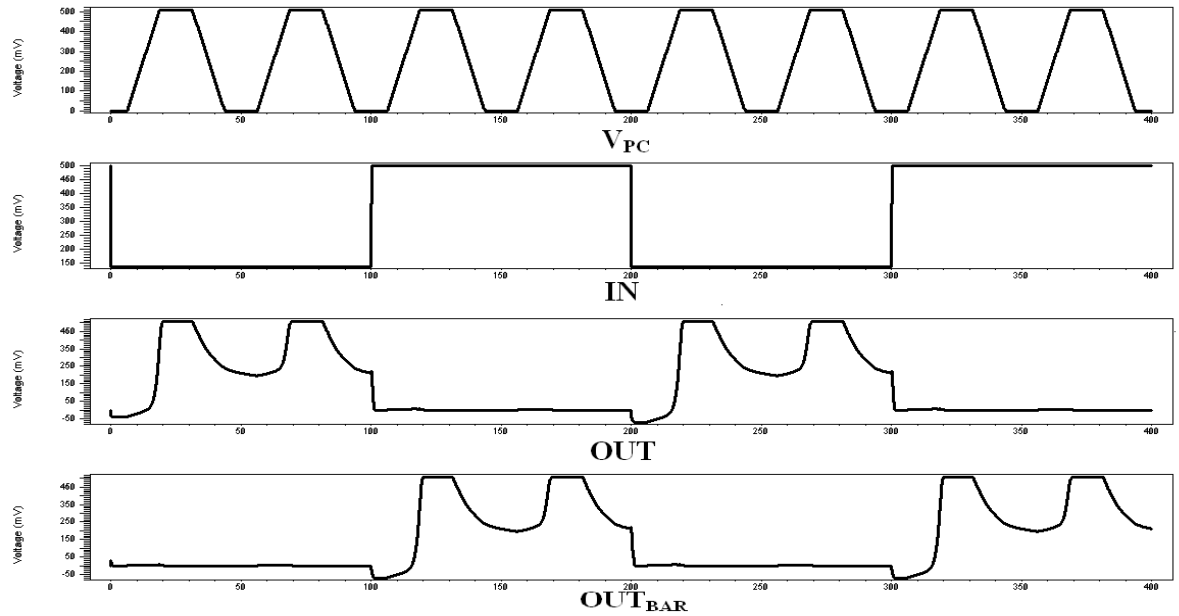


Fig. 4 IECRL Inverter

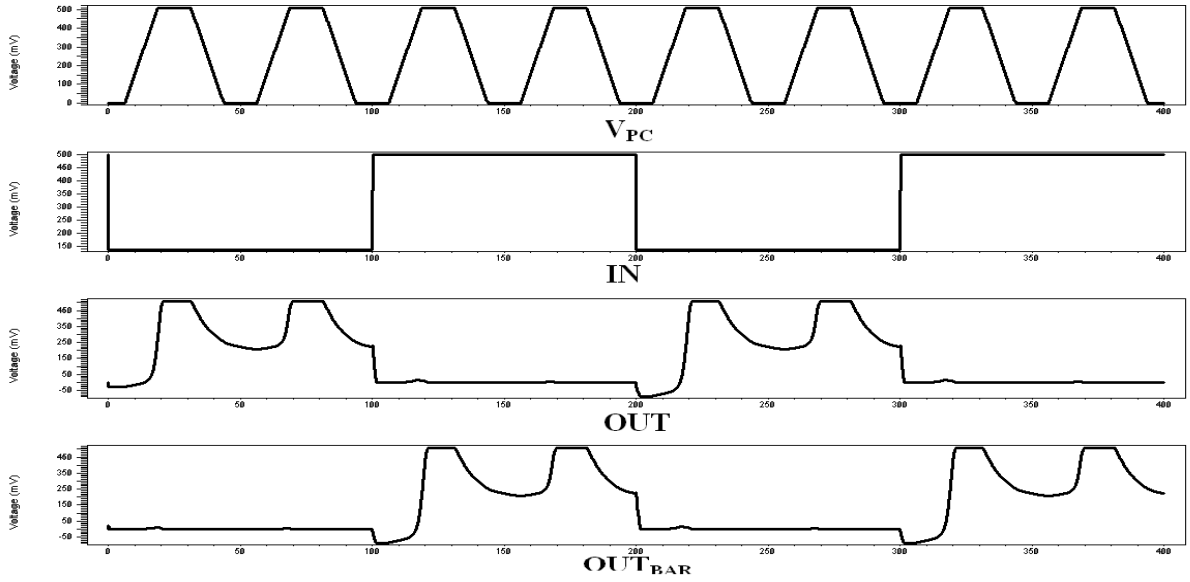
IV. SIMULATION RESULTS

In this section, the inverter circuits simulations of each of the adiabatic logic families in subthreshold region is discussed above are discussed. All simulations were carried out using Tanner EDA software using 180nm technology. The simulation waveforms for the inverters are shown in Fig. 5. The performance of the two inverters in the two logic families is compared in terms of power, delay and power delay product at different frequencies. The results are listed in Table I.

International Journal of Advance Research in Science and Engineering
Volume No.06, Issue No. 11, November 2017
www.ijarse.com
IJARSE
ISSN: 2319-8354



(a)



(b)

Fig. 5 Simulation Waveform (a) ECRL Inverter (b) IECRL inverter

International Journal of Advance Research in Science and Engineering
Volume No.06, Issue No. 11, November 2017
www.ijarse.com
IJARSE
ISSN: 2319-8354

Table.6.1 Power dissipation (µW) for different operating frequencies(MHz)

FREQUENCY / LOGIC FAMILY	5 MHZ	10 MHZ	20 MHZ	30 MHZ	40 MHZ	50 MHZ	60 MHZ
Power (µW)							
ECRL	3.73	8.49	18.86	29.94	39.17	48.31	59.26
IECRL	6.09	14.13	23.33	39.19	55.31	60.53	-
Delay (nS)							
ECRL	12.28	5.83	2.66	1.97	1.63	1.46	1.34
IECRL	12.19	5.34	3.63	4.12	3.61	2.81	-
Power Delay Product (PDP) (fJ)							
ECRL	45.81	49.49	50.17	58.98	63.85	70.53	79.41
IECRL	74.24	75.45	84.69	161.46	199.67	170.09	-

During the simulations the following advantages and disadvantages corresponding to various families were observed:

ECRL uses a method in which pre-charge and evaluation occur simultaneously which eliminates the need of pre-charging diode and hence reduces energy dissipation. One of the disadvantage of ECRL is that it has the coupling effects, because the two outputs are connected by the PMOS latch and the two complementary outputs can interfere with each other. Also the energy recovery is partial due to premature turning off of the PMOS path to the power clock. In multistage application once the charge from the previous stage has been recovered from the gate of the NMOS devices, there is no pull-down path to ground. This has implications for noise susceptibility. Also when cascaded, each subsequent stage would need a power clock with a phase lag of 90 degrees than the previous stage for proper operation.

IECRL shows improvement over ECRL by providing a path to ground, but however due to the presence of extra transistors than ECRL, it would occupy greater on-chip area. The delay and power dissipation for different operating frequencies and load capacitances is found to be almost identical to that of the ECRL family.

V. CONCLUSION

This paper presents a technique to obtain ultra low power digital circuit by combining the advantages offered by the adiabatic logic family and subthreshold operation. Adiabatic circuits operating in the sub-threshold region reduces both the dynamic as well as static power thus greatly reducing the overall power dissipation. Two different adiabatic logic families have been discussed and successfully operated within the sub-threshold region. Their functionality has been verified by means of their inverters, and have been compared based on their power dissipation and propagation delays at different input frequencies. All simulations have been carried out using TANNER EDA software using 180nm technology.

REFERENCES

[1] Y. Moon, and D.K. Jeong, "An efficient charge recovery logic circuit,"*IEEE J. Solid-State Circuits.*, vol. 31, no. 4, pp. 514–522, April 1996.

[2] J. S. Denker, "A Review of Adiabatic Computing," in *Proc. IEEE Int. Symp. Low Power Electronics*, San Diego, CA, Oct. 10–12, 1994, pp.94–97.

[3] Sanjay Kumar Singh, B.K. Kaushik, D.S. Chauhan and Sampath Kumar, "Reduction of Subthreshold Leakage Current in MOS Transistors",World Applied Sciences Journal 25 (3): 446-450, 2013 ISSN 1818-4952 © IDOSI Publications, 2013 DOI: 10.5829/idosi.wasj.2013.25.03.797

[4] Po-Hsuan Huang, Hongchin Lin,and Yen-Tai Lin, "A Simple Subthreshold CMOS Voltage Reference Circuit With Channel- Length Modulation Compensation", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 53, NO. 9, SEPTEMBER 2006

[5] W. C. Athas, L. J. Svensson, J. G. Koller, N. Tzartzains, and E. YC. Chou, "Low-power digital systems based on adiabatic-switching principles," IEEE Trans. VLSI Syst., vol. 2, no. 4, pp. 398–407, Dec. 1994.

[6] B. C. Paul, A. Raychowdhury, and K. Roy, "Device optimization for digital subthreshold logic operation," IEEE Transactions on Electron Devices, vol. 52, pp. 237–247, Feb. 2005.

[7] R. M. Swanson and J. D. Meindl, "Ion-implanted complementary MOS transistors in low-voltage circuits," IEEE Journal of Solid-State Circuits, vol. 7, pp. 146–153, Apr. 1972.

[8] A. Bryant, J. Brown, P. Cottrell, M. Ketchen, J. Ellis-Monaghan, and E. J. Nowak, "Low-power CMOS at vdd=4kt/q," in Proc. of IEEE Device Resarch Conference (DRC'01), Notre Dame, IN, USA, June 2001,pp. 22–23.

[9] G. Schrom and S. Selberherr, "Ultra-low-power CMOS technologies," in Proc. of IEEE International Semiconductor Conference (CAS'96), Oct.1996, pp. 237–246.

[10] X. Qi, S. C. Lo, A. Gyure, Y. Luo, M. Shahram, K. Singhal, and D. B. MacMillen, "Efficient subthreshold leakage current optimization," IEEE Circuits and Devices Magazine, vol. 5, pp. 39–47, 2006

[11] E. J. Nowak, "Maintaining the benefits of CMOS scaling when scaling bogs down," IBM Journal of Research and Development, vol. 46, pp. 169-180, Mar. 2002.

[12] B. H. Calhoun and A. Chandrakasan, "Characterizing and modeling minimum energy operation for subthreshold circuits," in Proc. of IEEE International Symposium on Low Power Electronics and Design Conference (ISPLED'04), Newport Beach, CA, USA, Aug. 2004, pp. 90–95.

[13] G. Schrom and S. Selberherr, "Ultra-low-power CMOS technologies," in Proc. of IEEE International Semiconductor Conference (CAS'96), Oct.1996, pp. 237–246.

[14] Y. Moon, and D.K. Jeong, "An efficient charge recovery logic circuit,"IEEE J. Solid-State Circuits., vol. 31, no. 4, pp. 514–522, April 1996.

[15] J. S. Denker, "A Review of Adiabatic Computing," in Proc. IEEE Int. Symp. Low Power Electronics, San Diego, CA, Oct. 10–12, 1994, pp.94–97