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ON-CHIP PERMUTATION NETWORK IN MULTIPROCESSOR SYSTEM ON-CHIP FOR ADDRESSING PERMANENT ERRORS

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ABSTRACT

This paper presents the design of on-chip permutation network to support traffic permutation and an adaptive system for detecting and bypassing permanent errors in on-chip interconnects. Without interrupting the data flow this system employs pipelined circuit-switching approach with dynamic path setup which reroutes the data to a set of spare wires on erroneous links .If there is any change in permutation dynamic path set up scheme supports run time path arrangement. The multistage network topology detects permanent errors at runtime. The circuit-switching offers a guarantee of permuted data and enables the benefit of stacking multiple networks. In-Line Test (ILT) using spare wires and test pattern generator is proposed.

Keywords: Permutation, Pipelined Circuit Switching, Multistage Network, In-Line Test (ILT)

I. INTRODUCTION

As the number of the elements and transactions among cores of the Multiprocessor SoC (MPSoC) and Multi core processor (MCP) increases, the reliability and performance of the system becomes a key design and implementation issue for large scale system. Fault may be either transient or permanent and packet congestion in the interconnection network is sources for reducing the reliability and performance in a NoC based system. A fault tolerant and high performance network system provides continuous operation in the presence of faults or congestions.

Permutation traffic is a traffic pattern where each input sends traffic to exactly one output and each output receives traffic from exactly one input, is one of the important traffic classes exhibited from on-chip multiprocessing applications [7], [8].

In order to maintain coding strength in the presence of permanent errors, spare wires are used to replace permanently erroneous wires.Spare wires requires the following: 1) reconfiguration control and logic to replace the erroneous wires and 2) a protocol for synchronizing information between receiver and transmitter. A system that replaces permanently erroneous wires without any interruption in data flow is designed using spare wires. To detect permanent errors, In-Line Test (ILT) method to test each adjacent pair of wires in a link for opens and shorts. These tests can be run periodically to ensure that each link's error correction. Every wire in the link is

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tested; the ILT method also recovers resources from intermittent errors that were incorrectly flagged as permanent.

II. ON-CHIP NETWORK DESIGN

The pipelined circuit-switching approach with a dynamic path-setup scheme supports runtime path arrangement. The path setup, network topology is done then switching nodes are designed.

Clos network is a family of multistage networks is applied to build scalable commercial multiprocessors with thousands of nodes in macro systems [7], [11]. A three-stage Clos network is given as C (n, m,p), where n represents the number of inputs in each of p first-stage switches and m is the number of second-stage switches.

The advantage of this network is connection between a large number of input and output ports made by using only small-sized switches. The matching between the ports can be made by configuring the switches in all stages. In figure n represents the number of sources which feed into each of the m ingress stage crossbar switches. There exists only one connection between each ingress stage switch and each middle stage switch. And each middle stage switch is connected to only once to each egress stage switch.

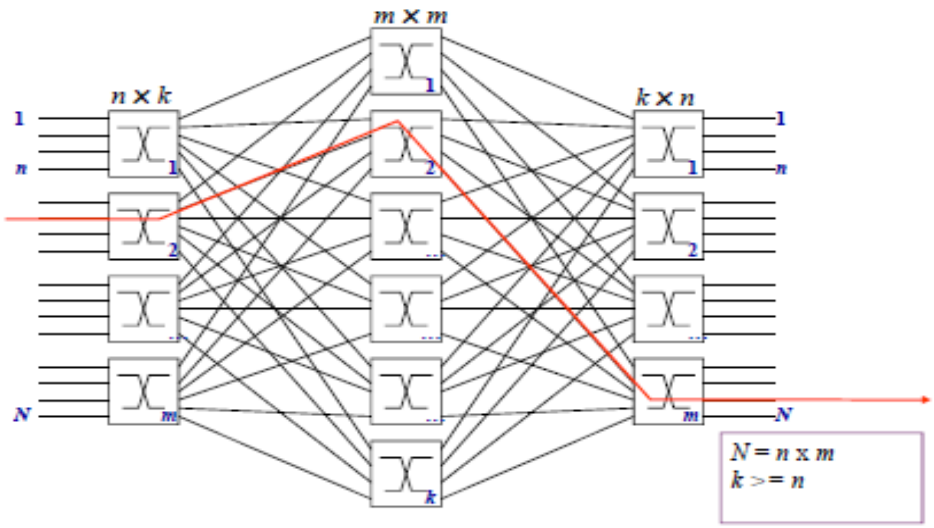

Figure 1: 3-Stages Clos Network.

To support a parallelism degree of 16 as in MPSoCs [3]–[5], C(4,4,4) is used as a topology for the designed network. This network can realize all possible permutations between its input and outputs using rearrange able property.

The three-stage Clos network is used to minimize implementation cost and it enables a rearrange able property for the network. There are three phases in a pipelined circuit-switching scheme: the setup, the transfer, and the release [2], [9].

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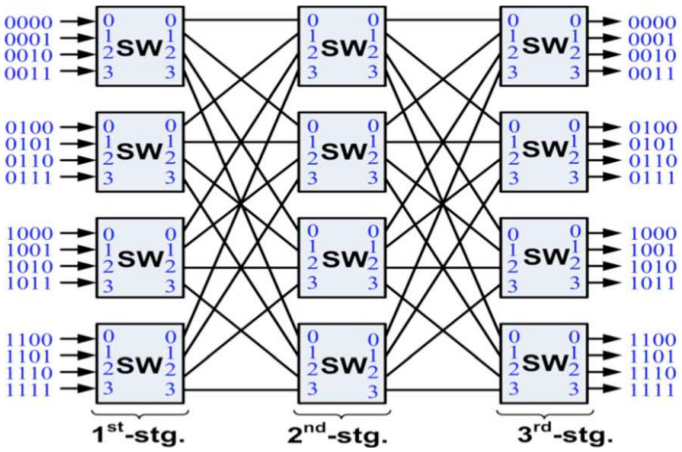

Figure 2: On-chip network topology

2.1. SWITCH INTERCONNECTION

A switch-by-switch interconnection with handshake signals is proposed to support circuit switching. The bit format of the handshake is 1-bit Request (Req) and a 2-bit Answer (Ans). When an idle link is requested by the corresponding downstream switch in the setup phase Req=1 is used. It is also kept during data transfer along the set up path. A Req=0 the switch releases the occupied link. This code is also used in both the setup and the release phases. The destination is ready to receive data from the source when Ans=01. When Ans=01 the signal propagates back to the source, denoting that the path is set up, then a data transfer can be started immediately. When Ans=11(nAck) end-to-end flow control is maintained when the receiving end is not ready to receive data being busy with other tasks, or overflow at the receiving buffer. An Ans=10(Back) means that the link is blocked. This Back code is used for a backpressure flow control of the dynamic path-setup scheme, which is discussed in the following subsection.

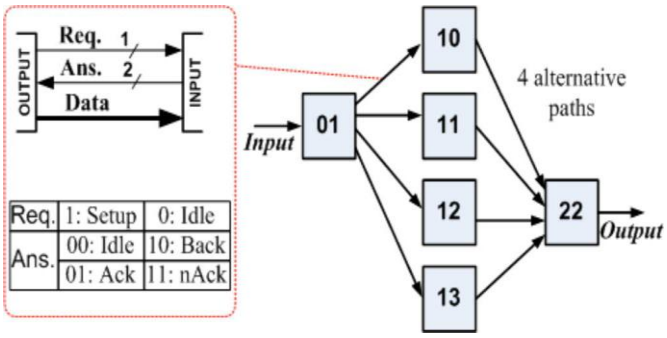

Figure 3: Path-diversity

III. ERROR CORRECTION TECHNIQUES

To identify reliability issues in on-chip interconnects Error control coding (ECC) techniques are used [16]–[22], but these techniques generally target transient errors rather than permanent errors. A permanent fault can reduce or even eliminate the correction capabilities the codes. ECC research applied to on-chip networks considers only

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transient errors; protection against permanent or intermittent errors is rarely discussed. Two recovery techniques are used when an error on a link has been detected. In Automatic Repeat Query (ARQ), a retransmission is requested, while in Forward Error Correction (FEC), check bits transmitted together with the data are used to correct errors without the need for retransmission [24].

3.1 SPARE RESOURCES

The use of spare modules to replace erroneous ones, in array structures, is a long-known fault-tolerant approach [27]. Spare cells and wires are used in field-programmable gate arrays to bypass defective components [28],[29]. Refan *et al.* use spare wires to recover from switch failure by connecting each processing element to two switches in a network-on-chip (NoC); if a permanent fault occurs in one switch, processing elements share the working switch, and the system reroutes its data accordingly. Grecu *et al.* have analysed the use of spare wires in NoCs to increase manufacturing yield; reconfiguration of the links used crossbar switches with redundant channels. The presented reconfiguration system uses a synchronous design methodology and FEC to achieve higher throughput.

3.2. PERMANENT ERROR CORRECTION

Permanent-error correction using spare wires in on-chip network is a two-step process. The permanent error must be detected first followed by link must be reconfiguration to avoid transmitting over the faulty wire.-

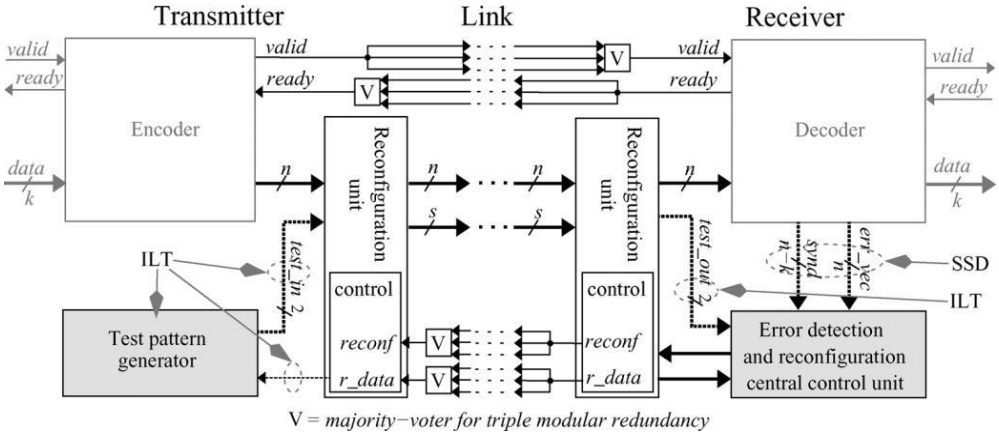

Figure 4: Reconfigurable link system.

The adaptive link framework is shown in Figure and consists of a transmitter, a link, and a receiver. The incoming -bit-wide data word is encoded in the transmitter to a code word of width, which is transmitted through the link and decoded in the receiver. Decoder corrects any errors and outputs the original –bit data word. More number of spare wires is available. Reconfiguration units at the transmitter and receiver determine the lines carry data and which are left idle. The reconfiguration control units pass the information between the receiver and transmitter and synchronize reconfiguration.

The error detection and reconfiguration control unit detects permanent errors and initiates reconfiguration. The input to this control unit depends on the method of detection. For the ILT method, test outputs from the spare

wires under test are needed. The ILT method requires a Test Pattern Generator (TPG) block and test inputs to produce test signals. The techniques are applied to permanent and intermittent errors in the link; the logic units are assumed to function correctly.

IV. ILT METHOD

The ILT method routes data sequentially from each pair of adjacent wires to a set of available spare wires, allowing each pair to be tested for intermittent and permanent faults. This is achieved without interrupting data transmission, by making use of the reconfiguration system. To protect against runtime permanent errors, the ILT is run periodically, with a period that can be shortened to improve error or increased energy efficiency. With this periodic testing, the ILT can be triggered when an error is detected beyond the error correction capability of the code protecting the link. The trigger can be controlled by an upper protocol layer (e.g., application) to save energy during idle periods.

V. CONCLUSION

This paper presents an on-chip network design which supports traffic permutation in MPSoC applications. A reconfiguration system utilizes spare wires for erroneous wires without interfering data transmission. Energy, latency and throughput are improved considerably. This adaptive system provides tolerance against number of permanent errors equal to the number of spare wires in the system. A reconfigurable system uses spare wires to replace erroneous wires and enable reconfiguration without interfering with data transmission h. The results show that the approach provides tolerance against a number of permanent errors equal to the number of spare wires in the system.

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