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Implementation and Analysis of Cascaded H Bridge Multilevel Inverter Using Space Vector PWM

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ABSTRACT

The implementation and analysis strategies plays vital role to minimize THD in Multilevel inverter. The modulation technique regards Selective harmonic Elimination and Space Vector Pulse Width Modulation(SVPWM).Multilevel inverters has tremendous application in the area of high-power and medium-voltage energy control. In this paper simulation of SVPWM is performed for cascaded H bridge Multilevel inverter . Simulation of three,five ,seven, eleven leves and thirteen levels cascaded H bridge multilevel inverter with Space vector PWM has been carried out. Implementation and Analysis are presented to realize the validity of the Total harmonic distortion.

Keywords: Multilevel Inverter, Pulse Width Modulation, Space Vector Pulse Width Modulation, Total Harmonic Distortion.

I. INTRODUCTION

Numerous industrial applications require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. A multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations Subsequently, several multilevel converter topologies have been developed.A multilevel converter not only achieves high power ratings but also enables the use of renewable energy sources. The advantages of three-level Inverter topology over conventional two-level topology are 1)The voltage across the switches is only one half of the DC source voltage 2)The switching frequency can be reduced for the same switching losses 3)The higher output current harmonics are reduced by the same switching frequency.

I.space vector PWM technique is used for variable frequency drive applications.It utilizes DC bus voltage more effectively SVPWM utilize a chaotic changing switching frequency to spread the harmonics continuously to awide brand area so that the peak harmonics can be reduced greatlyease of use.

II.BASIC PULSE WIDTH MODULATION TECHNIQUES

i) Single Pulse Width Modulation:

In Single Pulse Width Modulation control, the width of the pulse is varied to control the inverter output voltage and there is only one pulse half per cycle. By comparing the rectangular reference signal with the triangular

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carrier wave the gating signals are generated as shown in Fig 1. The frequency of reference signal determines fundamental frequency of output voltage.

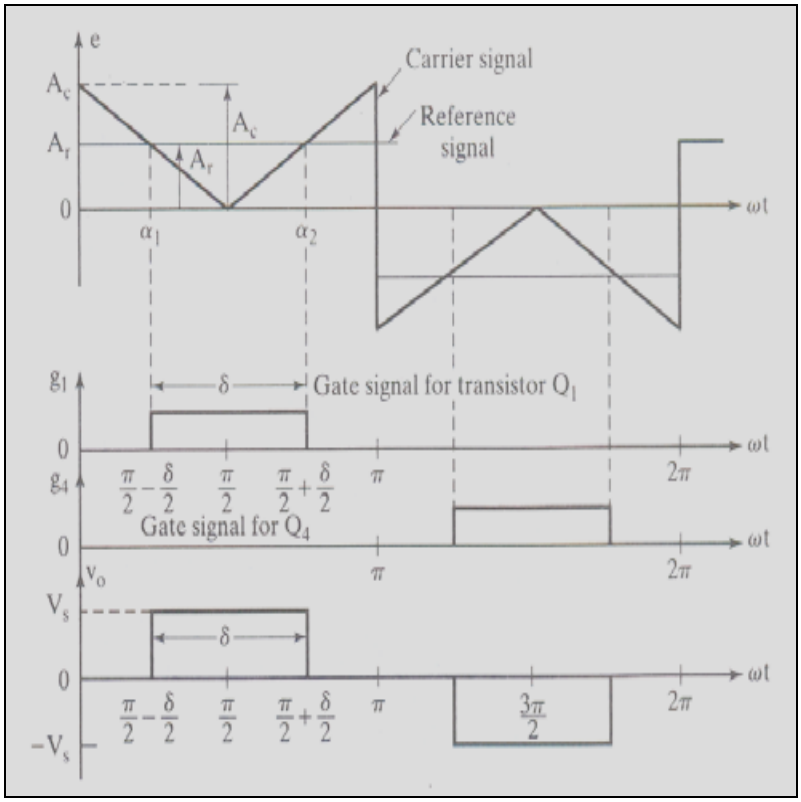

Fig 1.Single pulse width modulation

Advantages:

1. The even harmonics are absent due to the symmetry of the output voltage along the x-axis.
2. Nth harmonics can be eliminated from inverter output voltage if the pulse width is made equal to $2\pi/n$.

Disadvantages:

1. The output voltage introduces a great deal of harmonic content.
2. At a low output voltage the distortion factors increases significantly

ii) Multiple Pulse Width Modulation:

In Multiple Pulse Width Modulation several equidistant pulses per half cycle are generated as shown in Fig 2. By using several pulses in each half cycle of output voltage the harmonic content can be reduced.

Advantages:

1. Amplitudes of lower order harmonics are reduced.
2. Derating factor is reduced significantly.

Disadvantages:

1. The fundamental component of output voltage is less.
2. The amplitudes of higher order harmonics increases significantly.
3. Switching losses are increased.

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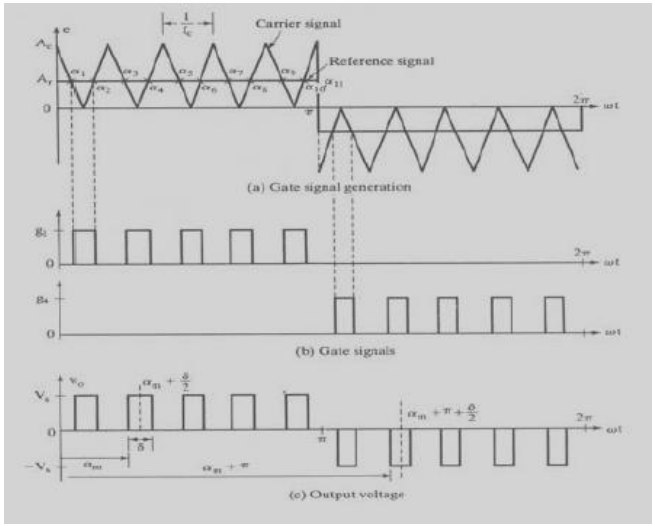

Fig.2. Multiple pulse width modulation

iii) Sinusoidal Pulse Width Modulation:

In Multiple Pulse Width Modulation, by varying the width of each pulse in proportion to the amplitude of the reference wave the distortion factor and lower order harmonics can be reduced significantly and the width of all the pulses are maintained the same. This type of modulation is commonly used in industrial applications and is known as Sinusoidal Pulse Width Modulation.

By comparing sinusoidal reference signal with a triangular carrier wave of frequency, f_c, the gating signal is generated. The inverter output frequency, f_o, and its peak amplitude, A_r, determines the frequency of reference signal fr and controls the modulation index, M, and then in turns the rms output voltage, Vo. The number of pulses per half cycle depends upon the carrier frequency.

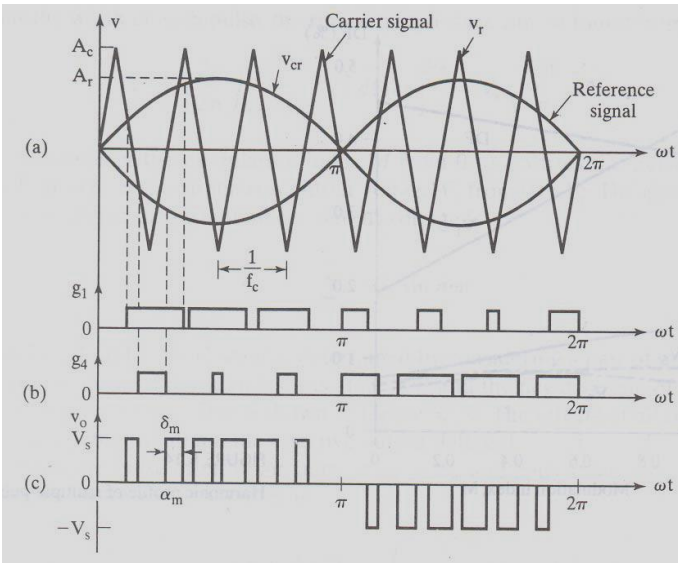

Fig.3. Sinusoidal pulse width modulation

By varying the modulation index M, the rms output voltage can be varied. Each pulse corresponds approximately to the area under sine wave between the adjacent midpoints of off periods on the gating signals. If δ_m is the width of the m^{th} pulse, the rms output voltage can be found from

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$$v_0 = v_s \sqrt{\sum_{m=1}^{p} \frac{\delta m}{\pi}} \quad \text{----------} \quad 2.1$$

The distortion factor is significantly reduced compared to that of multiple Pulse modulations. This type of modulation eliminates all harmonics less than or equal to 2p-1.

For p=5, the lowest order harmonic is ninth.

iv) Advanced Modulation Techniques:

Trapezoidal modulation:

By comparing a triangular carrier wave (Vc) with a reference trapezoidal wave (Vr), the switching instance to semiconductor devices are generated. This type of modulation increases the peak fundamental output voltage up to 1.05Vd, but output voltage contains lower order harmonics.

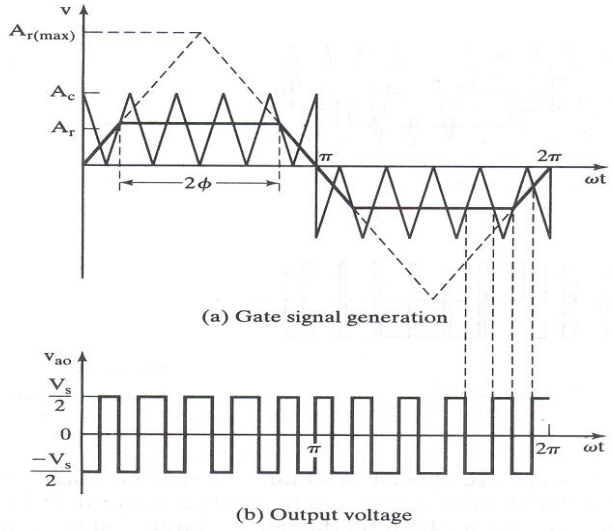

Fig.4 Trapezoidal modulation

v) Staircase modulation

In staircase Pulse Width Modulation the modulated wave eliminates specific harmonics. In order to obtain desired quality of output voltage, the modulation frequency ratio mf and the number of steps are chosen. If the number of pulses is less than 15 per half cycle this is optimized PWM.

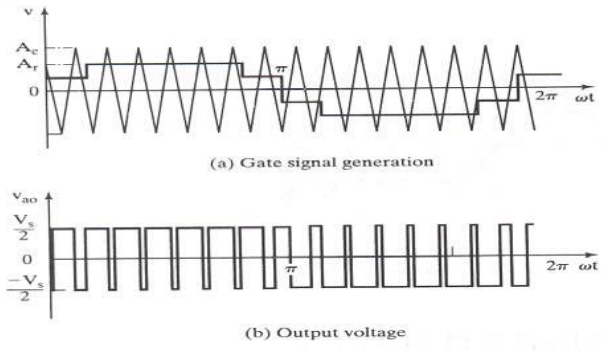

Fig.5 Staircase modulation

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vi) Stepped modulation

In this modulation the signal is stepped wave. In order to control the magnitude of the fundamental component and to eliminate specific harmonics this wave is divided into specific intervals, with each interval being controlled individually. When compared to that of normal Pulse Width Modulation control this type control gives low distortion but higher fundamental amplitude.

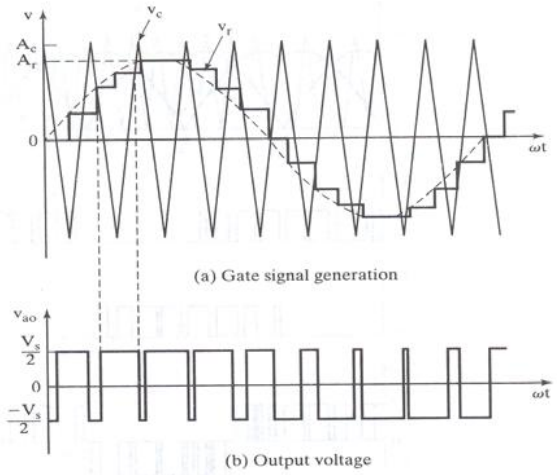

Fig.6 Stepped modulation

vii) Harmonic Injected modulation

In this modulation the signal is generated by injecting harmonics to the sine wave. The result is a flat topped wave form and it reduces the amount of over modulation. A higher fundamental amplitude and low distortion of output voltage is provided. The amplitude of fundamental components is approximately 15% more than that of normal sinusoidal Pulse Width Modulation.

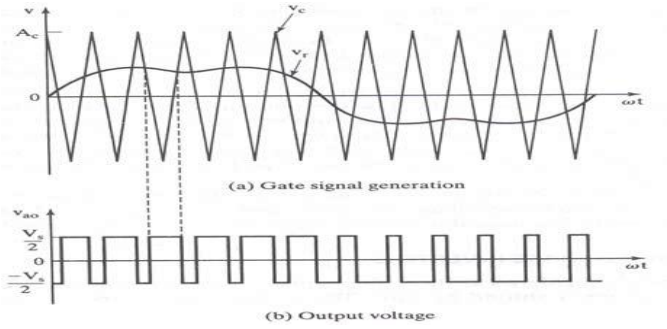

Fig.7 Harmonic injected modulation

viii) Delta modulation

In this modulation a triangular wave is allowed to oscillate within a defined window Δv above and below the reference wave Vr. From the vertices of the triangular wave Vc, the output voltage is generated. This type of modulation is also known as Hysteresis modulation. Keeping the slope of the triangular wave constant, if the frequency of modulating wave is changed, the number of pulses and pulse widths of modulated wave would change.

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The fundamental output voltage can be uptoVs and is dependent on peak amplitude Ar and frequency fr of reference voltage. This modulation can control the ratio of voltage to frequency. Depending on the permissible harmonic content in the inverter output voltage, machine type, power level and semi conductor switching devices employed for a particular application, the particular Pulse Width Modulation is choose.

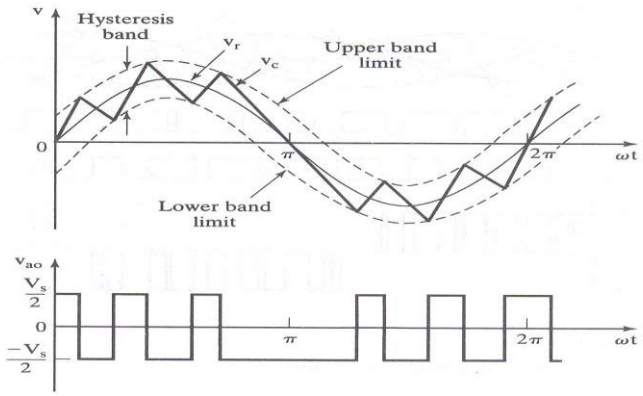

Fig.8 Delta modulation

ix) Space Vector Pulse Width Modulation:

This modulation is relatively new and popular technique in controlling motor devices. By combing the switching states corresponding to the basic space vector, the reference voltage is approximated. The main advantage of this technique is that it will generate less harmonic distortion in the output voltages and currents.

Advantages of PWM Techniques:

- Using Pulse Width Modulation techniques lower order harmonics can be eliminated or minimized along with its output voltage control. The filtering requirements are also minimized.
- Both the output voltage and frequency control is possible in a single power stage of the inverter without any additional components.
- The presence of constant DC supply permits the parallel operation of several independent Pulse Width Modulation inverters on the same rectifier power supply. Pulse Width Modulation inverter has a transient response which is much better than that of quasi-square wave rectifier.

III.SVPWM SCHEME

Space Vector Modulation(SVM) is an algorithm for the control of pulse width modulation (PWM).It is used for the creation of alternating current (AC) waveforms; most commonly to drive 3 phase AC powered motors at varying speeds from DC using multiple class-D amplifiers. There are various variations of SVM that result in different quality and computational requirements. One active area of development is in the reduction of total harmonic distortion (THD) created by the rapid switching inherent A three phase inverter as shown to the right converts a DC supply, via a series of switches, to three output legs which could be connected to a three-phase motor.

The switches must be controlled so that at no time are both switches in the same leg turned on or else the DC supply would be shorted. This requirement may be met by the complementary operation of the switches within a

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leg. i.e. if A^+ is on then A^- is off and vice versa. This leads to eight possible switching vectors for the inverter, V_0 through V_7 with six active switching vectors and two zero vectors.

3.1 SVPWM SCHEME

For an *n*-level inverter the output voltage vector in this paper is defined as

$$V_{out} = (n-1).(u_a + u_b.e^{j\frac{2}{3}\pi} + u_c.e^{j\frac{4}{3}\pi} \quad ---------- \quad 3.1$$

whereu_a, u_b, and u_c are the instantaneous output voltages of phases A, B, and C of the inverter, respectively, relative to the negative terminal of the DC source. When assuming the voltages on the DC-link capacitors are identical, the output voltage vector becomes.

$$V_{out} = V_{dc}.(s_a + s_b.e^{j\frac{2}{3}\pi} + s_c.e^{j\frac{4}{3}\pi} \quad ---------- \quad 3.2$$

Where V_{dc} is voltage of the DC source, and S_a, S_b, and S_c(S_a, S_b ,*S*c=0, 1, …*n*-1) are the switching states of phases A, B, and C, respectively. Accordingly, the voltage of each DC-link Capacitor is V_{dc}/(*n*-1), and the output voltages of phase A, B, and C relative to the negative terminal of the DC source are*Sa*·V_{dc}/(*n*-1), *S*b·V_{dc}/(*n*-1), and S_c·V_{dc}/(*n*-1), respectively.

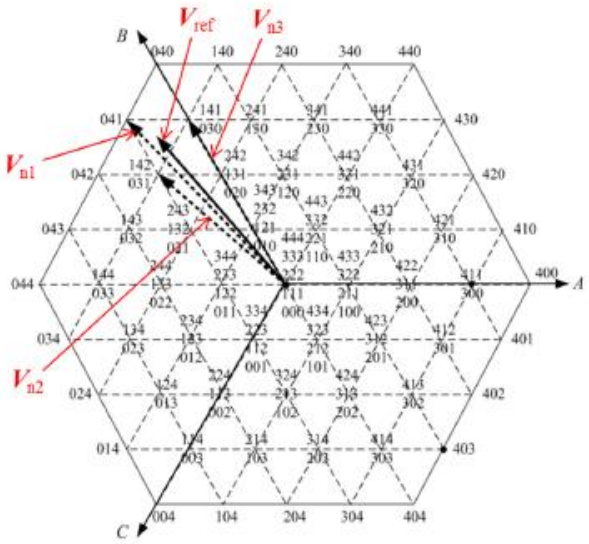

Fig.9.Space vector diagram of a five-level inverter

A space vector diagram containing all the output vectors and the corresponding switching states of the inverter can be generated . For example, Fig.3.3 shows the space vector diagram of a five-level inverter calculated in this way, where $\boldsymbol{V}_{ref}$ is the reference or desired voltage vector, and $\boldsymbol{V}_{n1}$, $\boldsymbol{V}_{n2}$, and $\boldsymbol{V}_{n3}$ are the corresponding nearest three vectors. It is the task of the SVPWM scheme to synthesize the reference vector as follows

$$T_s.V_{ref} = d_1.V_{n1} + d_2.V_{n2} + d_3.v_{n3} \quad ---------- \quad 3.3$$

where*T*s is the commanded switching cycle, and *d*1, *d*2, and *d*3 are the duty cycle times of ***V***n1, ***V***n2, and ***V***n3, respectively.

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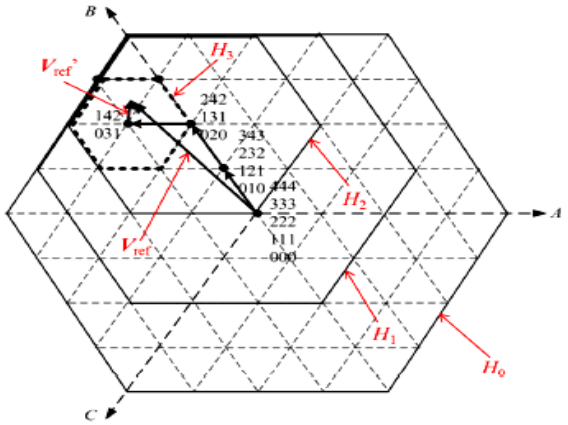

Fig.10.Location method for the reference vector

The SVPWM scheme proposed is shown in Fig. 10. It can generate all the available switching sequences and the corresponding duty cycles according to thereference voltage and the commanded switching frequency forany level of inverter. For purposes of demonstration, theSVPWM is illustrated based on the space vector diagram ofthe five-level inverter shown in Fig.9. The detailed method of generating the switching sequences and calculating the corresponding duty cycles is introduced as follows.

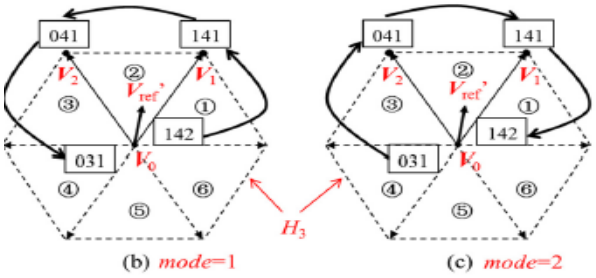

Fig11.switching sequence modes

3.2 SWITCHING SEQUENCE

First, the reference vector $\boldsymbol{V}_{ref}$ is represented as the sum of a set of "vertex vectors" and a "remainder vector"$\boldsymbol{V}_{ref}$, as shown in Fig. 10. A vertex vector is a vector connecting two adjacent vertices. The vertex vectors connect the centre vertex of the *n*-level space-vector diagram *H*0 with a first vertex of the "modulation triangle" (composed by the vertices of the nearest three vectors ***V***n1, ***V***n2, and ***V***n3 as in Fig.9). The remainder vector is the vector enclosed by the modulation triangle and connecting the first vertex of the modulation triangle with the reference vector.

One way to determine the set of vertex vectors is based on determining a set of nested hexagons *H*1, *H*2, and *H*3enclosing the reference vector, as shown in Fig. 10. Each nested hexagon corresponds to a specific level ranging from (*n*-1) to a second level, and centers at the vertex of a vertex vector. For instance, the method of selecting the nested (*n*-1)-level hexagon *H*1 is shown in Fig.12. There are six vertex vectors available for the nested (*n*-1)-level hexagon *H*1, i.e., the one blue solid arrow and five blue dashed arrows as shown in Fig. 12. The actual vertex vector, among the six available vertex vectors, for the nested (*n*-1)-level hexagon *H*1 is the one for which the angle between this vertex vector and the reference vector is the smallest. In this way, the first

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vertex vector can be selected, as the blue solid arrow shown in Fig.12, and the origin of the reference vector is shifted to the vertex of the selected vertex vector, which is the center vertex of the selected nested hexagon *H*1. The other nested hexagons can be selected in a similar way.

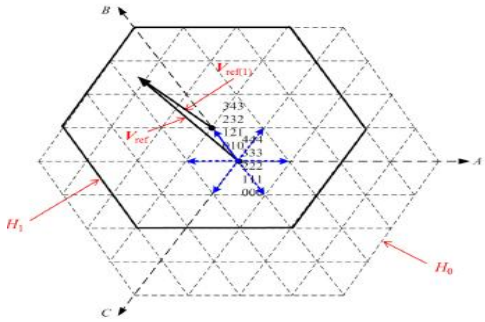

Fig.12. Selection of the vertex vectors and nested hexagons

Second, based on a function *s* of the angle φ of the corresponding vertex vector relative to axis *A*, determine iteratively the switching states at the vertices for each vertex vector in the set of vertex vectors, starting from the present switching states of the inverter at the origin vertex, by modifying (increase or decrease by 1) a corresponding phase of the present switching states to produce the switching states of the inverter at the first vertex of the modulation triangle. The function *s* of the angle φ ($0 \leq \varphi < 2\pi$) of the corresponding vertex vector can be described as

S=3 +1 ----------3.

IV.SIMULATIONRESULTS

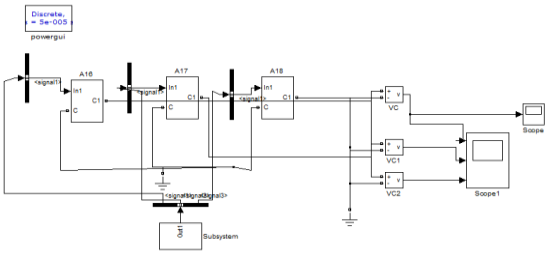

Fig.4.1 Three level H-bridge inverter

The FFT analysis five level cascaded H bridge inverter with SVPWM is shown in the Fig.4.2

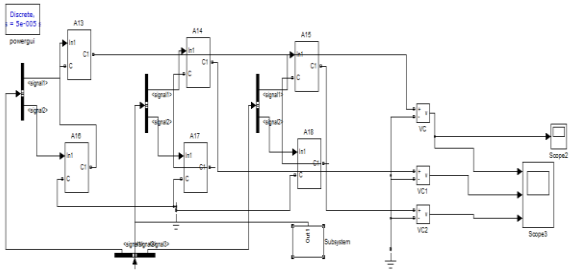

Fig.4.2 Five level H-bridge inverter

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The FFT analysis of seven level cascaded H bridge inverter with SVPWM is shown in the Fig.4.3

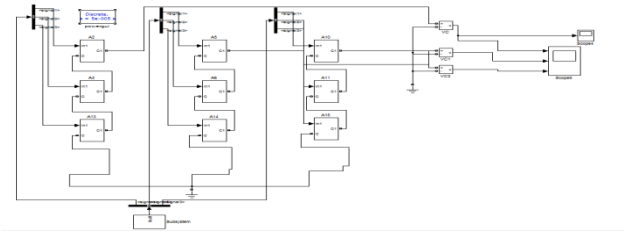

Fig.4.3 Seven level H-bridge inverter

The FFT analysis of eleven level cascaded H bridge inverter with SVPWM isisas shown in the Fig.4.4

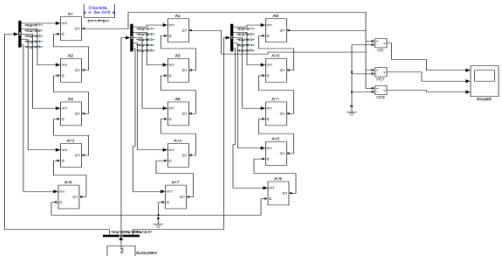

Fig.4.4 Eleven level H-bridge inverter

The FFT analysis of thirteen level cascaded H bridge inverter with SVPWM is as shown in the Fig 4.5.

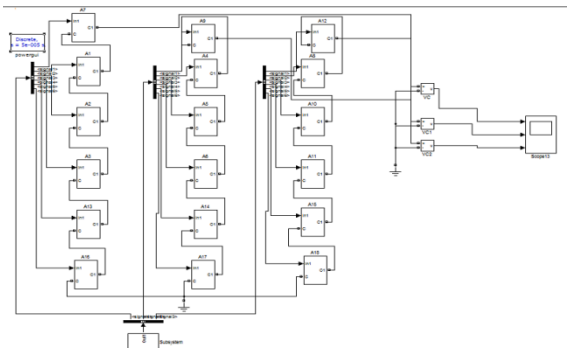

Fig.4.5 Thirteen level H-bridge inverter

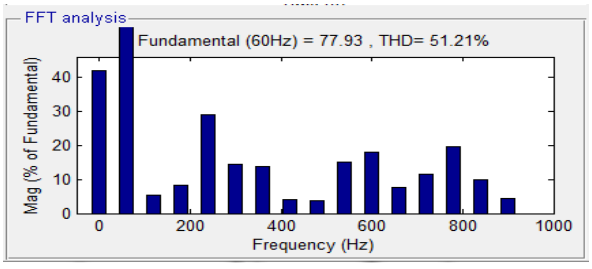

Fig.4.6The FFT analysis of three cascaded H bridge inverter with SVPWM is shown in the Fig.4.1

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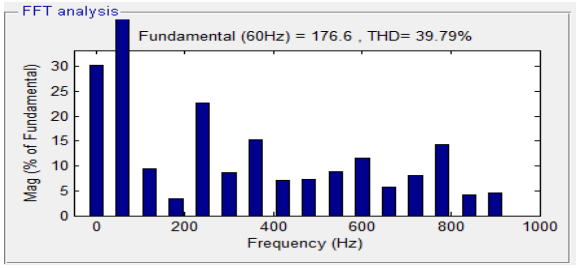

Fig.4.7 The FFT analysis of five level cascaded H bridge inverter

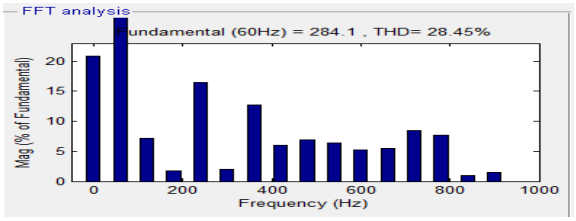

Fig.4.8The FFT analysis ofseven level cascaded H bridge inverter

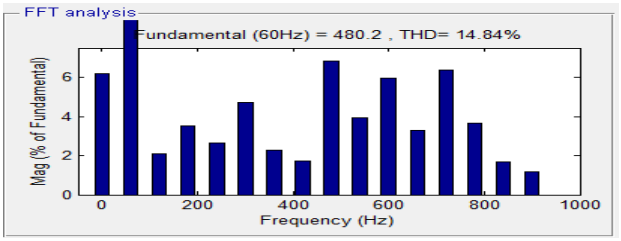

Fig.4.9.The FFT analysis ofelevenlevel cascaded H bridge inverter

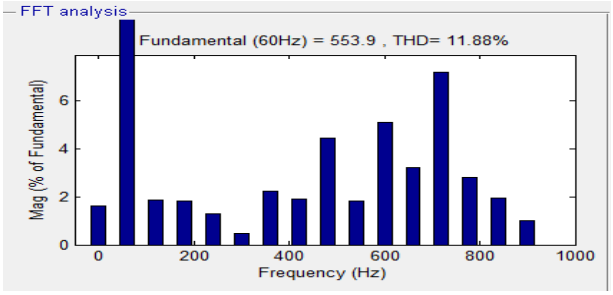

Fig.4.10.The FFT analysis of thirteenlevel cascaded H bridge inverter

Level	THD(%)
3	51.21
5	39.79
7	28.45
11	14.84
13	11.88

Table1. THD Analysis

V. CONCLUSION

simulation of SVPWM is performed for cascaded H bridge Multilevel inverter . Simulation of three, five ,seven, eleven leves and thirteen levels cascaded H bridge multilevel inverter with Space vector PWM has been carried out and Total harmonic distortion calculated.

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